Radiation Mitigation Techniques (*for Mixed-Signal Circuits*)

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Hardening Techniques for AMS Circuits

- Radiation Effects in AMS Circuits: Unique issues and considerations
- Total Ionizing Dose and Basic Mitigation Strategies
- Single Event Effects and Basic Mitigation Strategies
- Hardening by Design for AMS
- A look to the future
- Summary

Radiation Effects in Analog Circuits

1838 IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 40, NO. 6, DECEMBER 1993

Observation of Single Event Upsets in Analog Microcircuits

R. Koga, S.D. Pinkerton, S.C. Moss, D.C. Mayer, S. LaLumondiere,
S.J. Hansel, K.B. Crawford, and W.R. Crain
The Aerospace Corporation
PO Box 92957, Los Angeles, CA 90009

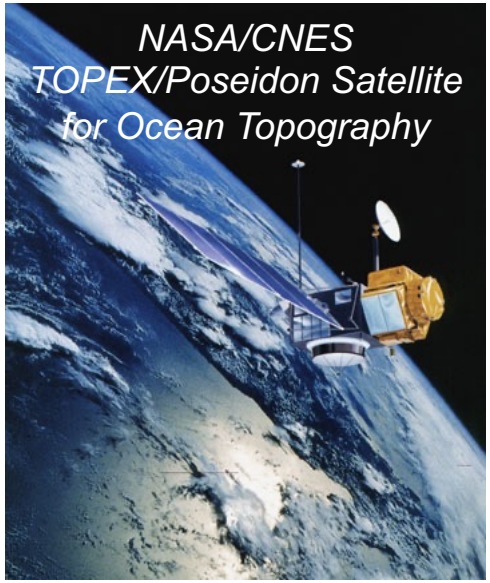
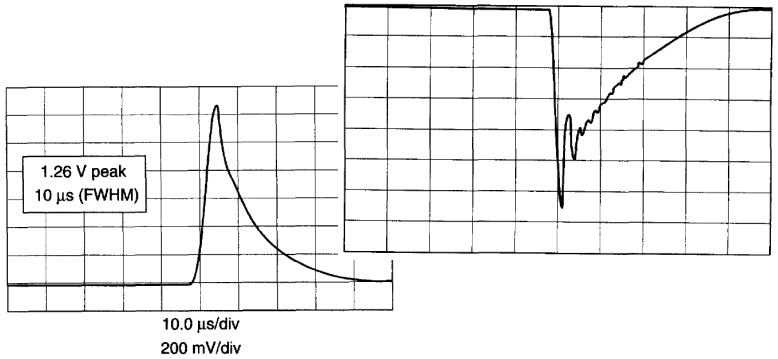
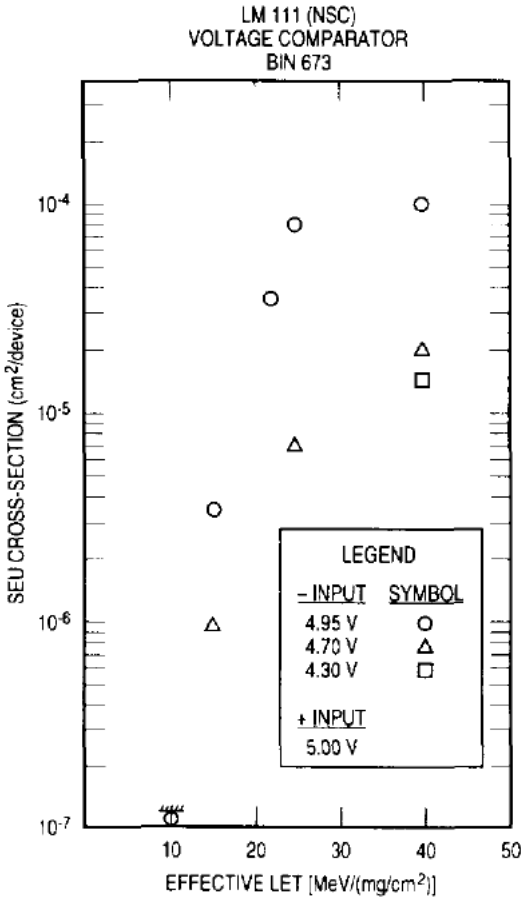


Image courtesy JPL/NASA





Emergence of RHBD AMS

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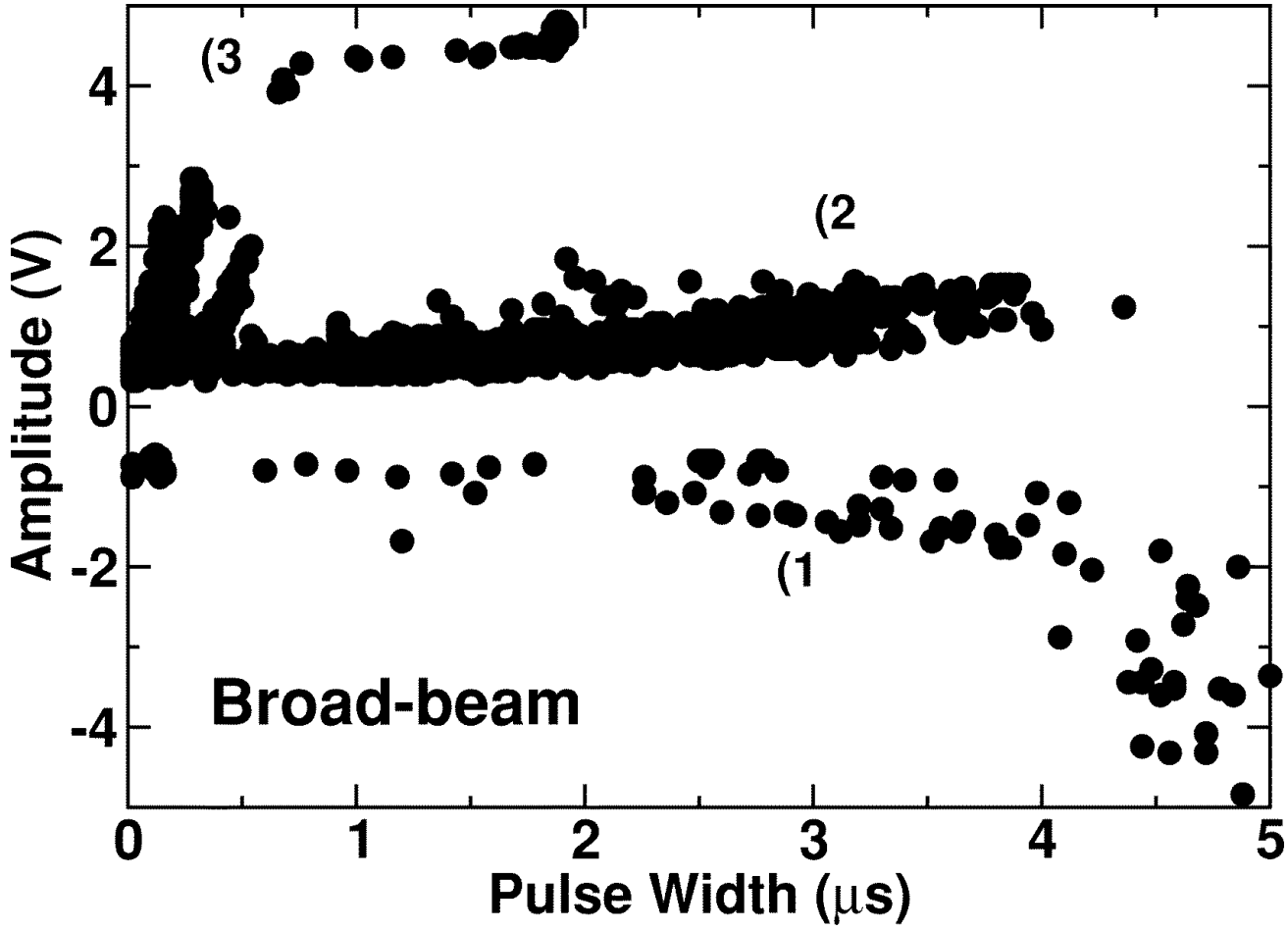
- Suggested the first 2 “mixed-signal” strategies for mitigating single event effects (SEE) that have since become commonplace
  - Temporal redundancy: It was suggested that multiple consecutive samples could be taken at the analog-to-digital interfaces (thresholds)
  - Increase design margins/relax tolerances (i.e., system design): It was noted that this strategy was used in TOPEX

Complex Response Signatures

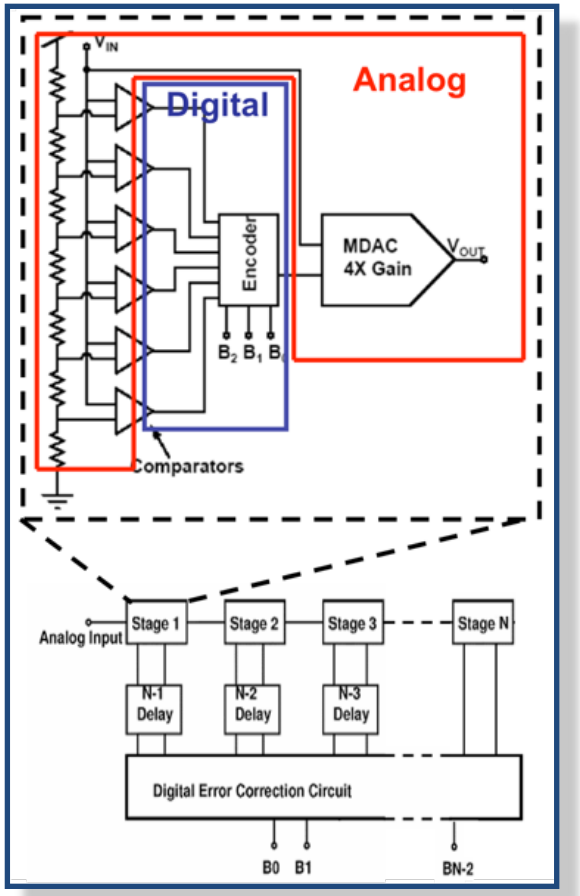
- Almost 30 years later, there is no single, standard metric for SEE in analog and mixed-signal (AMS) systems as the effect of an SEE is dependent on the **topology**, **function**, and the **operating mode**



LM124 Op Amp SEE Signatures
Boulghassoul 2002

RHBD Mixed-Signal Circuits

- If analog functionality can be done with digital technology, it will be!
- However, the ability to put entire systems on a chip has increased the demand for mixed analog/digital (mixed-signal) circuits – AMS is argued to have the highest share of the IC market
- Most SoCs require some analog – processes usually have a separate and higher VDD specifically for analog
- Single-event effects (SEE) present challenges for AMS systems
  - *single-event transients (SET) are subject to cross-domain response mechanisms*
  - *SE mechanisms may be difficult to identify due to complex signal paths*

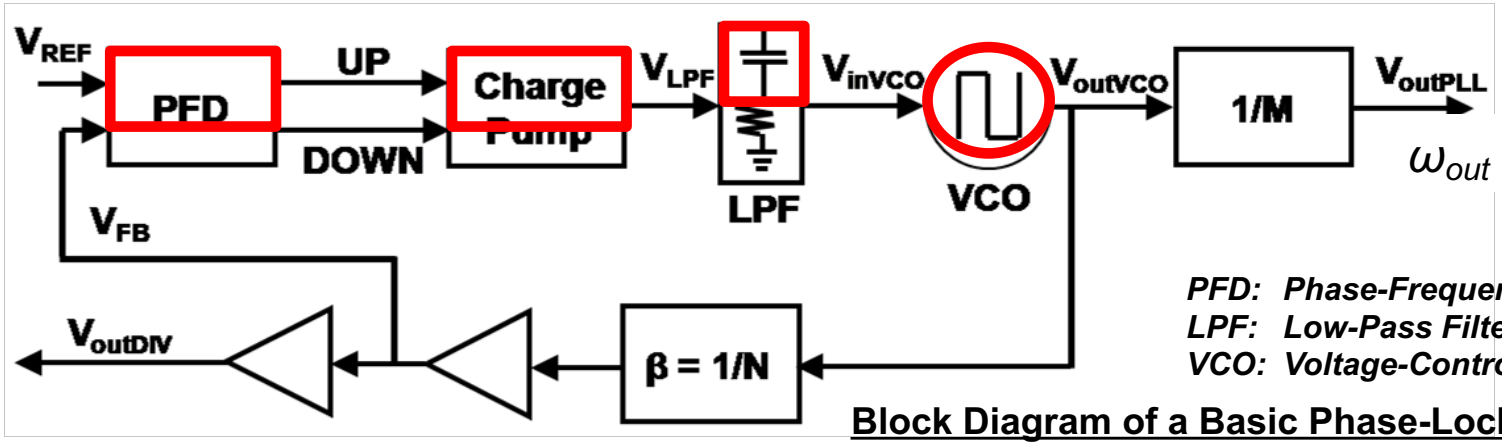


Block Diagram of a Pipelined Analog-to-Digital Converter
Olson 2008

Cross-Domain Response Mechanisms

- Mixed-signal circuits are required to bridge analog and digital domains - consequently, designs are often subject to a variety of response mechanisms
  - *steady-state and transient*
  - *low-frequency and RF*
  - *digital noise and sensitive analog components*
- Single-events are subject to all interactions

Phase → Digital (V) → Analog (I) → Analog (V) → Frequency



Block Diagram of a Basic Phase-Locked Loop (PLL)

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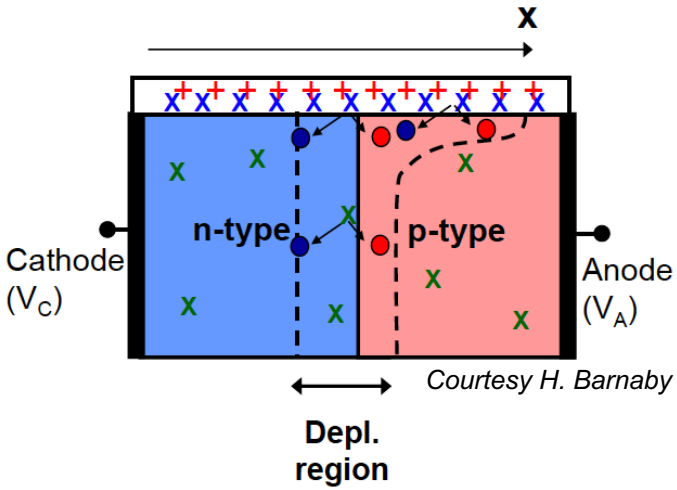
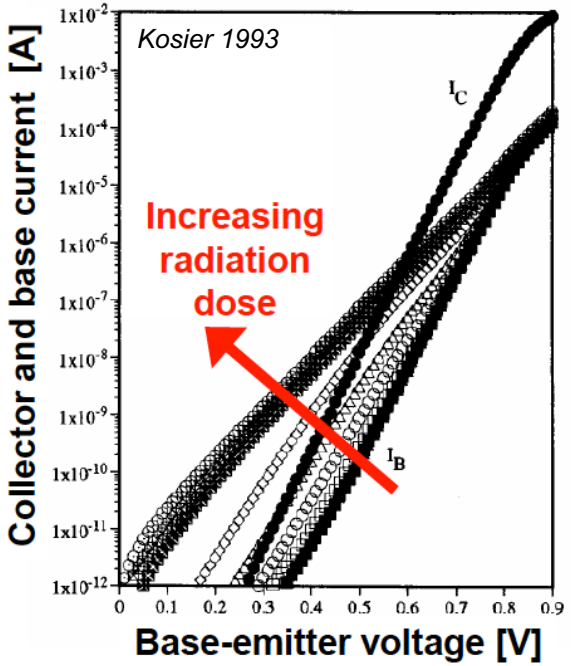
Total-Ionizing Dose Effects





Total-Ionizing Dose (TID) in Microelectronics

Semiconductor device dielectrics:

- **Interface traps** (N_{it}) increase the recombination rate in the depletion region
- **Fixed oxide traps** (N_{ot}) increase the depletion region, thus enhancing recombination
- **Trap defects** increase the generation in RB junctions

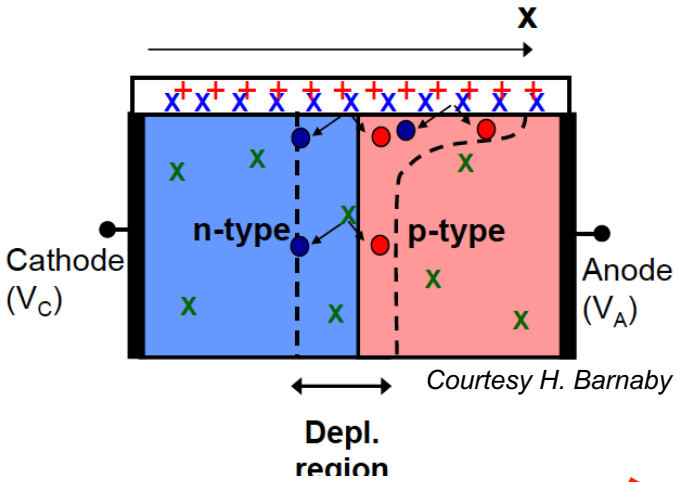
In **BJTs**, TID damage to oxide dielectrics leads to:

- Excess base current (via enhanced recombination with traps and beta degradation)
- Increased collector current in *npn* devices due to increased emitter area (via surface inversion from N_{ot})
- Increased reversed leakage current from collector to base (CB) due to increased carrier generation (via traps) in CB junction

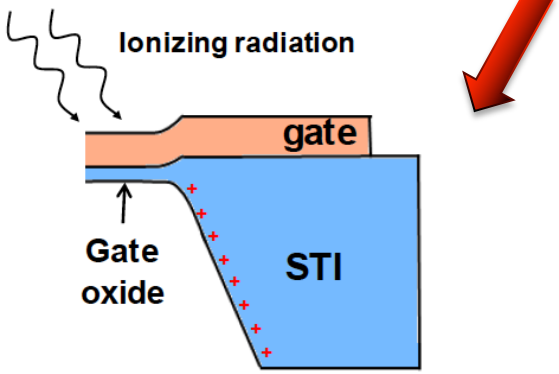
Enhanced Low-Dose-Rate Sensitivity (ELDRS)

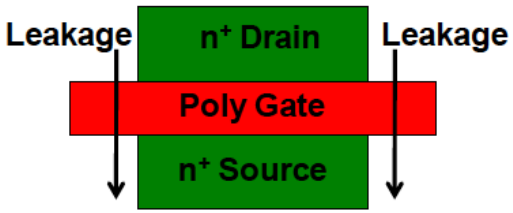
- Larger TID effects observed at low dose-rates (impacts testing methodologies)
- Primarily affects lateral bipolar devices

Total-Ionizing Dose Effects



Courtesy H. Barnaby





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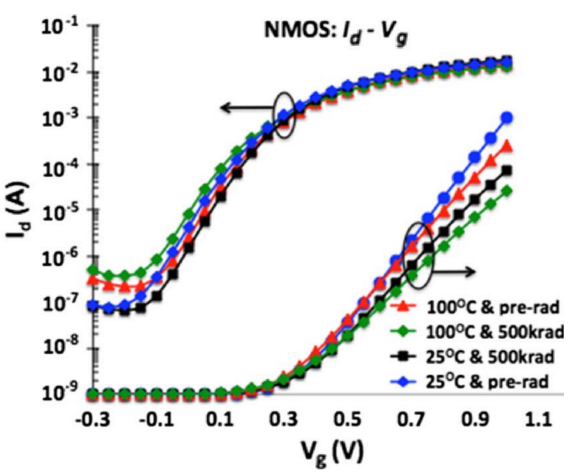
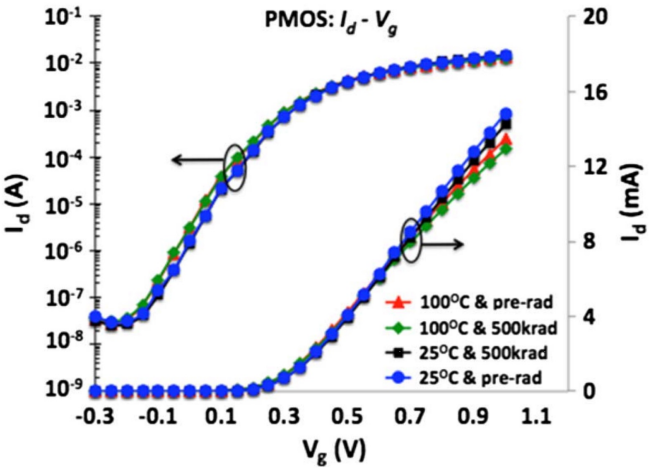
In **CMOS**, TID leads to:

- Threshold voltage (V_t) shifts, sub-threshold slope reduction, and mobility degradation in older CMOS technologies
- Increase intra-device (edge) leakage in nMOS transistors (both old and advanced SOI technologies)
- Increased inter-device leakage in parasitic n-channel devices
- Increased static supply current

Jagannathan 2013

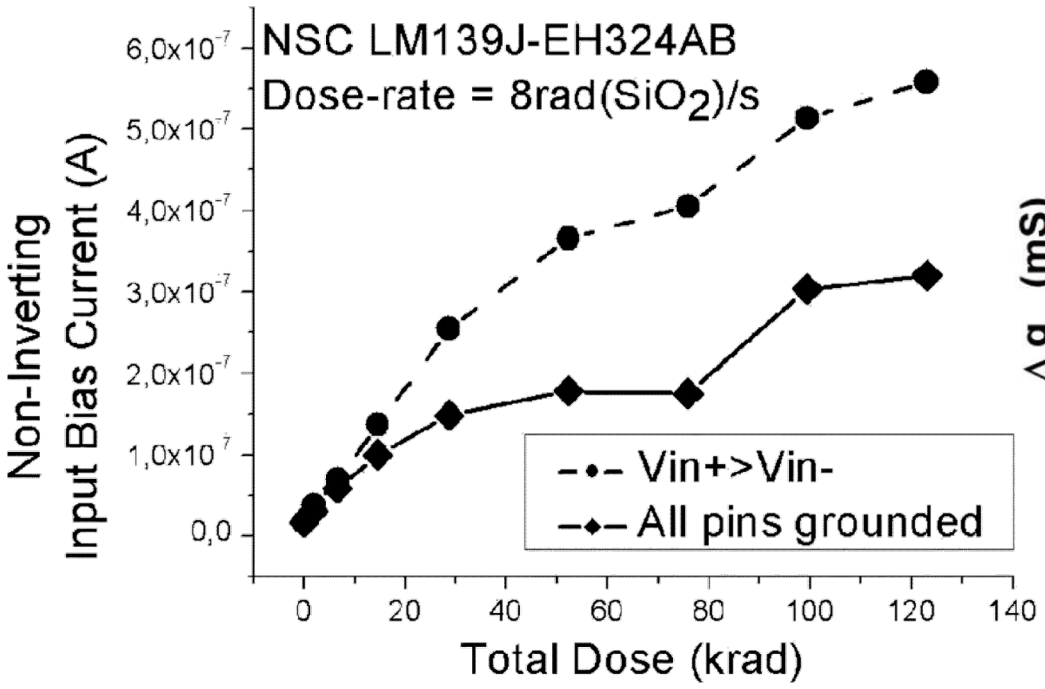




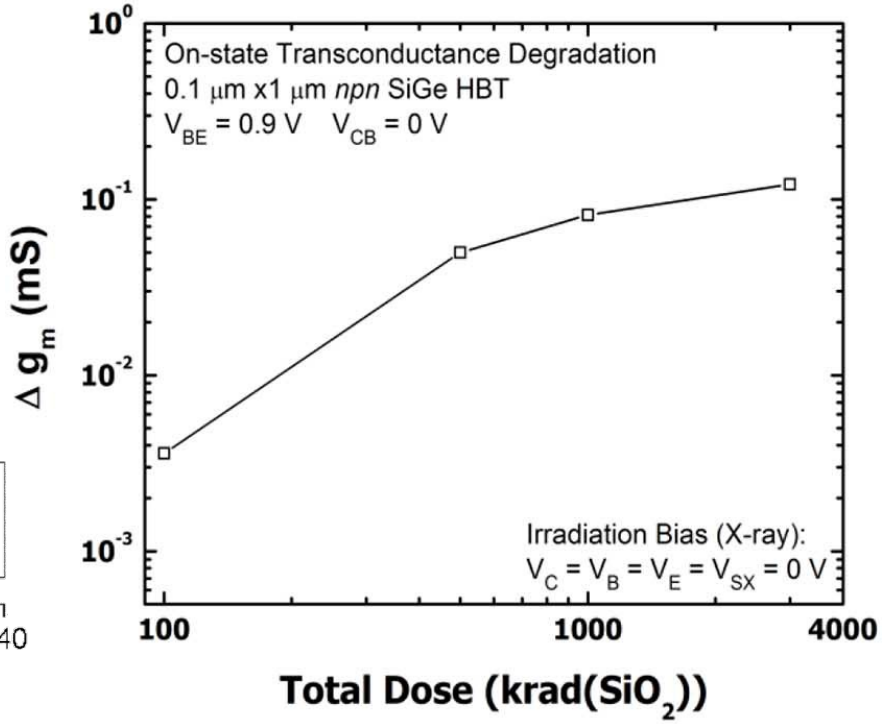
TID in Analog Circuits

Mismatch and degradation in AC parameters due to TID tend to be problematic for analog and RF circuits

Bernard 2006



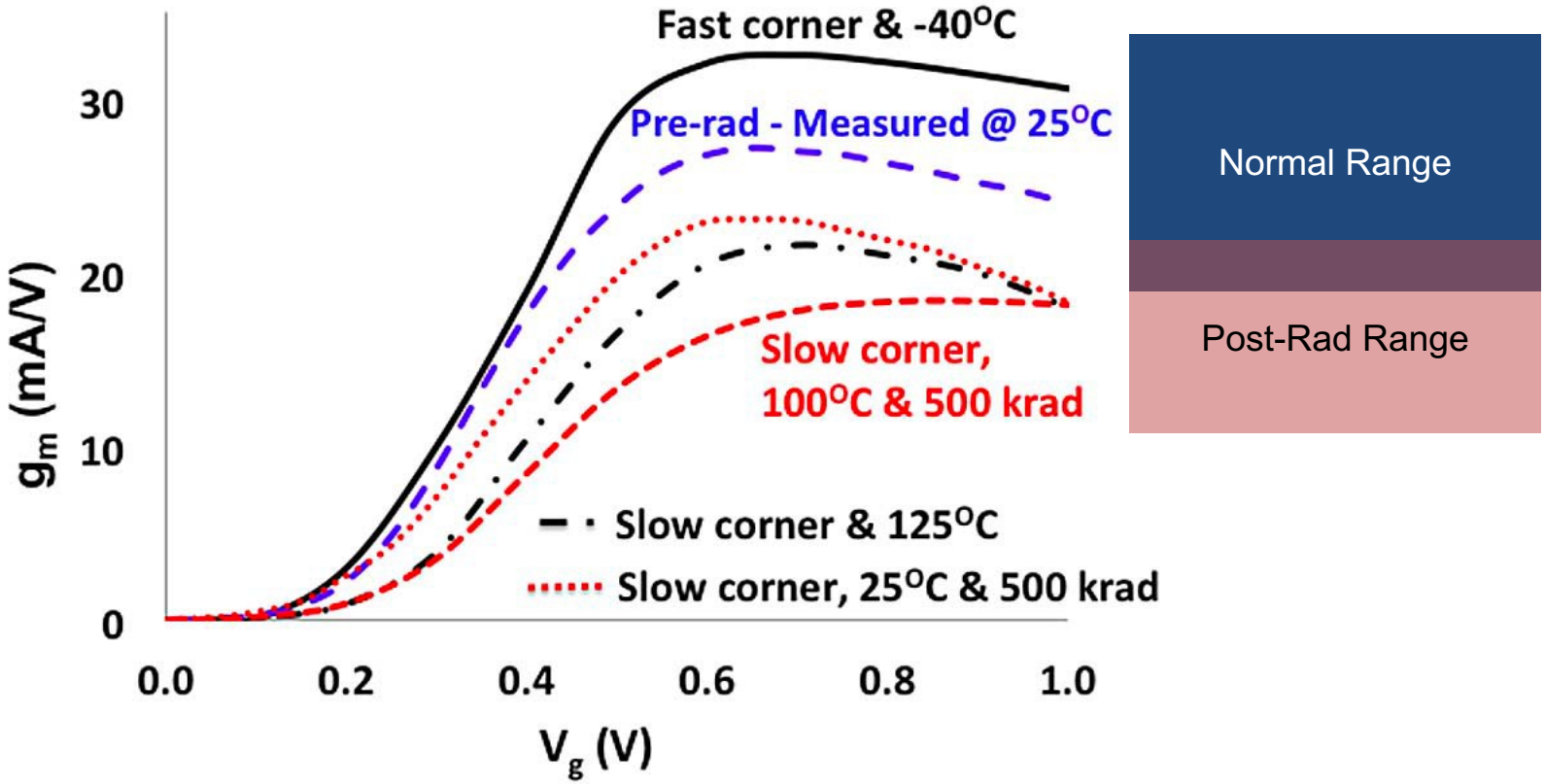
Inanlou 2014



Importance of Temperature

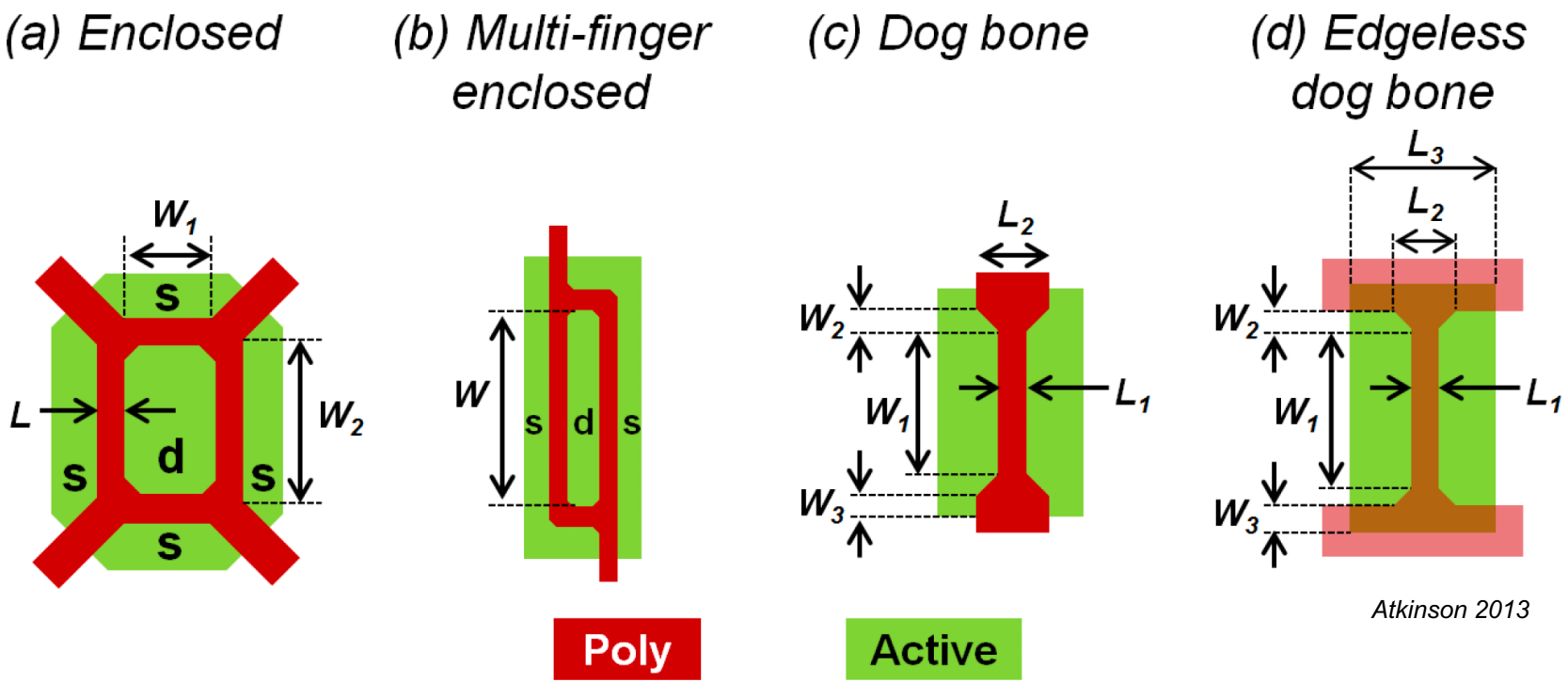
High Performance RF circuits tend to be ultra-sensitive to TID due to the tight design margins (process, voltage, temperature, radiation)

Process-Voltage-Temperature (PVT) and TID Analysis of a Commercial RF 45 nm Process *Jagannathan 2013*



TID Mitigation Through Transistor Layout

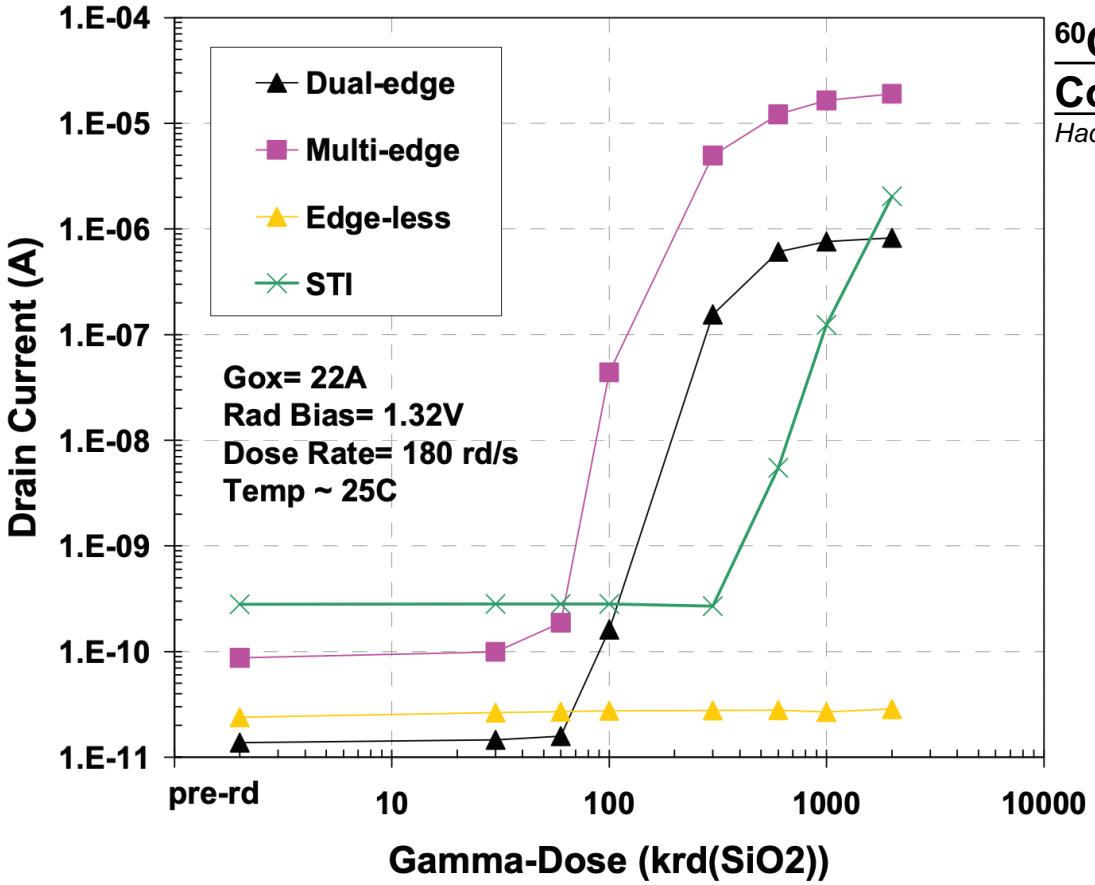
- The most common TID mitigation approach is through individual transistor layout
- Edgeless transistor layout eliminates the radiation-induced sidewall channel leakage in nFETs and reduces trapped charge in the field oxide bordering the channel that can contribute slightly to threshold voltage shifts



Atkinson 2013

Concentric Edgeless Layout

Concentric edgeless layout eliminates STI trapped-charge responsible for leakage



^{60}Co TID Evaluation of a Commercial 90 nm Process

Haddad 2008

Any cell that has not been designed for "critical node isolation" must be investigated for TID-induced failure

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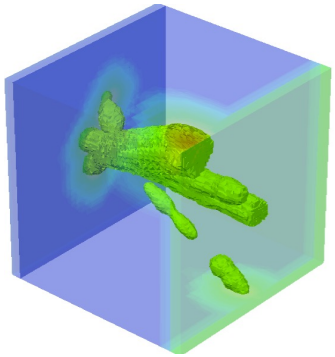
Single-Event Effects



Courtesy Vanderbilt

Single-Event Effects in Microelectronics

Single-Event Effects (SEE):

- Caused by the interaction of a single energetic particle

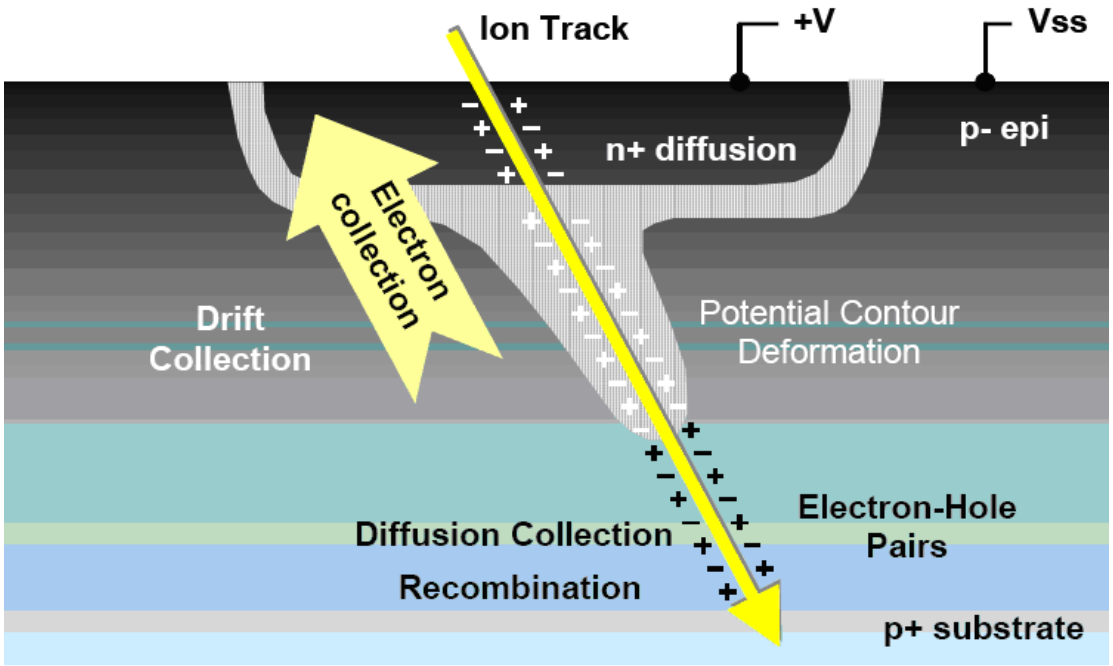
Ionizing Particles:

Heavy ions from deep space
(galactic cosmic rays)

Energetic protons
(trapped in the Van Allen belts)

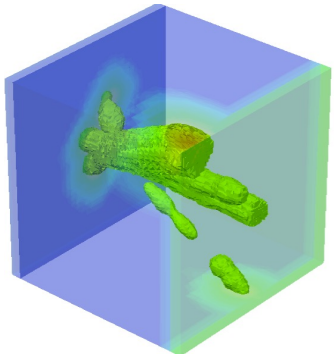
Neutron products
(terrestrial)

Alpha particles
(from contaminants)



Example of Ion Penetrating Reverse-Biased p-n Junction

Single-Event Effects



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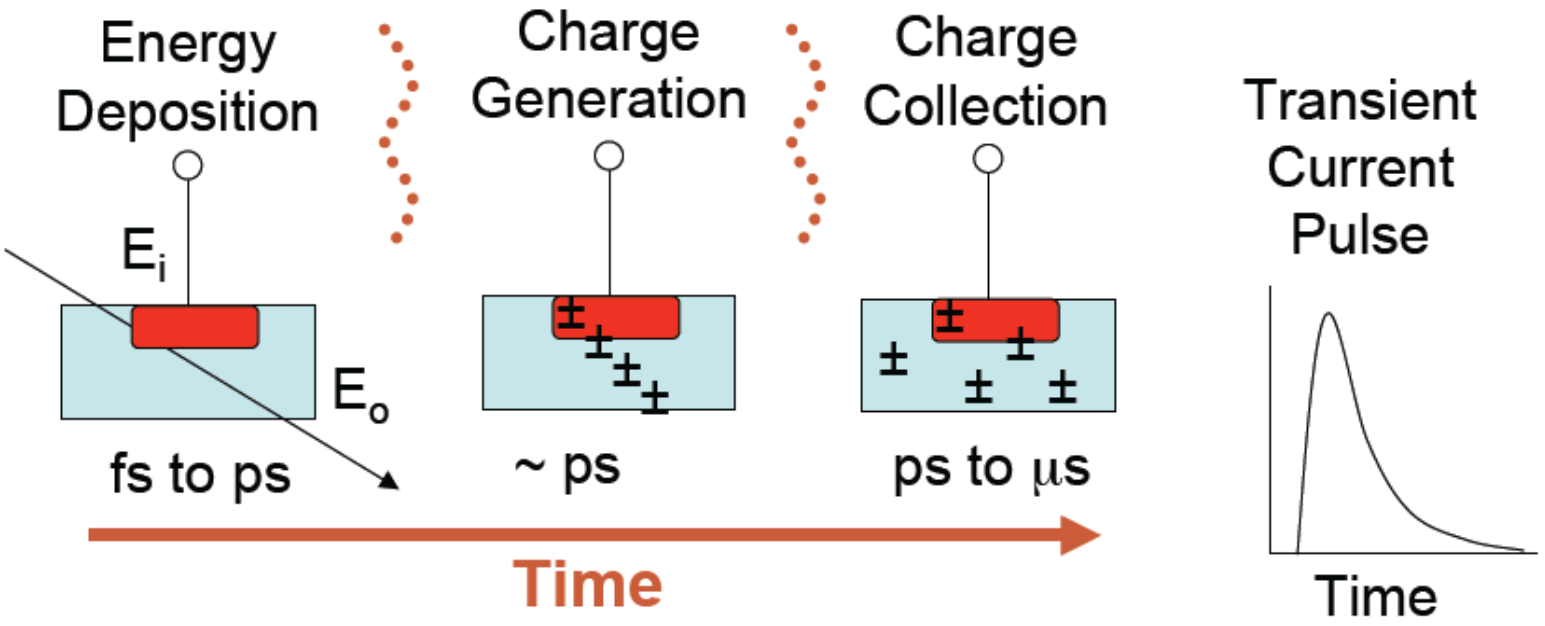
Single-Event Effects in Microelectronics

Single-Event Effects (SEE):

- Caused by the interaction of a single energetic particle
- SEE are determined by:
  - Charge generation
  - Charge collection
  - Circuit response



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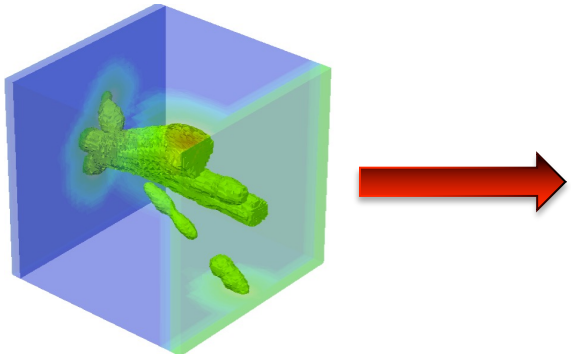

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Single-Event Effects in Microelectronics

Single-Event Effects (SEE):

- Caused by the interaction of a single energetic particle
- SEE are determined by:
  - Charge generation
  - Charge collection
  - Circuit response
- Types:

Non-destructive:

- Single-event upsets (soft errors)
- Single-event transients
- Single-event functional interrupt
- Multiple-bit upsets

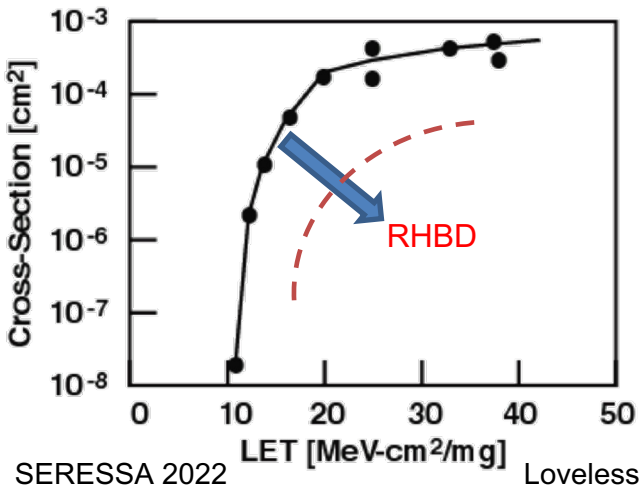
Destructive:

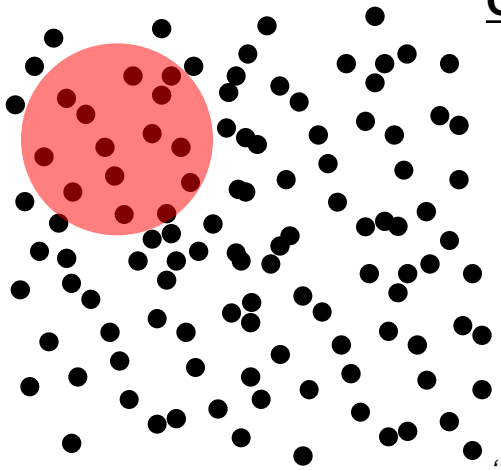
- Single-event latchup
- Single-event burnout
- Single-event gate rupture
- Single-event snap-back

Important Concepts:

Linear Energy Transfer (LET) & Cross-Section

Sensitive Area vs. LET





Calculation of Cross-Section

Known Arial Density of Shots (Ions)

Ex. 10 shots/cm²

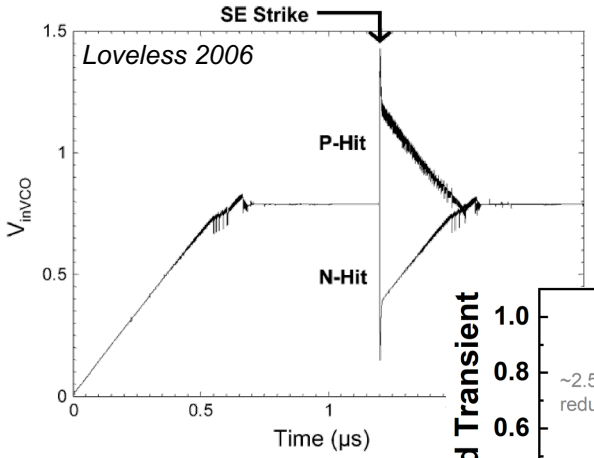
Number of shots that hit an **unknown** target

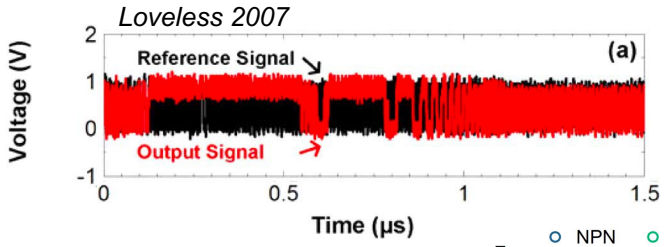
$$\text{Cross-section} = \frac{\text{14 shots/target}}{\text{10 shots/cm}^2} = \text{1.4 cm}^2\text{/target}$$

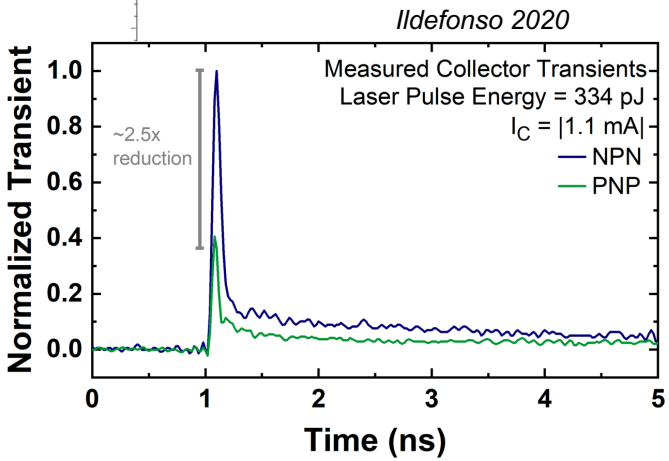
'Shotgun blast analogy' from C. C. Hafer, NSREC '09

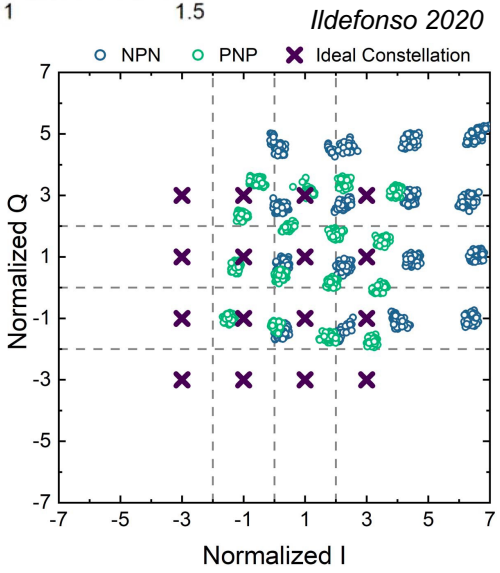
Single-Event Transients

- In digital electronics, an SET may lead to a single-event upset (SEU) – *alteration of memory cell state* – that can propagate through circuit
- In analog electronics, a single-event (SE) particle strike results in a single-event transient (SET)
  - *Competes with legitimate signals or perturbs functionality*
  - *Can result in a wide range of circuit responses*

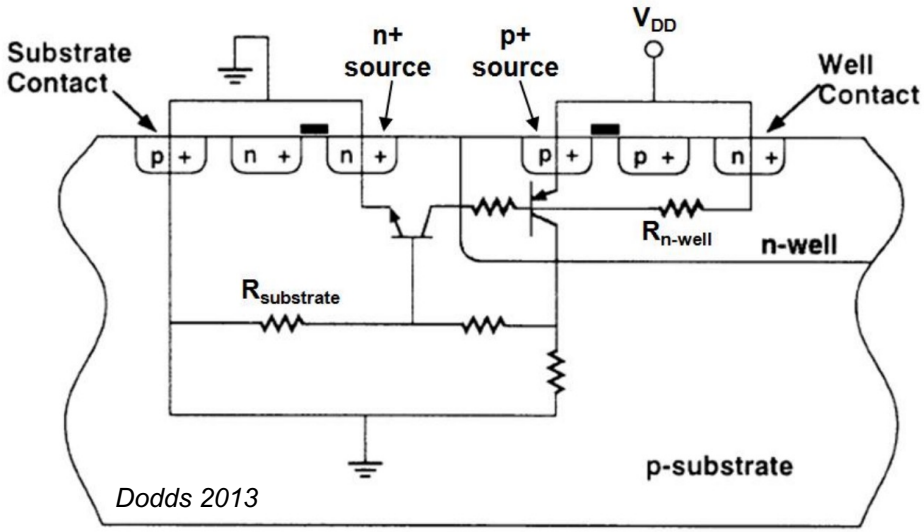




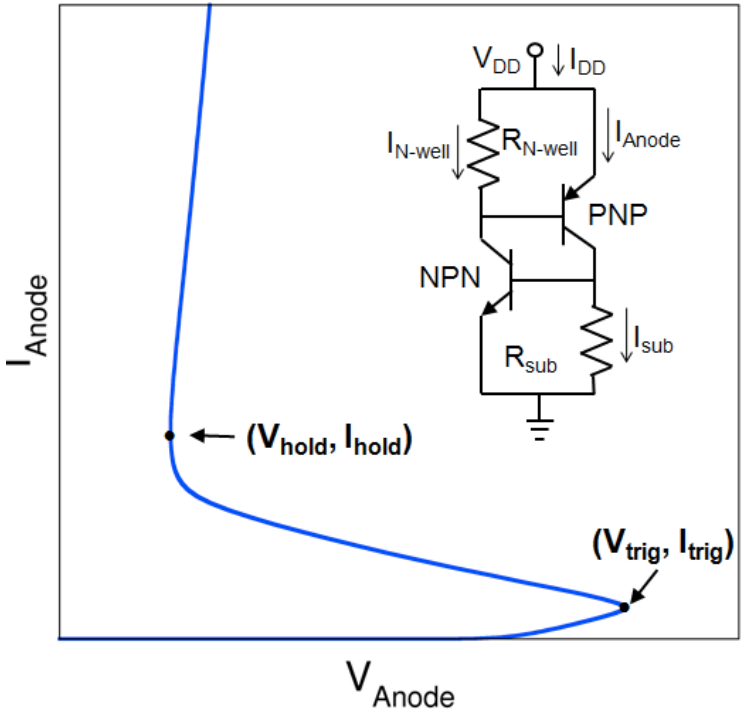




Single-Event Latchup

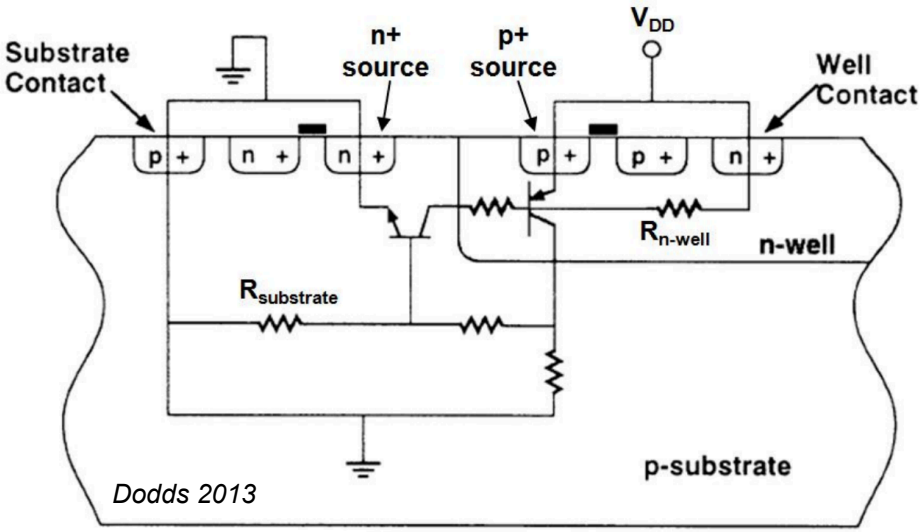


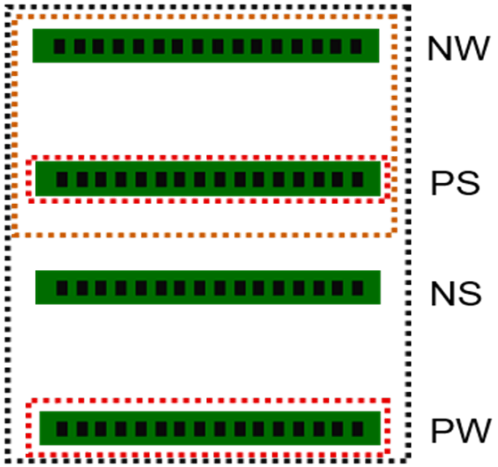
Cross-section of typical CMOS technology showing parasitic thyristor that can be triggered into low impedance state



- Latchup occurs when parasitic *p-n-p-n* regions (*composed of cross-coupled p-n-p and n-p-n BJTs*) are activated by an energetic ionizing particle
- The collector of each BJT is connected to the base of the other, creating a positive feedback loop
- Latchup can occur when:
  - *both BJTs conduct, creating a low-resistance path between V_{DD} and V_{SS}*
  - *the product of the gains in the BJTs in the feedback loop is greater than 1*

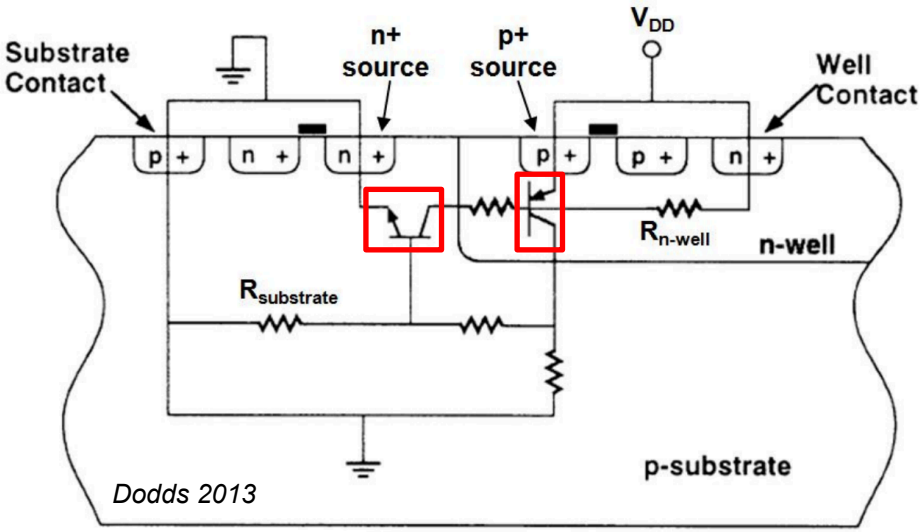
Single-Event Latchup Mitigation

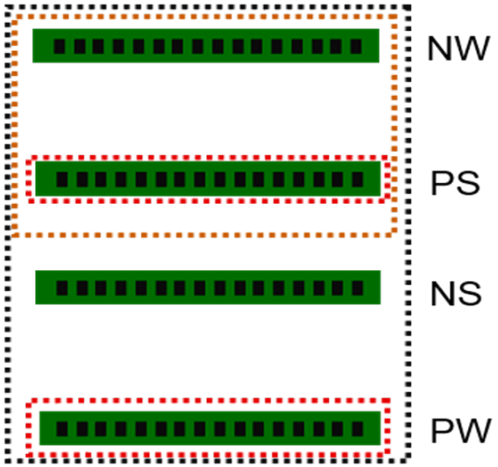




- Sensitivity depends on parasitic bipolar gains and well/substrate resistances
- Mitigation of SEL involves

Single-Event Latchup Mitigation





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  - *1) reduction of BJT gain*

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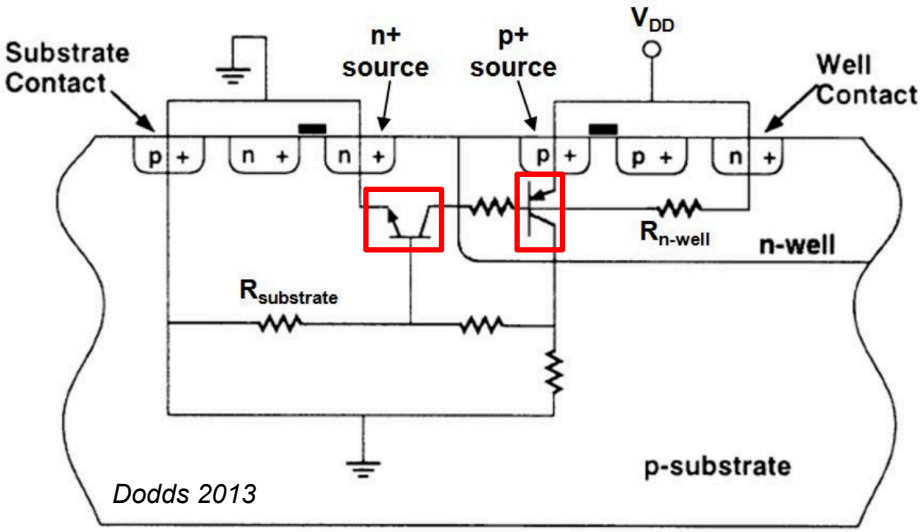

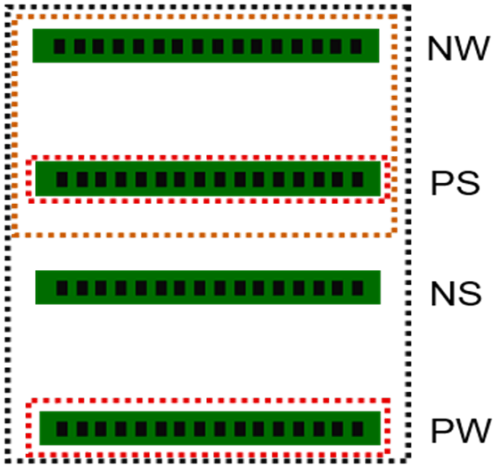

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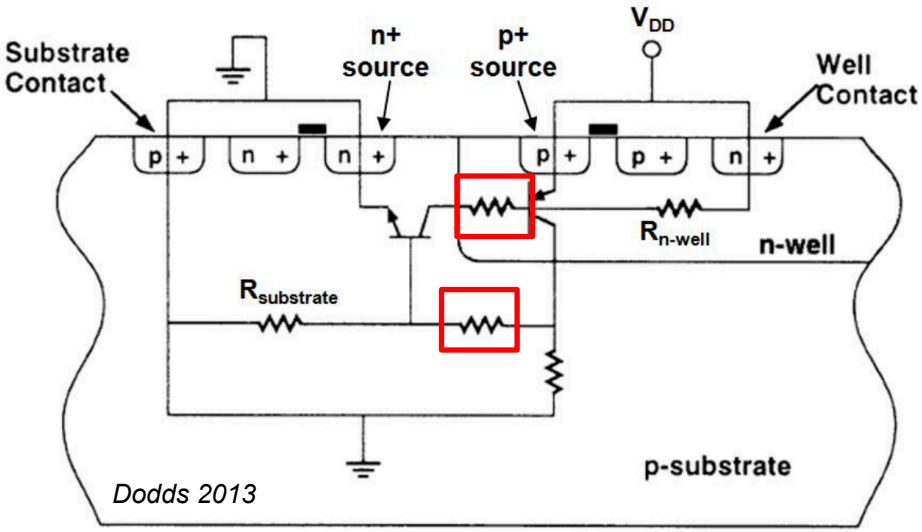
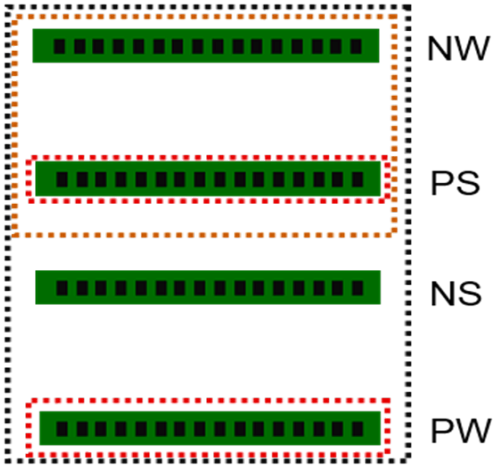
Process engineering: channel doping, silicide proximity, strain

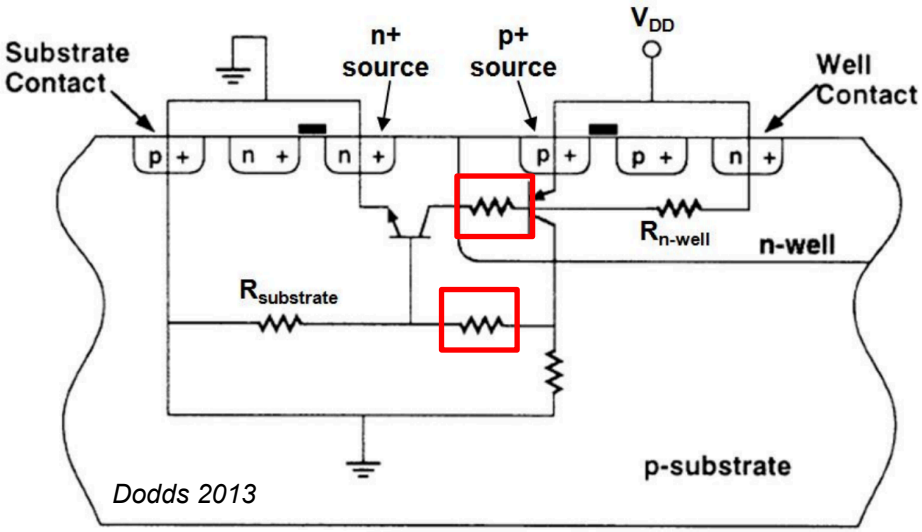
Single-Event Latchup Mitigation

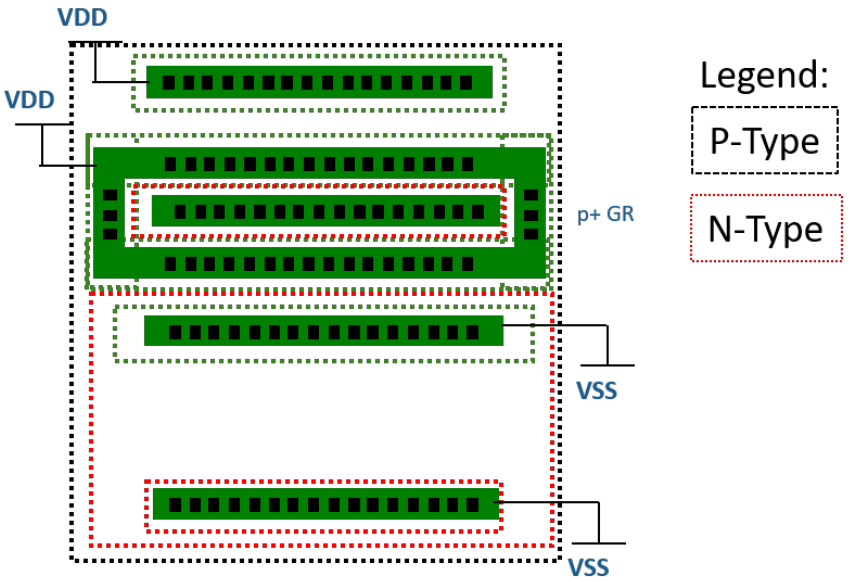




- Sensitivity depends on parasitic bipolar gains and well/substrate resistances
- Mitigation of SEL involves
  - *1) reduction of BJT gain*
  - *2) decoupling BJTs or increasing the coupling resistance*

Single-Event Latchup Mitigation





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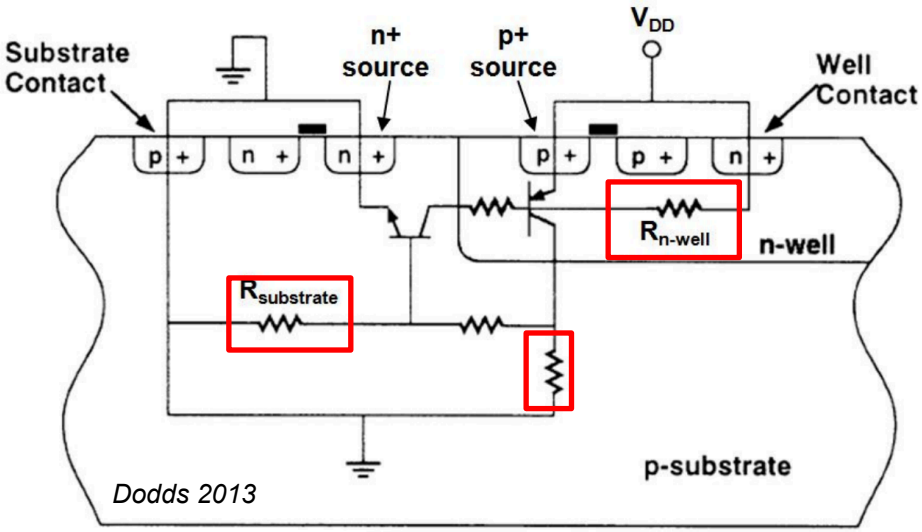
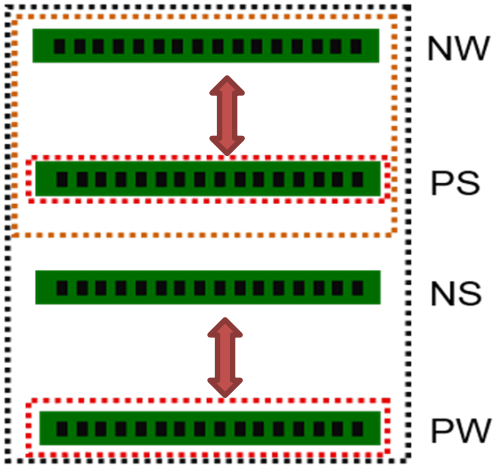
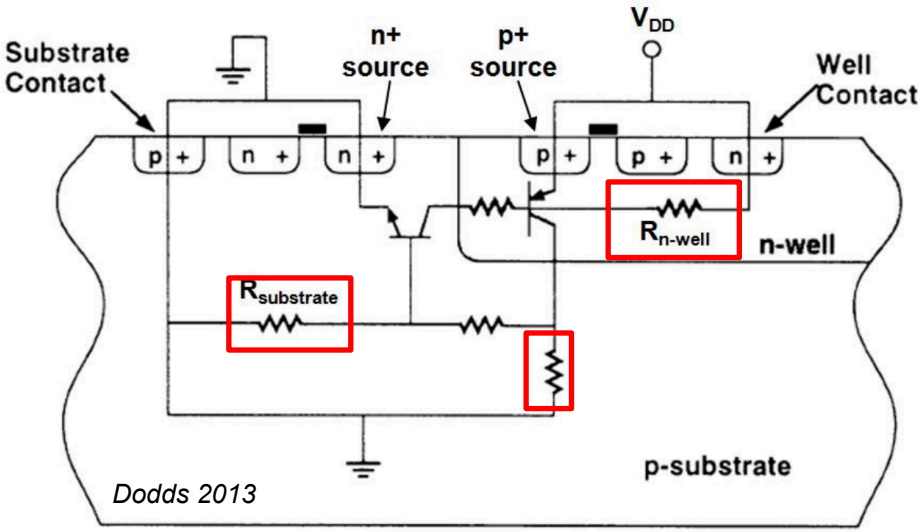
Single-Event Latchup Mitigation

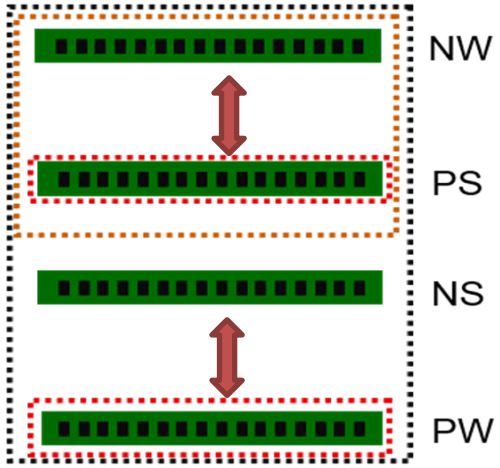




- Sensitivity depends on parasitic bipolar gains and well/substrate resistances
- Mitigation of SEL involves
  - *1) reduction of BJT gain*
  - *2) decoupling BJTs or increasing the coupling resistance*
  - *3) decreasing resistances from the BJTs to well and substrate contacts*

Single-Event Latchup Mitigation





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  - *1) reduction of BJT gain*
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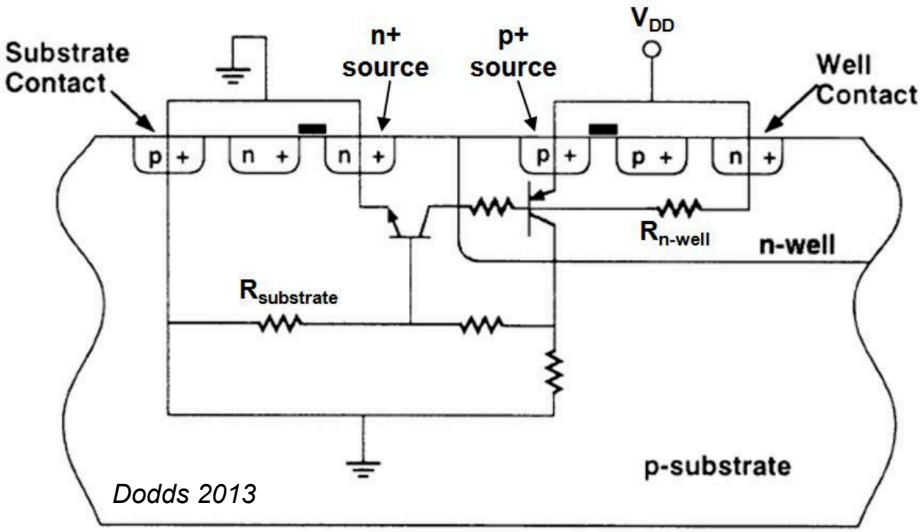
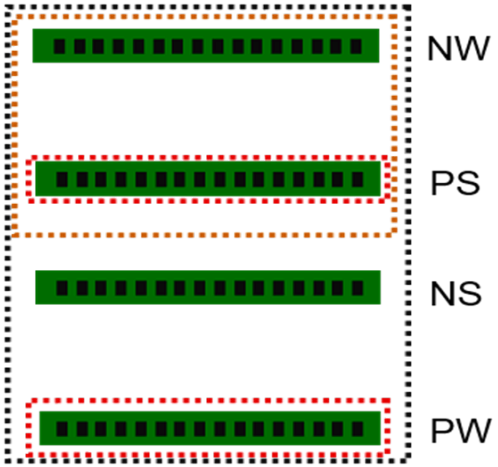
  - *3) decreasing resistances from the BJTs to well and substrate contacts*

Decrease source-to-well spacing
Increase contact density

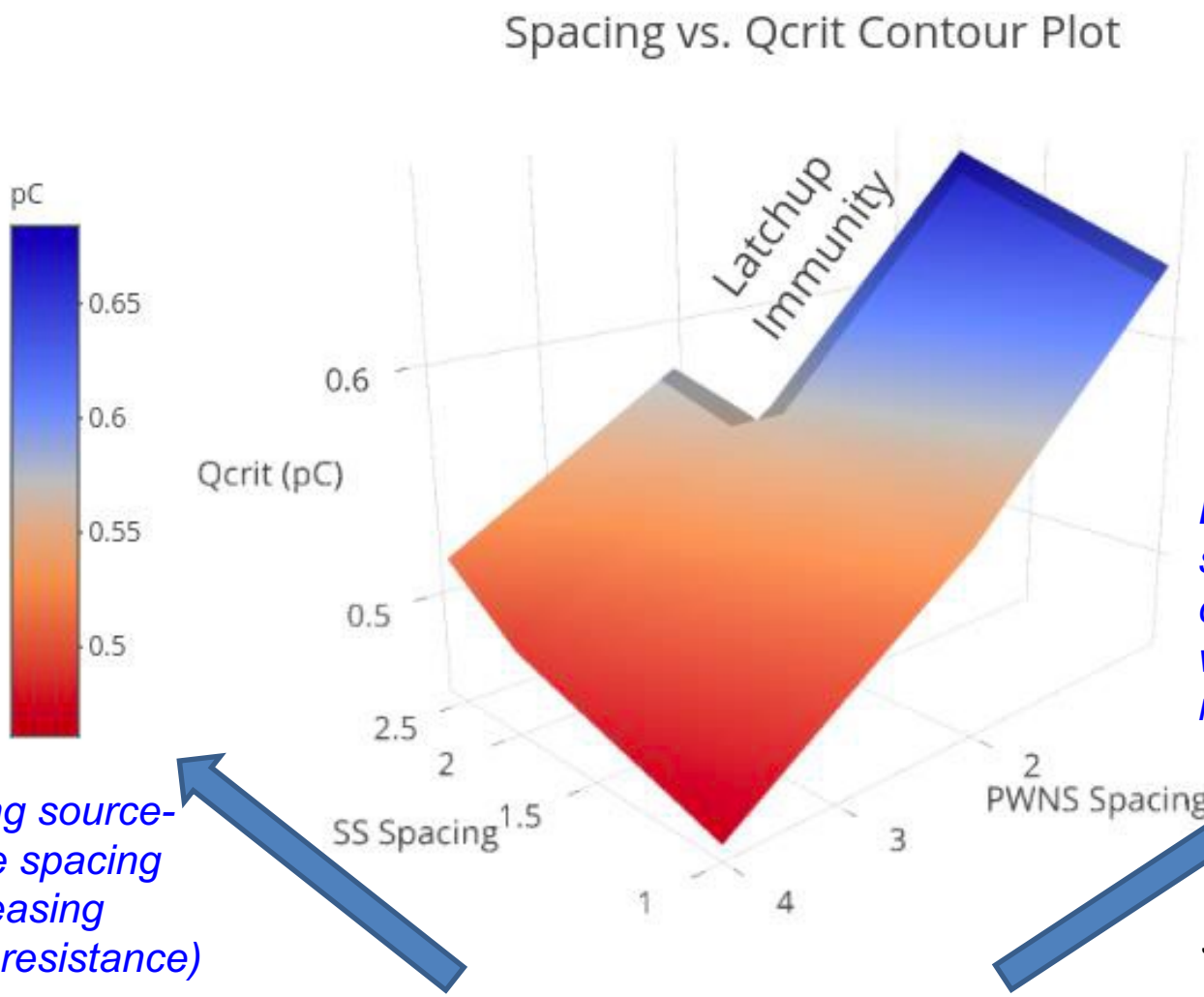
Single-Event Latchup Mitigation





- Sensitivity depends on parasitic bipolar gains and well/substrate resistances
- Mitigation of SEL involves
  - *1) reduction of BJT gain*
  - *2) decoupling BJTs or increasing the coupling resistance*
  - *3) decreasing resistances from the BJTs to well and substrate contacts*
- Geometry, density, and spacing of wells, sources, source-to-well contacts, and source-to-source contacts have large impact on overall vulnerability

Single-Event Latchup Mitigation



Increasing source-to-source spacing (i.e. increasing coupling resistance)

Decreasing well-to-source spacing (i.e., decreased well/substrate resistance)

Joplin 2018

Summary of SEE Mitigation Techniques

- SEE mitigation involves one or both of the following, irrespective of the technology:
  - ***reducing*** *the amount of* ***collected charge (Q_{col})*** *at a metallurgical junction:*
    - layout alternatives such as guard rings, drains, or diodes (MOS)
    - n-rings, substrate-tap rings, and nested minority-carrier guard rings (BJT)
    - substrate engineering: charge blocking layers in the substrate, use of very thin epitaxial silicon layer, silicon-on-insulator (SOI)
    - addition of dummy collector for charge collection in HBT devices
    - increased substrate and well contacts (reduced substrate and well impedances)

Hardening-by-process (technology modifications)

Hardening-by-design (layout modifications)

Summary of SEE Mitigation Techniques

- SEE mitigation involves one or both of the following, irrespective of the technology:
  - ***reducing*** *the amount of* ***collected charge*** *(Q_{col}) at a metallurgical junction:*
  - ***increasing*** *the* ***critical charge*** *(Q_{crit}) required to generate an SET*

    conventional, perhaps "brute force" methodology include:
    - increasing the transistor sizes (buffering)
    - increasing the drive currents
    - increasing the supply voltage
    - increasing capacitor sizes

Hardening-by-design
(layout, circuit, and/or system modifications

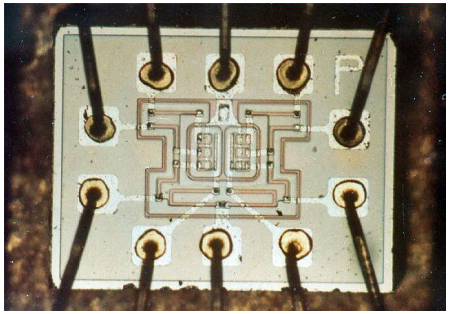
Hardening Techniques for AMS Circuits

- Radiation Effects in AMS Circuits: Unique issues and considerations
- Total Ionizing Dose and Basic Mitigation Strategies
- Single Event Effects and Basic Mitigation Strategies
- Hardening by Design for AMS
- A look to the future
- Summary

Radiation Hardening by Design

The Big Picture

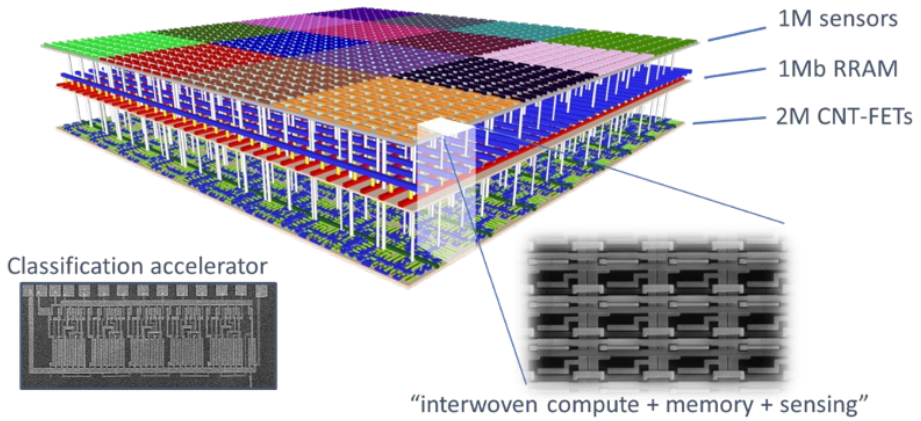
- State-of-the-art chip systems contain billions of transistors, integrated analog and digital, 3D IC stacks, and multiple voltage domains
- Critical charge can be just a few fC



Logical NOR IC from Apollo (~1961)

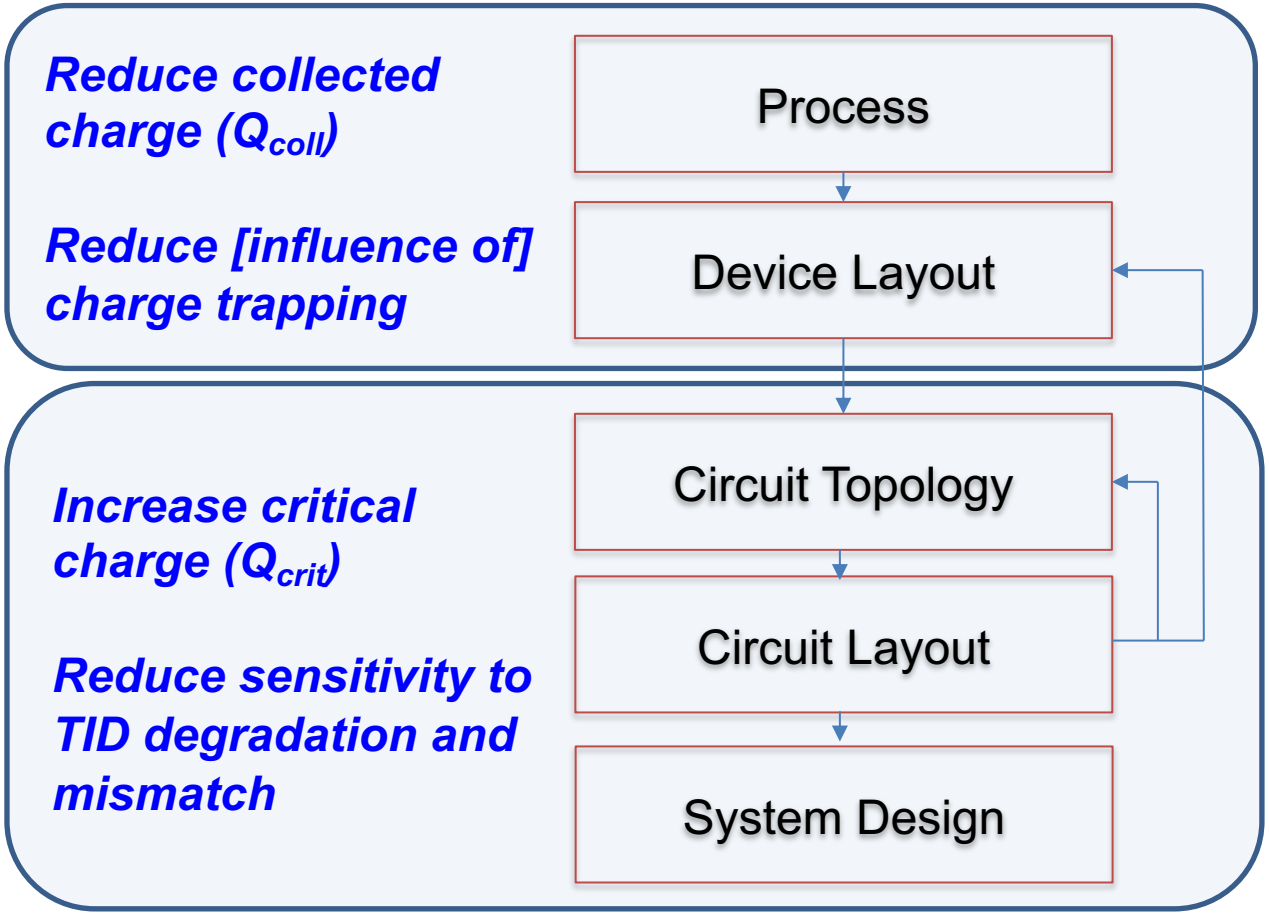
Challenges for RHBD

- Integration of process, layout, topology, and system-level approaches
- Architecture-level SE simulation and high-level RHBD approaches
- SEE for low-power circuits
- Development and analysis of RHBD libraries
- Effects of charge-sharing
- Integrated modeling, simulation and experimental analysis methodologies for advanced technology ICs

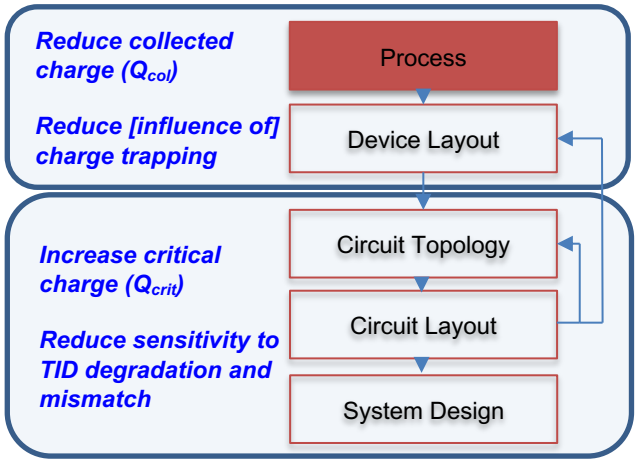


3D-SoC sensor/machine learning IC from Stanford (2017)

Basic RHBD for AMS



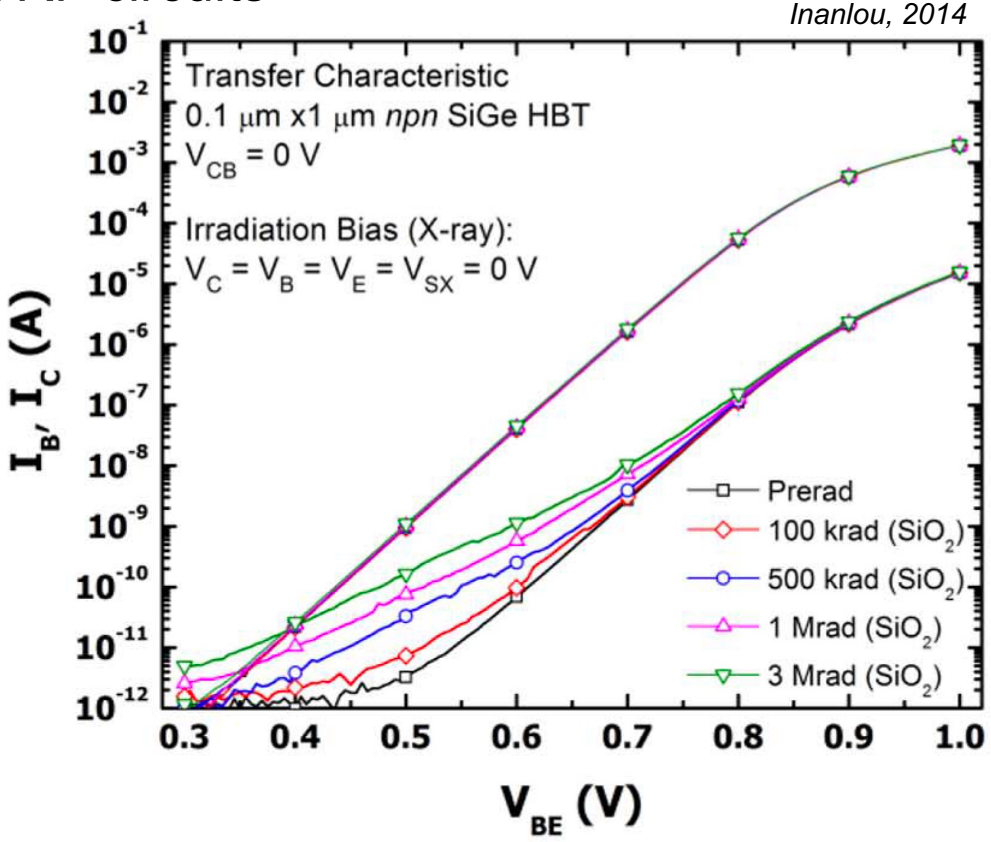
Basic RHBD for AMS: By Process



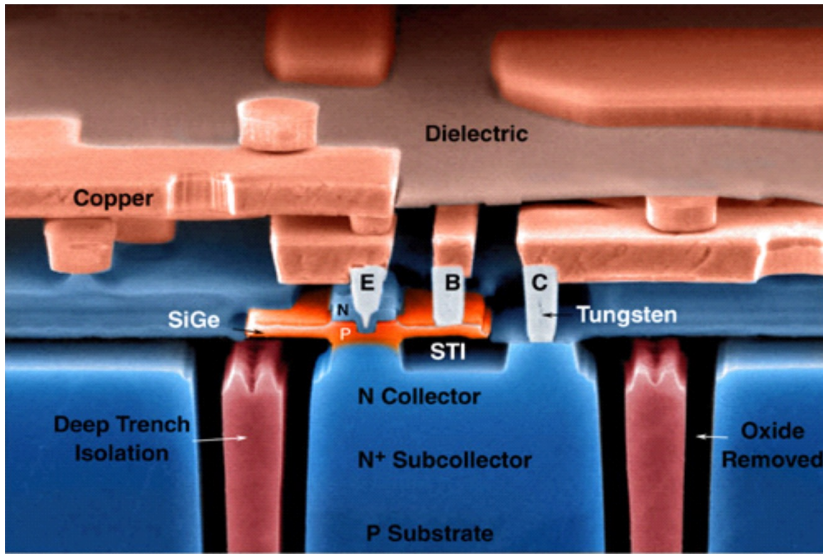
By-Process example:

Strained-enhanced SiGe HBTs (graded Ge layer in the base of a Si transistor) have emerged as an excellent alternative for TID-robust RF circuits

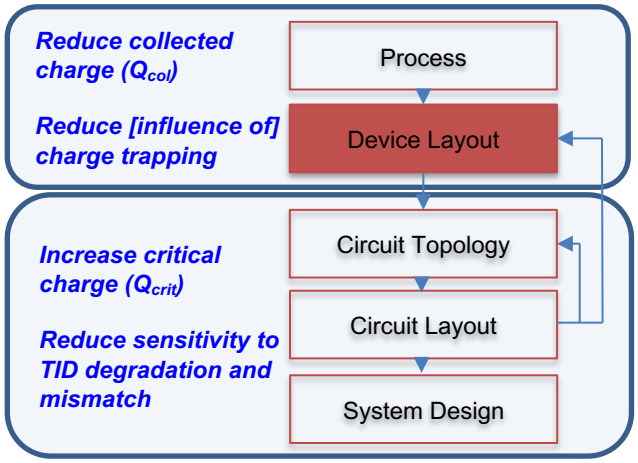
Inanlou, 2014



Cressler, 2009



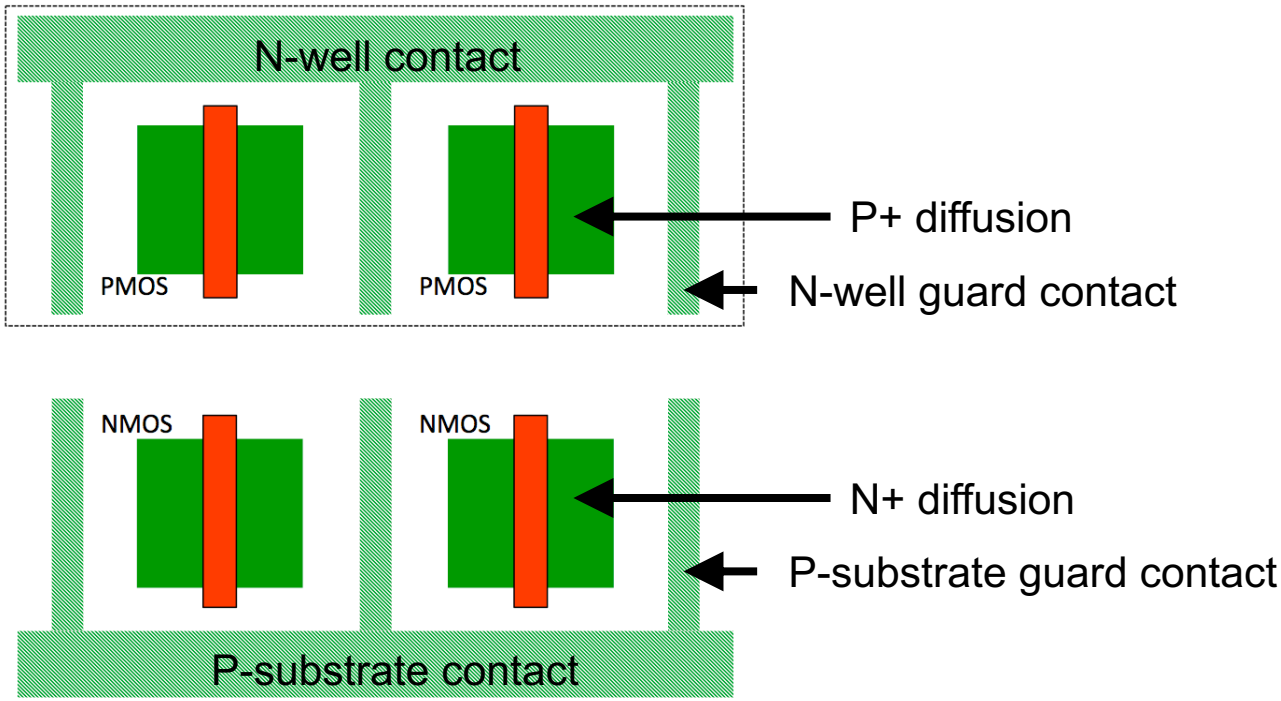
Basic RHBD for AMS: By [Layout] Design



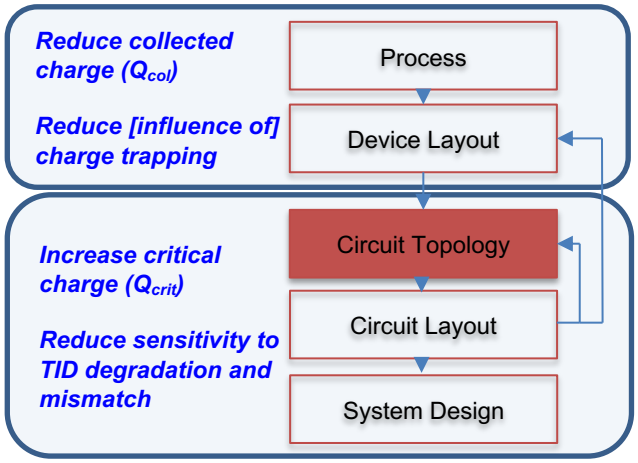
By-Design (Device Layout) example:

Guard contacts, formed from N-well and P-substrate diffusion contacts limit the charge collection at the circuit diffusions

Black, 2005



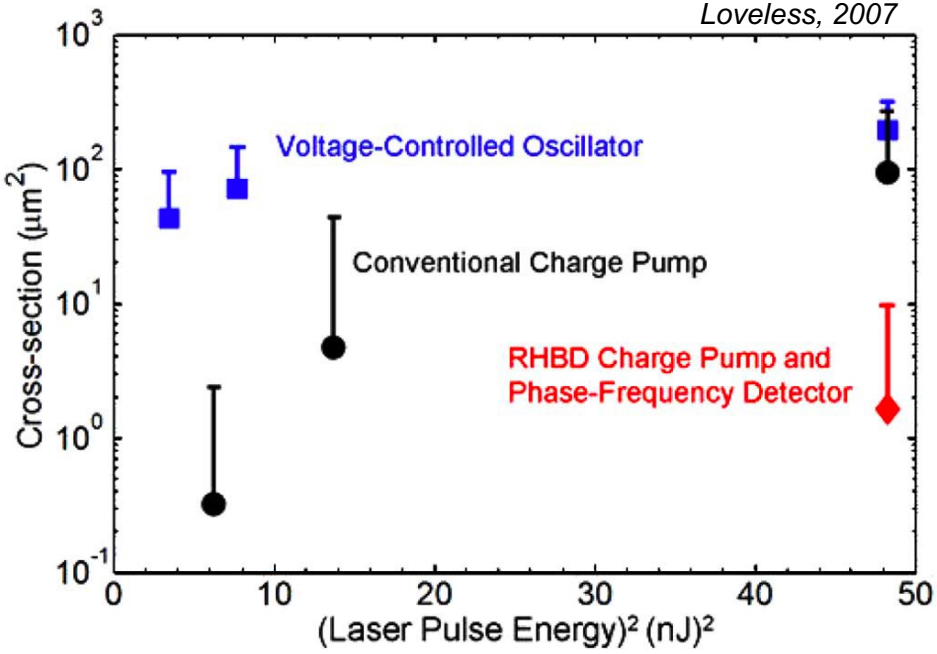
Basic RHBD for AMS: By [Circuit] Design



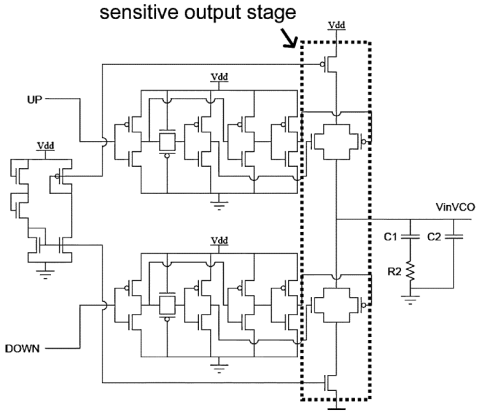
By-Design (Circuit) example:

Small changes to the circuit topology can lead to large gains in SEE performance

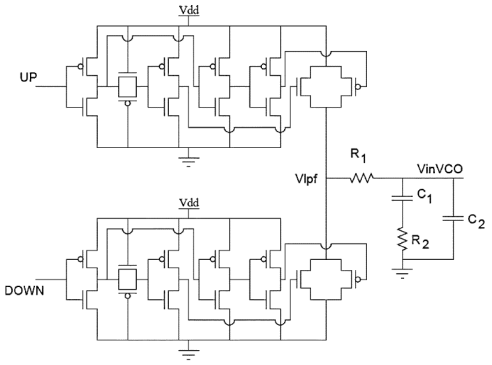
Loveless, 2007



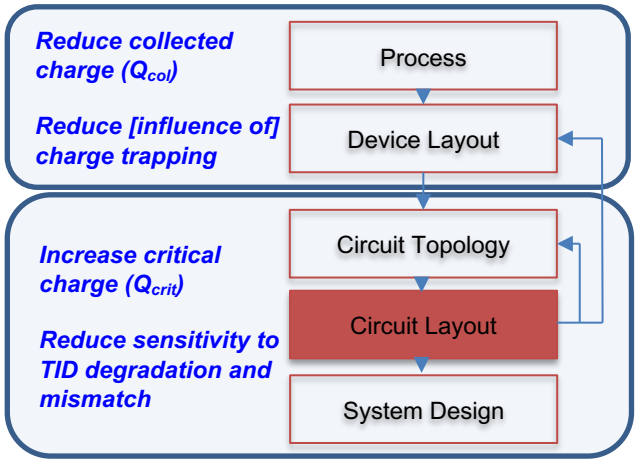
Unhardened Charge Pump (130 nm)

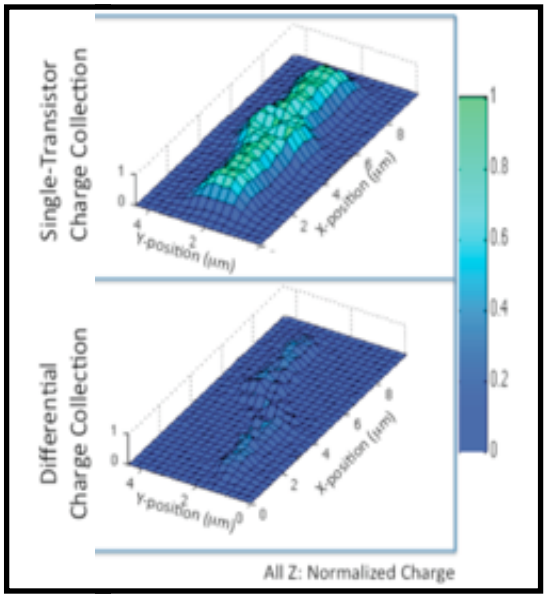


RHBD Charge Pump (130 nm)



Basic RHBD for AMS: By [Layout] Design

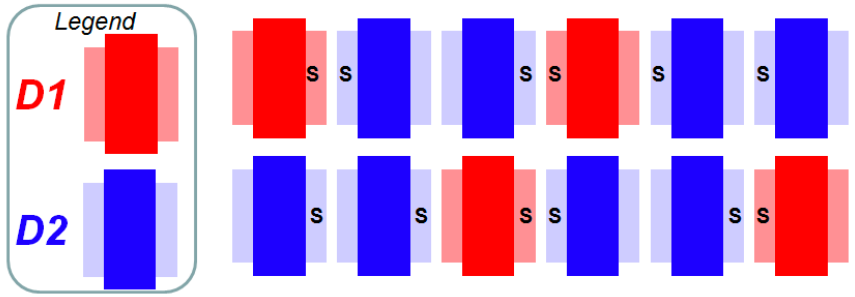




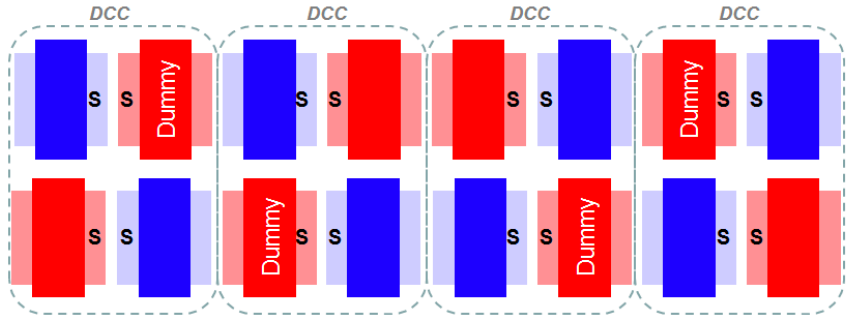
Armstrong, 2010

By-Design (Circuit Layout) example:

(a) Baseline quadrant layout of D1 and D2

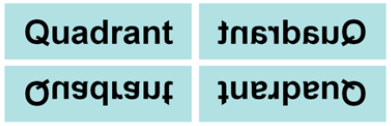


(b) DCC quadrant layout of D1 and D2

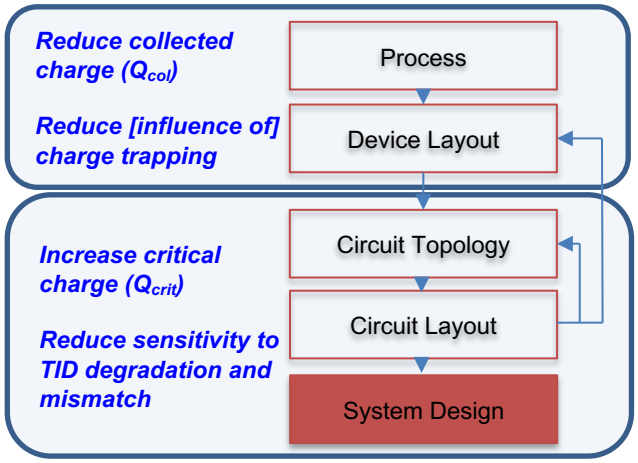


Atkinson, 2013

(c) Common-centroid layout of quadrants



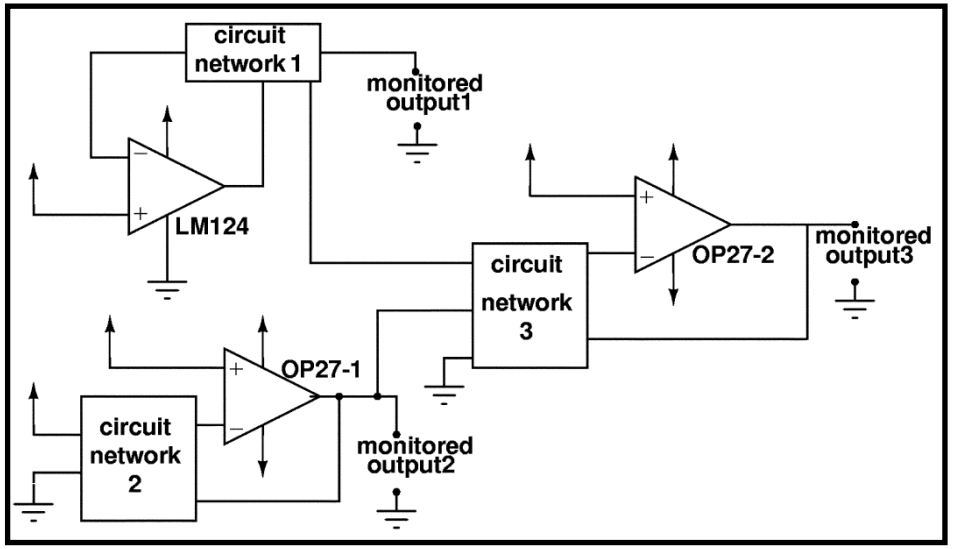
Basic RHBD for AMS: By [System] Design



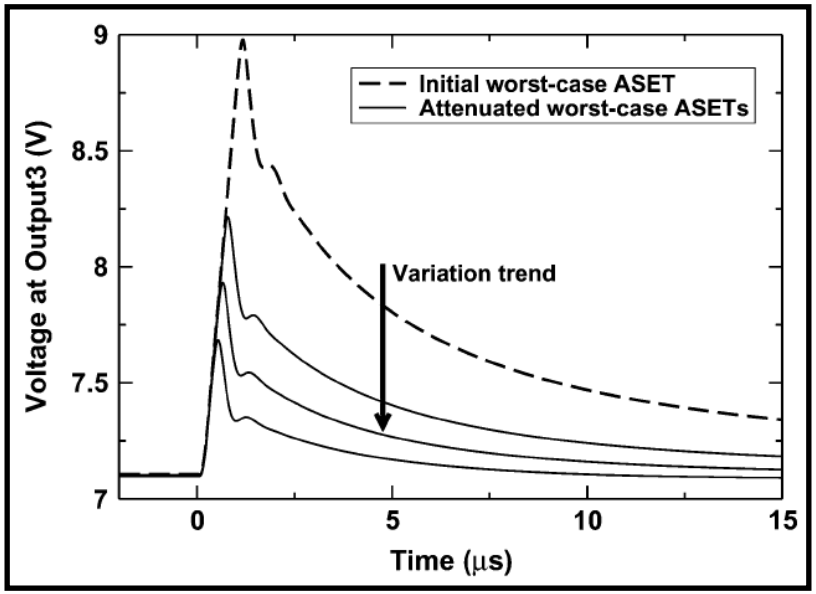
By-Design (System) example:

Low-pass filtering at system-level can effectively reduce SETs

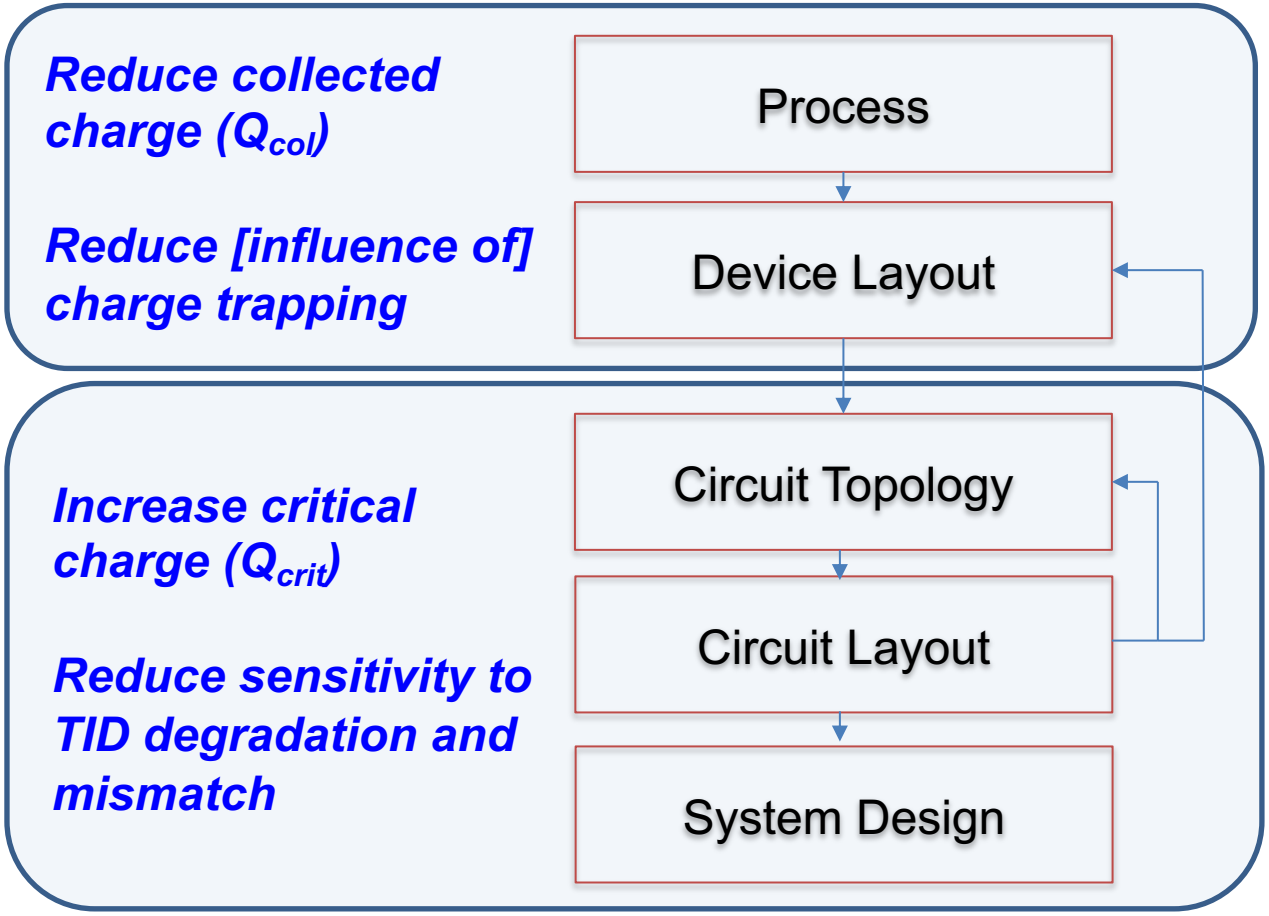
Boulghassoul, 2004



Block Diagram of Satellite Power Distribution Controller/Monitor

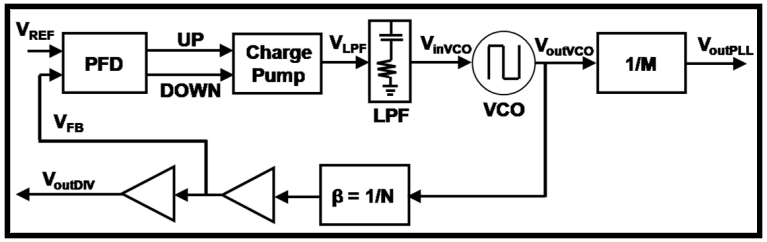


Ok, lets start to pull it all together



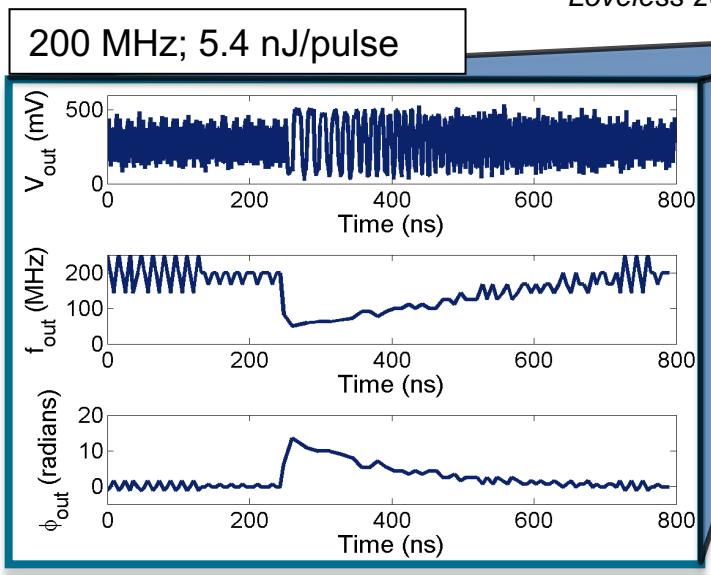
Targeted Laser Excitation

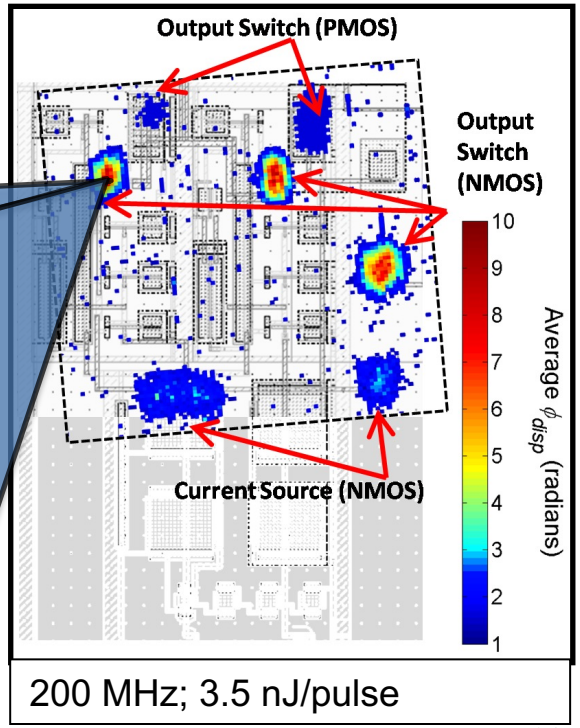
- PLL used as an example to illustrate complex inter-dependencies
- Laser SET mapping performed on charge pump sub-circuit (most sensitive block)
  - *output signals following 10 strikes per x-y location were recorded*
  - *frequency/phase transients extracted from transient output*



Two-Photon Absorption Laser-Induced SET Map of PLL Sub-Circuit (Charge Pump)

Loveless 2010



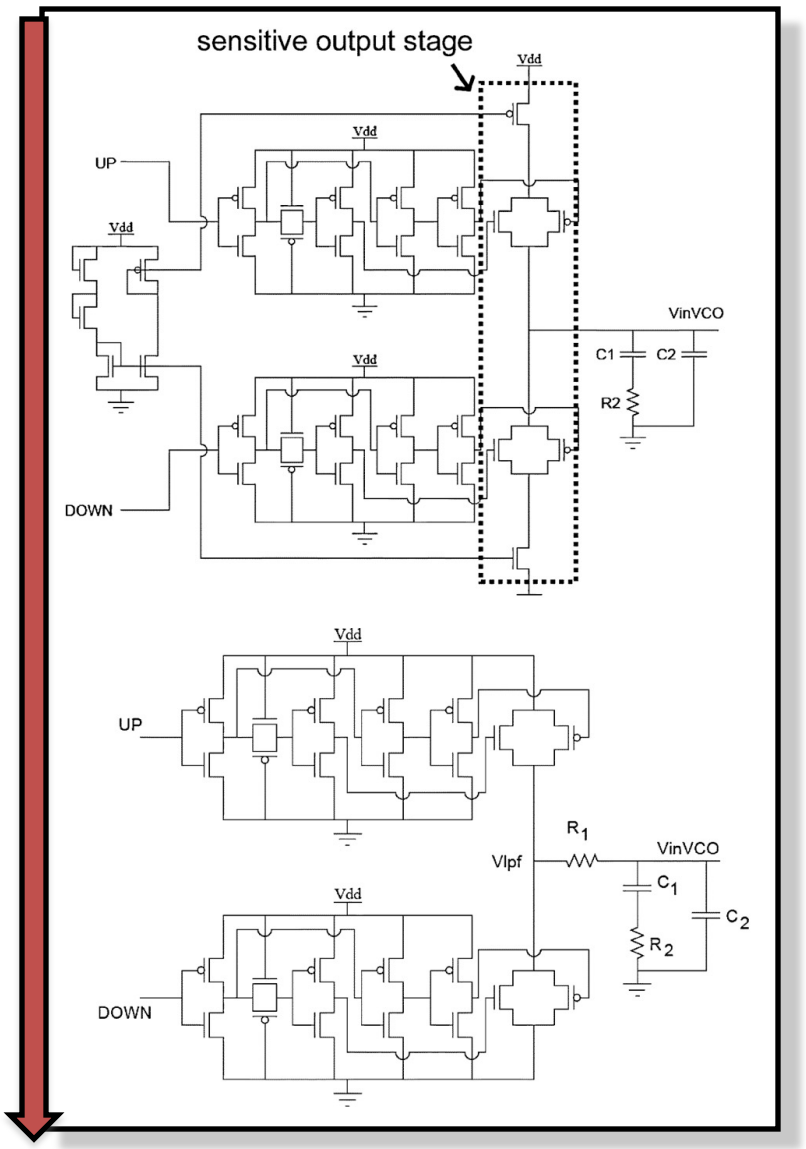


Now we know the issues, start with … ?

- **Resistive Decoupling**
  - *effectively increases the time constant seen by the two storage nodes and limit the maximum change in voltage during a single-event, thus increasing Q_{crit}*
- **Filtering**
  - *high-frequency transients may be filtered by decoupling nodes sensitive to ASETs and introducing a time constant through a series resistor or low-pass filter*
- **Increased Capacitance**
  - *increases the amount of charge, Q_{crit}, required to generate an ASET*

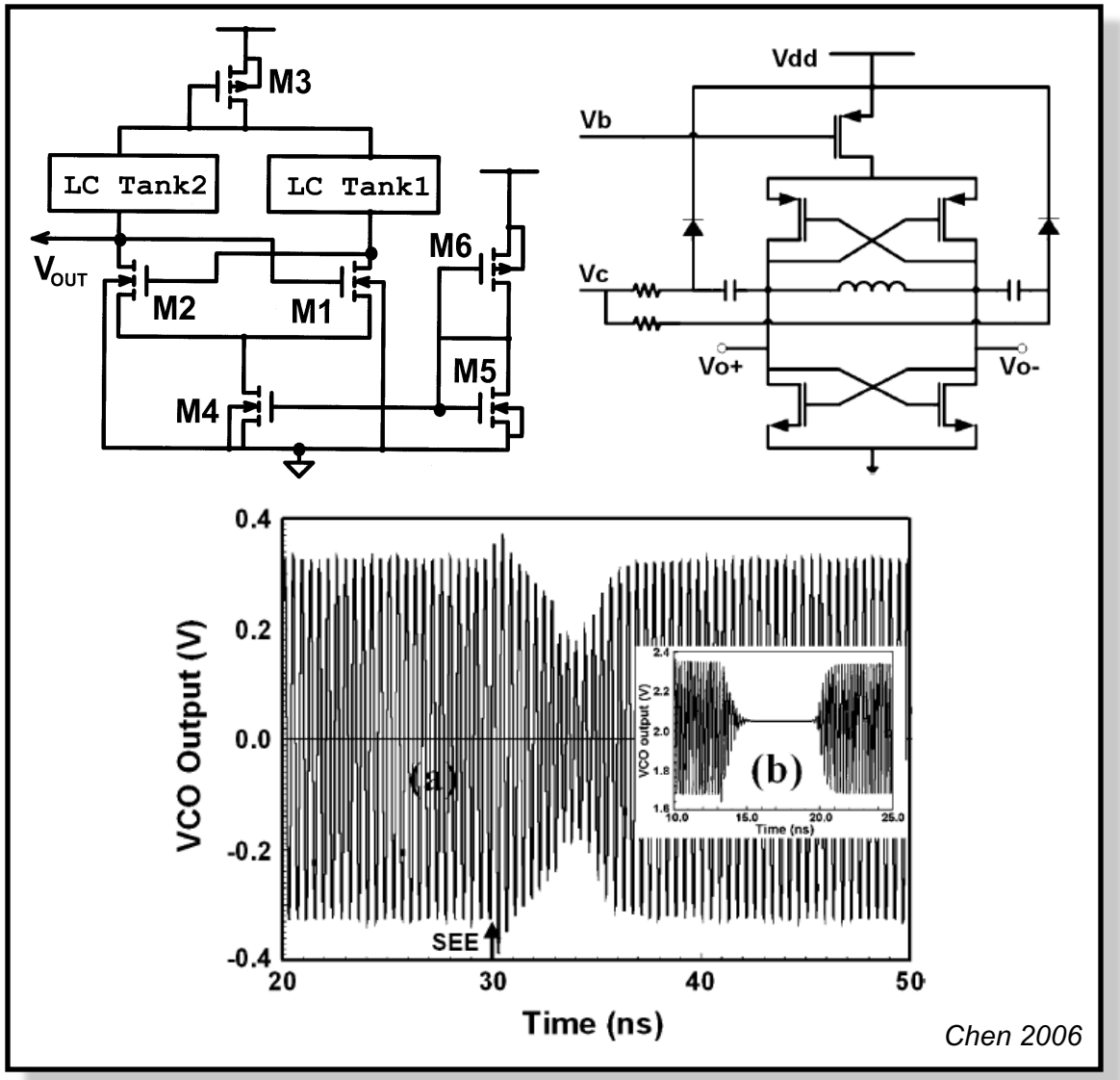
Single-Event Hardening of Charge Pump Sub-Block of PLL

Loveless 2006



High Impedance Nodes

- **Reduction of High Impedance Nodes**
  - *high impedance nodes have consistently been identified as the culprits!*
  - *can be reduced or eliminated at the circuit- or transistor-levels*

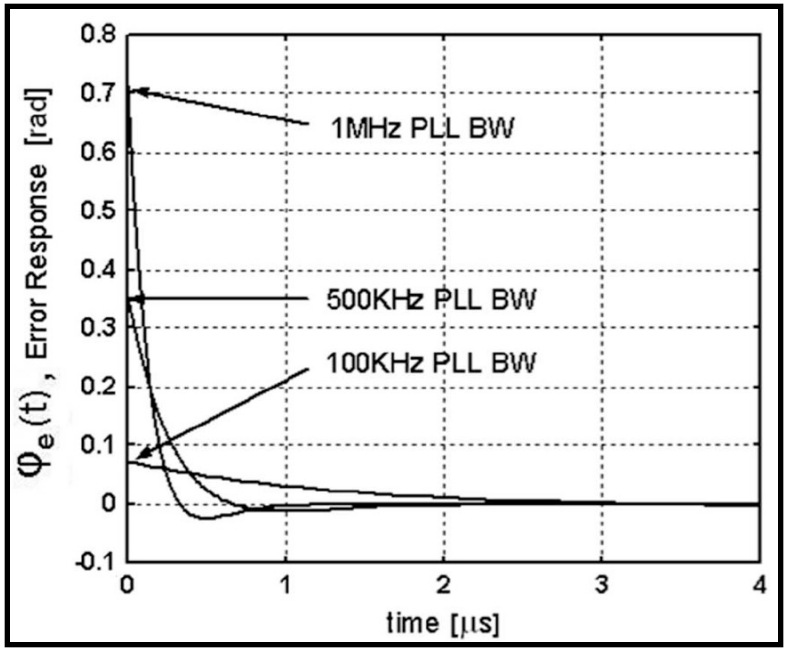


Chen 2006

Single Event Mitigation By Elimination of High-Impedance Nodes in an LC Tank Oscillator

Gain-Bandwidth Tradeoffs

- **Modifications in Bandwidth and Gain**
  - *in general, many works on amplifiers, phase-locked loops, voltage-controlled oscillators, … have shown that **reduction in bandwidth** results in **reduction in SE vulnerability***



Chung 2006

Error Response versus Time During a Single Event in the PLL at Various Bandwidths

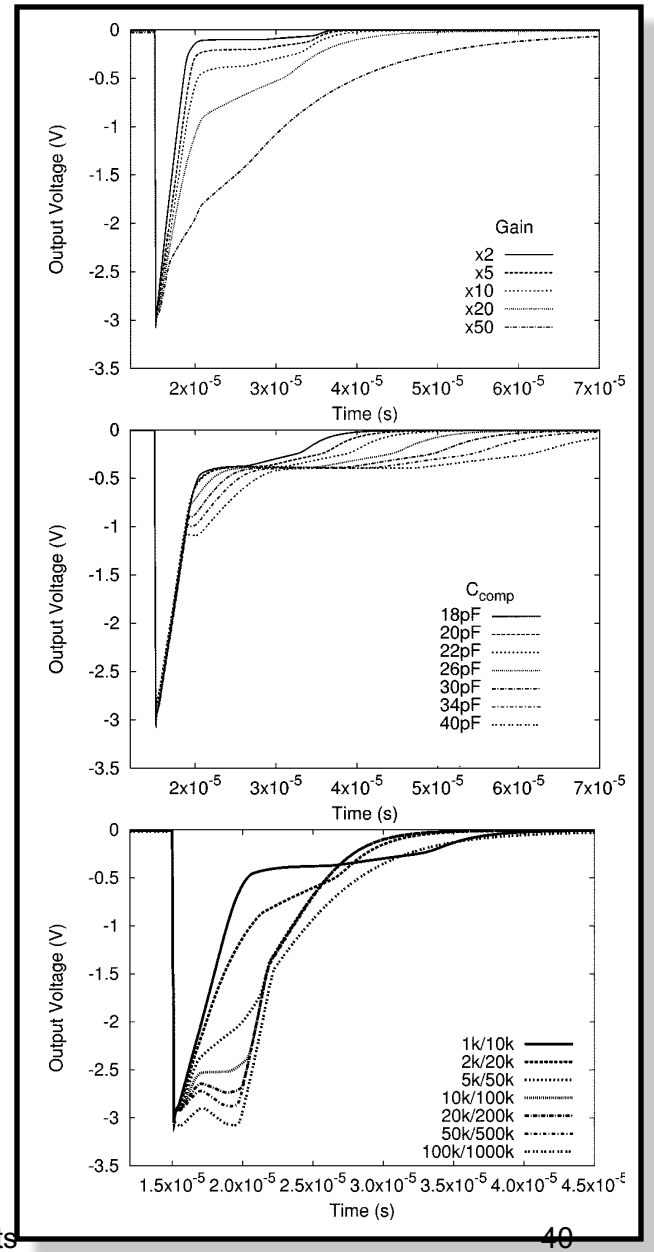
Gain-Bandwidth Tradeoffs

- **Modifications in Bandwidth and Gain**
  - *in general, many works on amplifiers, phase-locked loops, voltage-controlled oscillators, … have shown that **reduction in bandwidth** results in **reduction in SE vulnerability***
  - *gain and operating speed also play a particular role in determining the SET response*

Ex. "Faster operational amplifier with a smaller gain will have a better SET response than a slower operational amplifier run at a high gain. It also seems to be best to use the smallest practical values to set the closed-loop gain of the amplifier", *Sternberg*

Boulghassoul 2004

SET Dependence on Gain, Capacitance, and Resistance Values in Various Stages in an LM124 Op-Amp



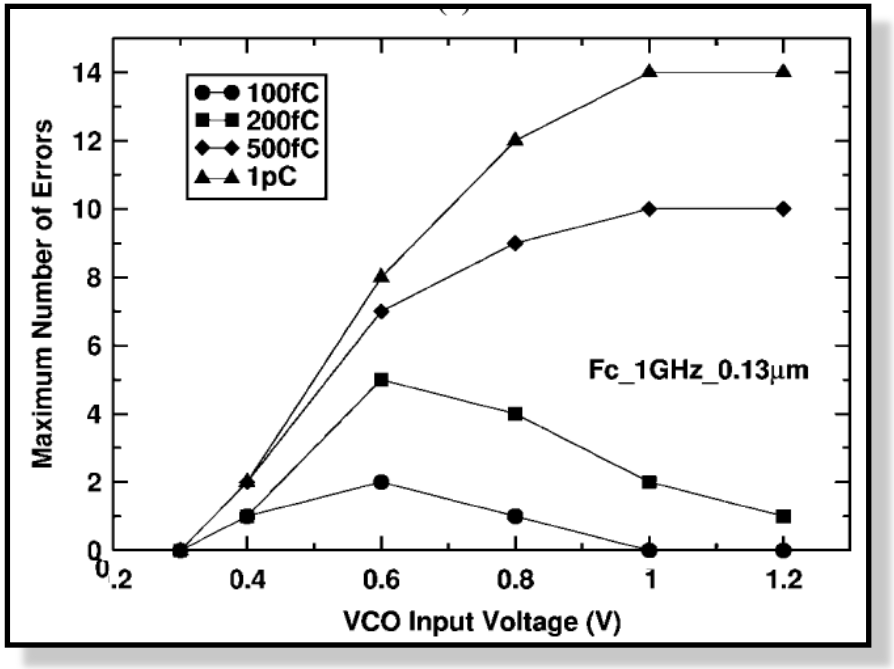
Gain-Bandwidth Tradeoffs

- **Modifications in Operating Speed and Current Drive**
  - *analog circuits have been shown to exhibit reduced ASET vulnerability for increased operating frequency*

Contrary to that seen in digital circuits

  - *increased speed is often accompanied by increased drive current and an improved ability to dissipate the deposited energy, making the circuit less vulnerable*
  - ***important to attribute the improvement to either speed or drive strength*** *(increased bias current is a well-known technique and is often used in AMS circuits for improved SET performance)*

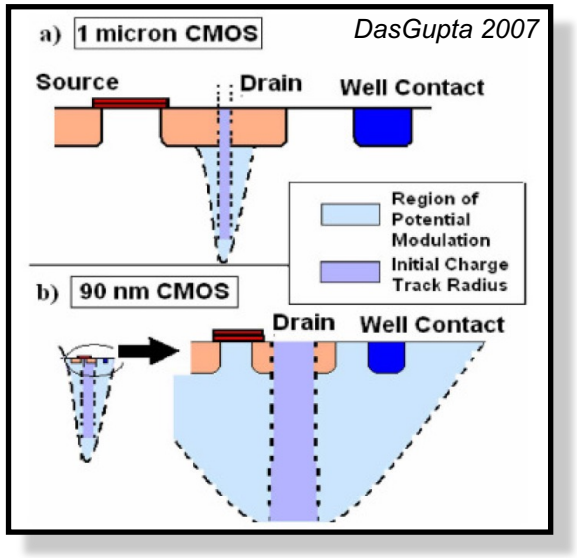
Boulghassoul 2005

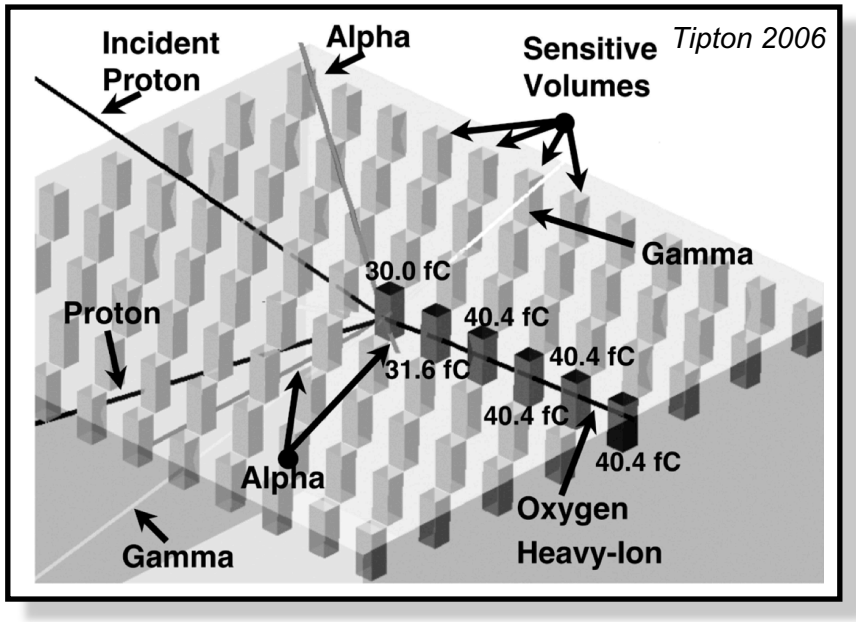


Number of Errors in VCO Output Bits Versus Input Voltage (Proportional to Drive Strength and Frequency)

Circuit Layout-Aware Mitigation

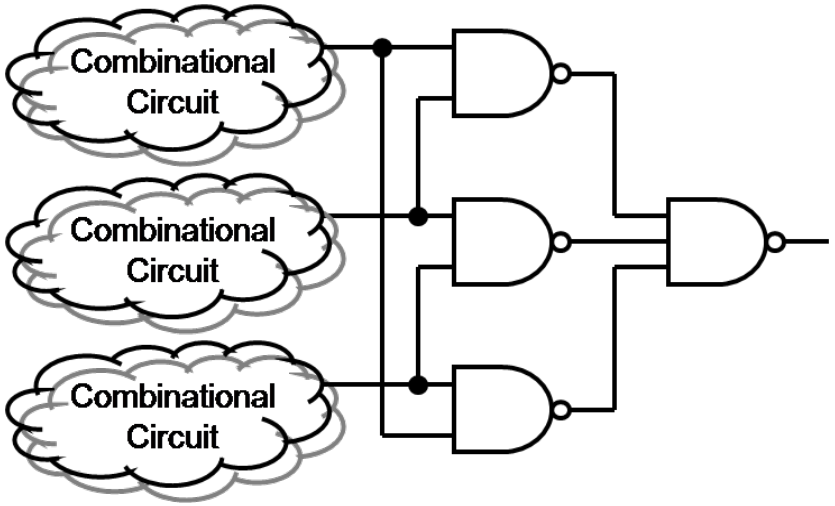
- In recent years, “charge sharing” between transistors has become commonplace:
  - *decreased spacing of devices with technology scaling can increase the charge collection at nodes other than the primary struck node*
  - *layout-level mitigation is becoming increasingly important for ensuring radiation hardness*





Charge Sharing Reliability Issues

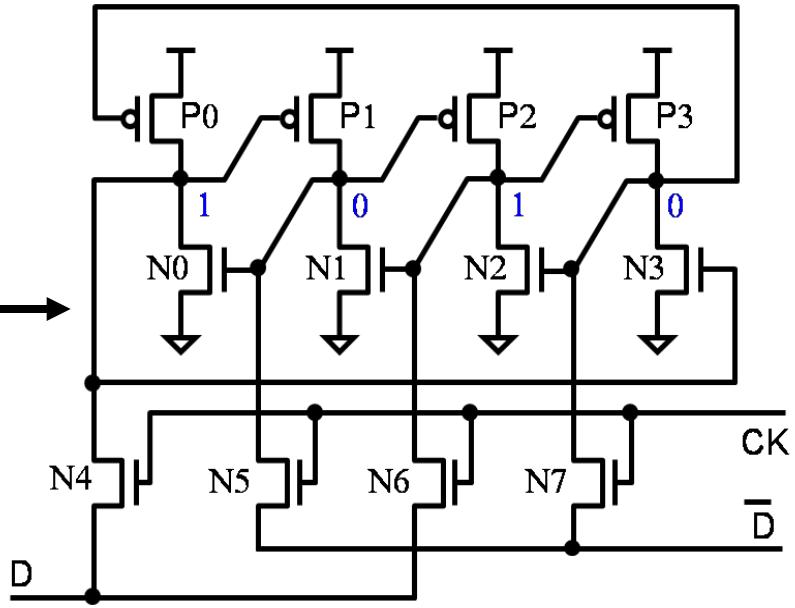
Charge sharing can render redundancy-based methods (e.g., Triple Modular Redundancy - TMR and Dual Interlocked Storage Cell - DICE latch) for SEU mitigation less effective



Triple Modular Redundancy *Peterson 1980*

DICE latch circuit

Calin 1996

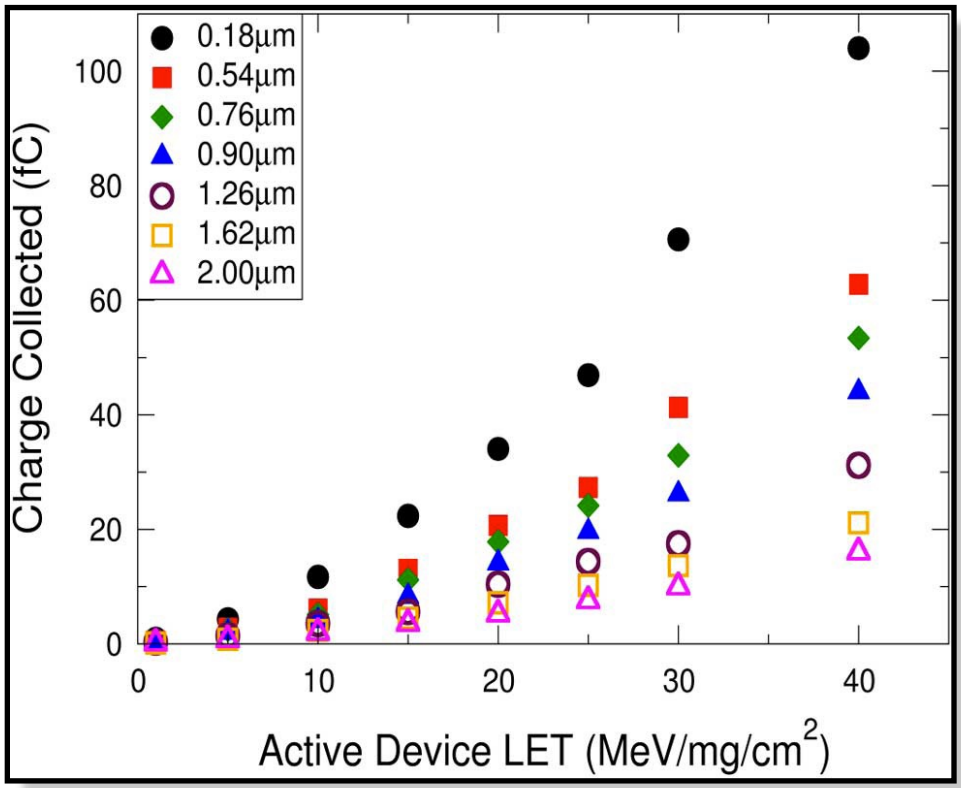


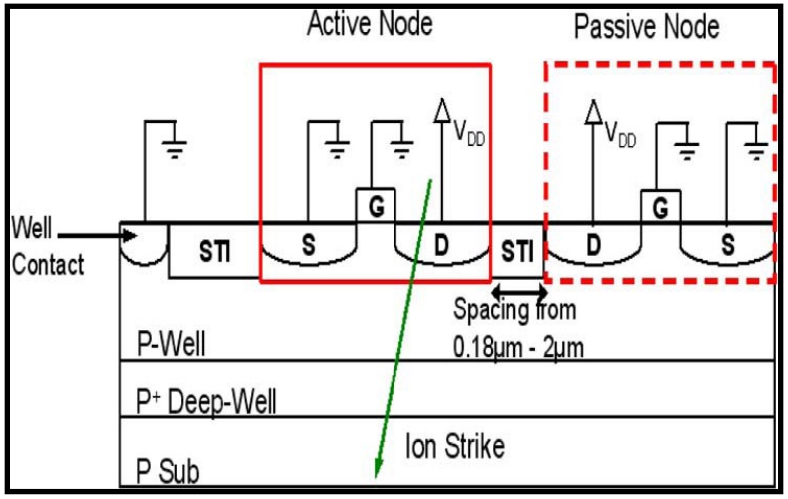
Layout-Level Mitigation: *Nodal Separation*

Nodal separation:

- *increasing the distance between devices can reduce the amount of charge collected on "passive" devices*

Amusan 2006





NMOS Cross Section Showing Active (Device Struck by Ionizing Particle) and Passive (Device that Indirectly Collects Charge) Device

Large Spacing Required To Mitigate Entirely

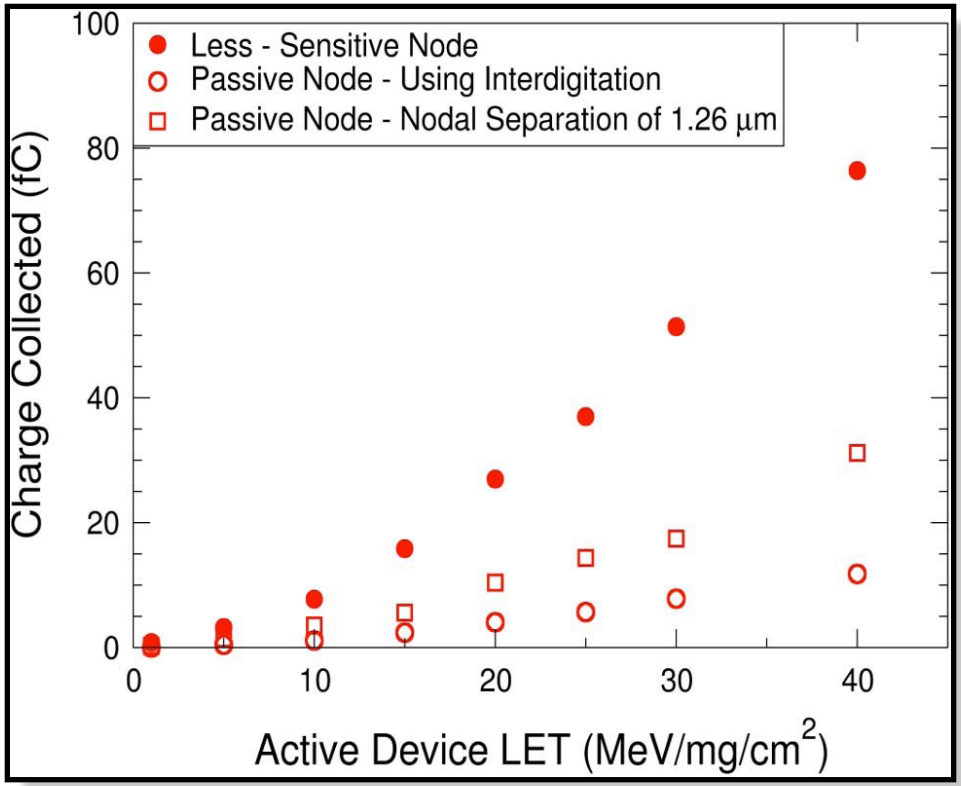
Nodal Separation of Two PMOS Devices (130 nm CMOS): Charge Collected on Passive Device

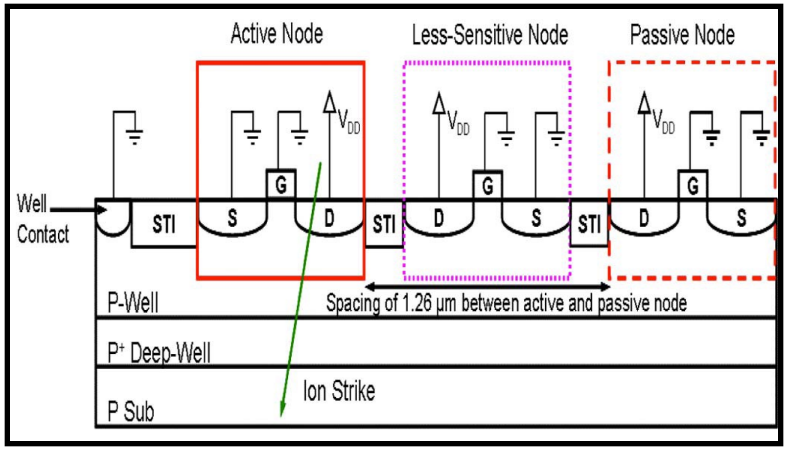
Layout-Level Mitigation: *Interleaving*

Interdigitation (Interleaving):

- *"less sensitive" devices placed between critical nodes*
- *gain benefits of nodal separation without adversely affecting total area*

Amusan 2006



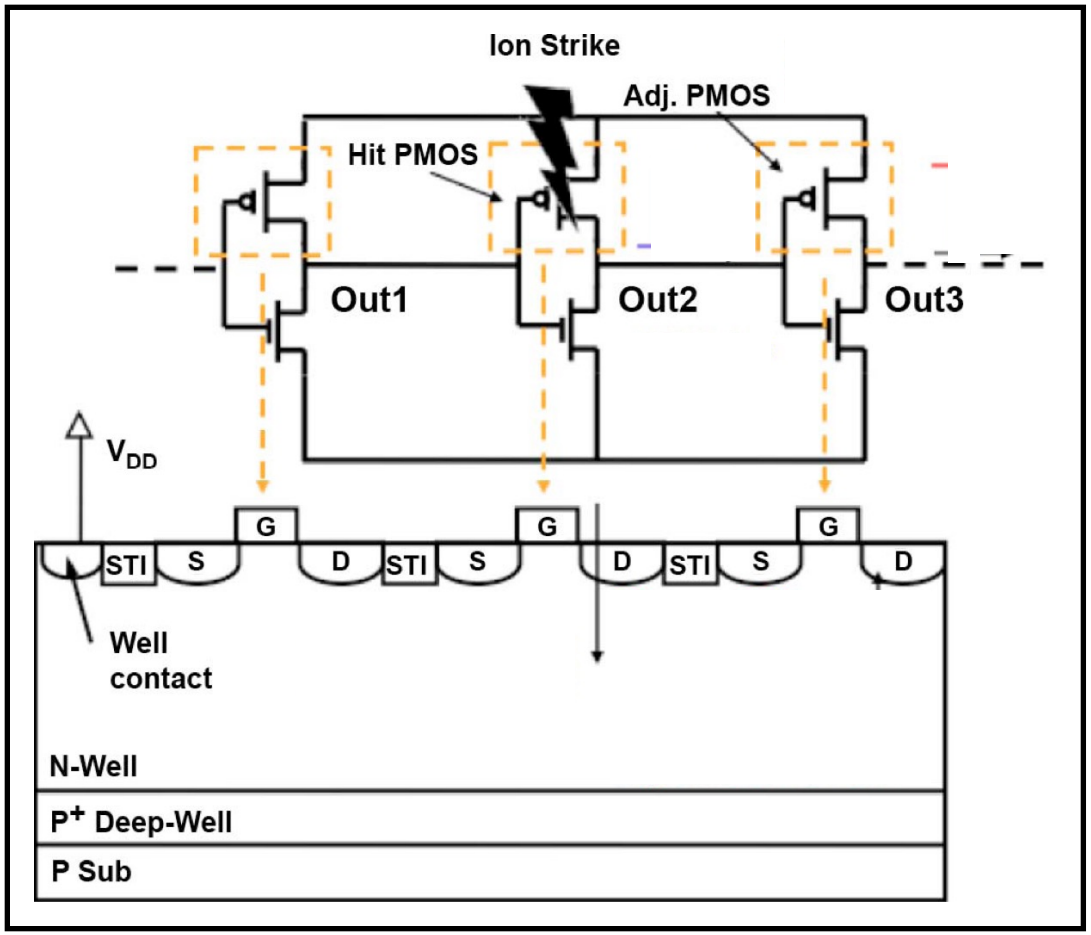


NMOS Cross Section Showing Active and Passive Devices: Less-Sensitive Node is Placed Between Active and Passive Devices

Nodal Separation of Two NMOS Devices (130 nm CMOS): Charge Collected on Passive Device with and without Interdigitation

Instead of Mitigate - Integrate (charge sharing)

The layout orientation and device spacing may be designed so the electrical signal and charge diffusion may interact as to truncate a propagated voltage transient (pulse quenching)

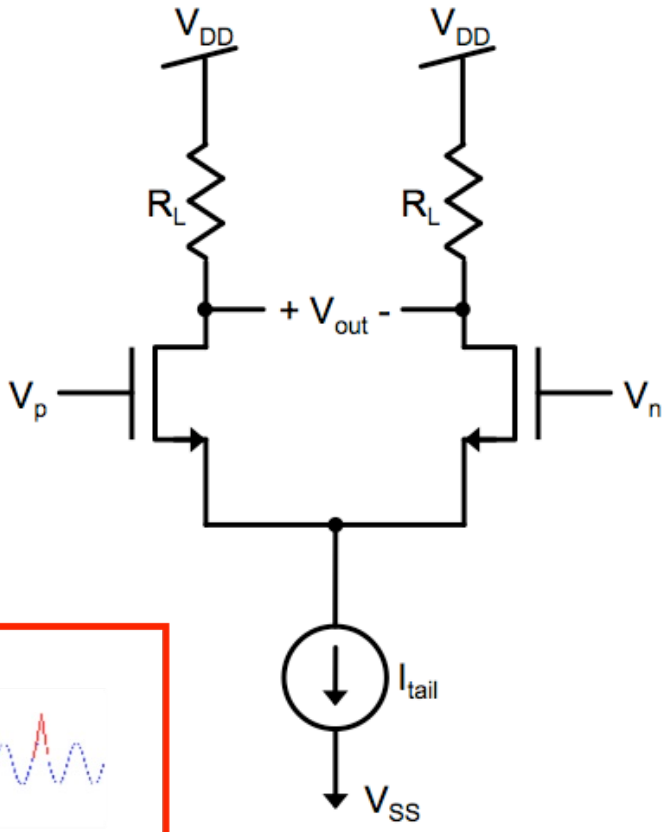


A Similar Mechanism can be Exploited for AMS ASICs

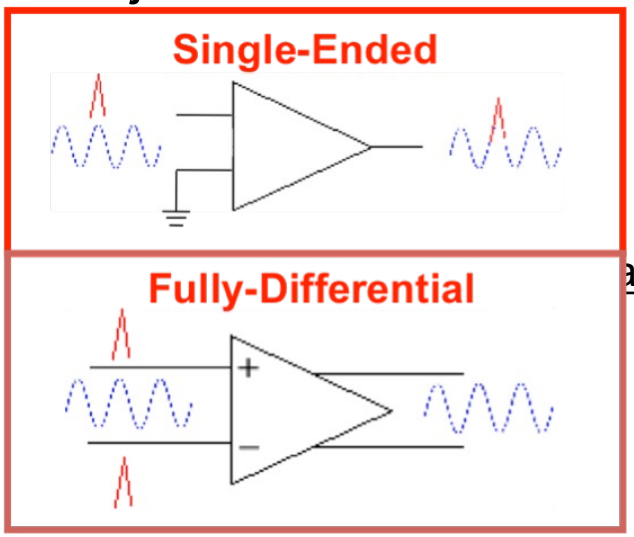
Illustration of Pulse Quenching

Hardening Via Charge Sharing

- Differential topologies are standard in most high-performance analog designs, including amplifiers, data converters, and switched-capacitor circuits
  - *improved dynamic output range and noise rejection over their single-ended counterparts*
  - *highly sensitive to Single-Event Effects!*
- Fully differential topologies reject common-mode noise
  - by maximizing charge sharing such that a single-event transient (SET) is common to both data paths, the SET can be rejected!



asic Differential Pair

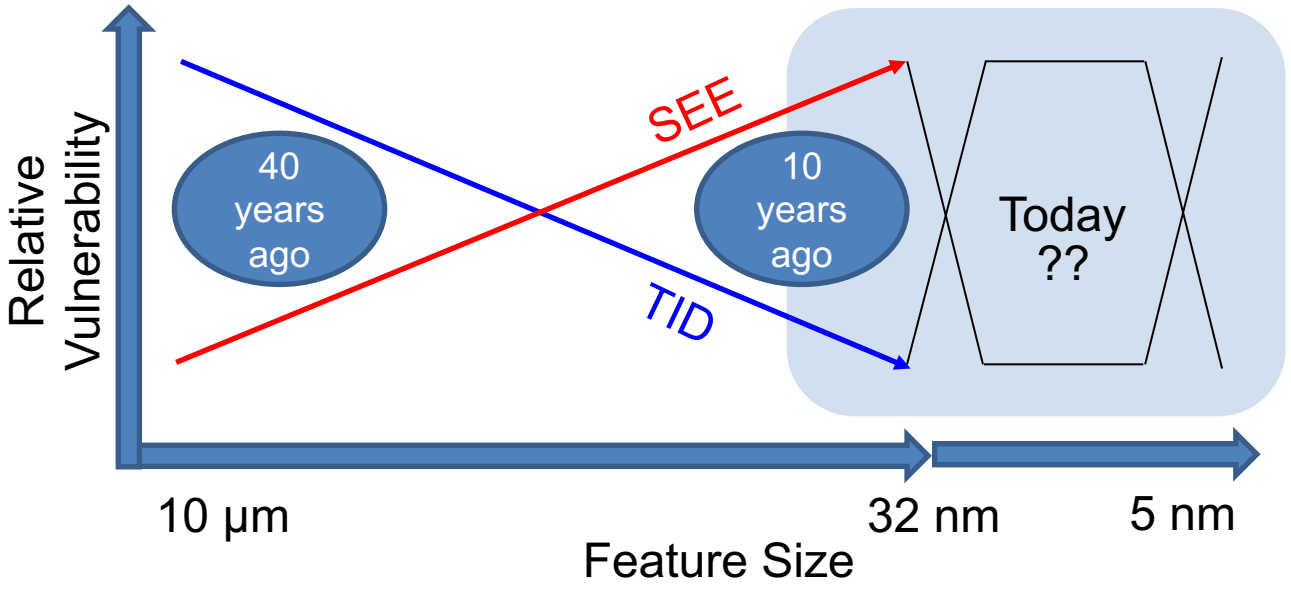


Hardening Techniques for AMS Circuits

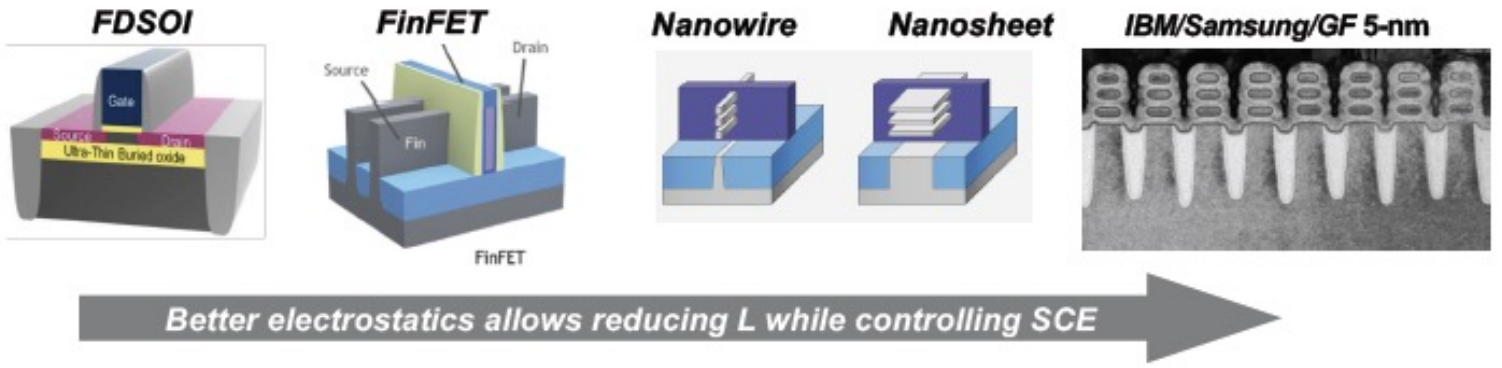
- Radiation Effects in AMS Circuits: Unique issues and considerations
- Total Ionizing Dose and Basic Mitigation Strategies
- Single Event Effects and Basic Mitigation Strategies
- Hardening by Design for AMS
- A look to the future
- Summary

Technology Scaling Trends

- In general, scaling has caused a decrease TID effects, but an increase in SEE
  - *TID improvement: thinner oxides, improved Si-SiO_2 interfaces*
  - *SEE degradation: lower supply voltage, decreased nodal capacitance*

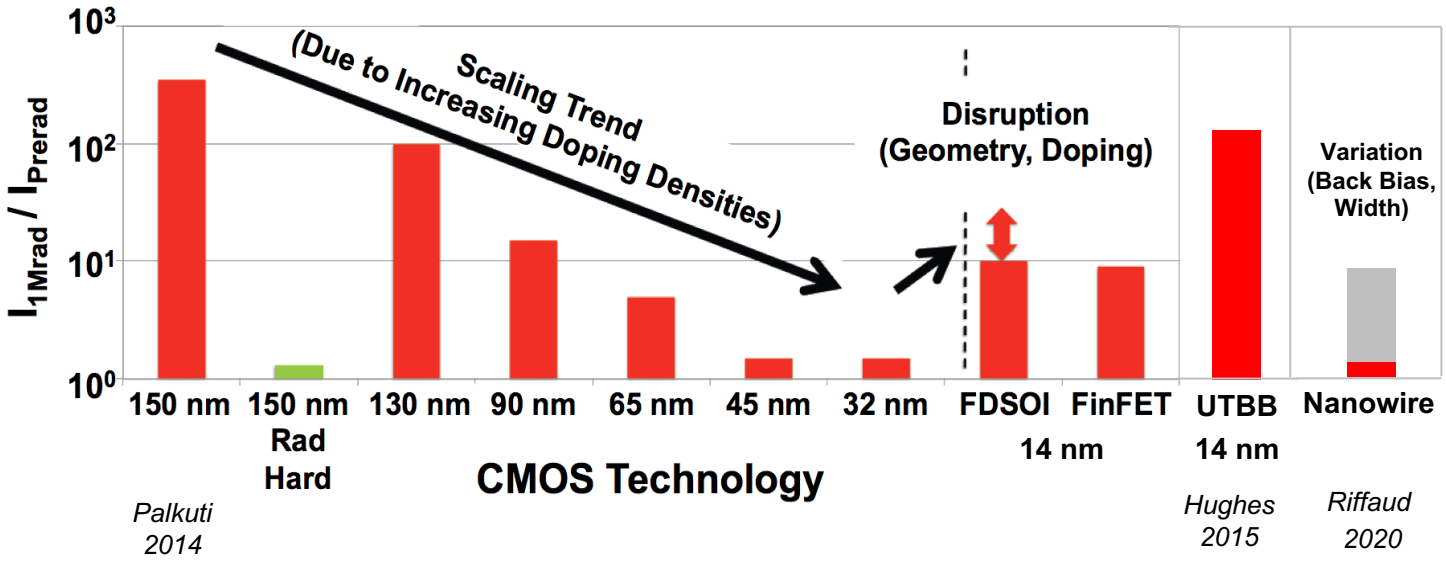


Emerging Technologies: TID

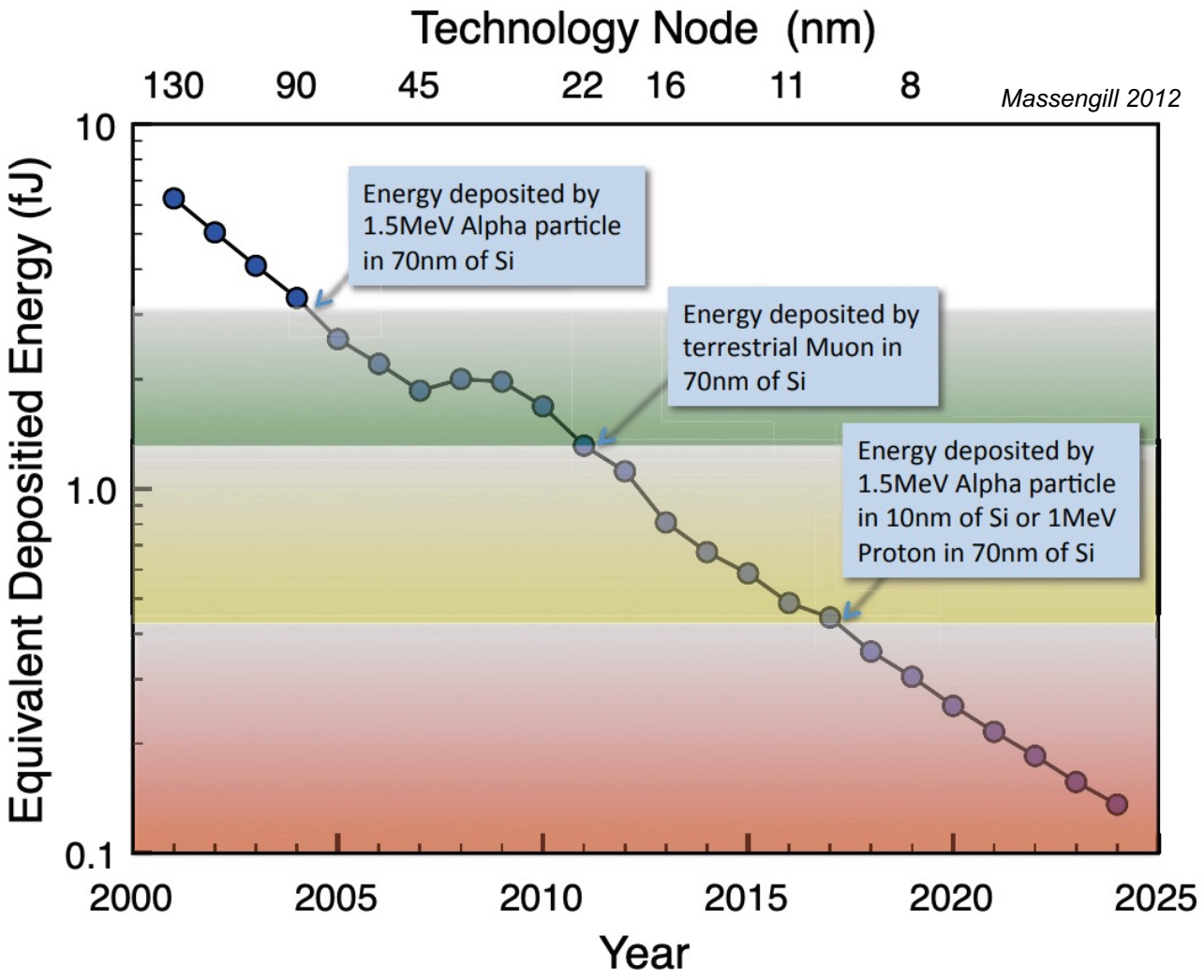


Esqueda, JPL Workshop, 2019

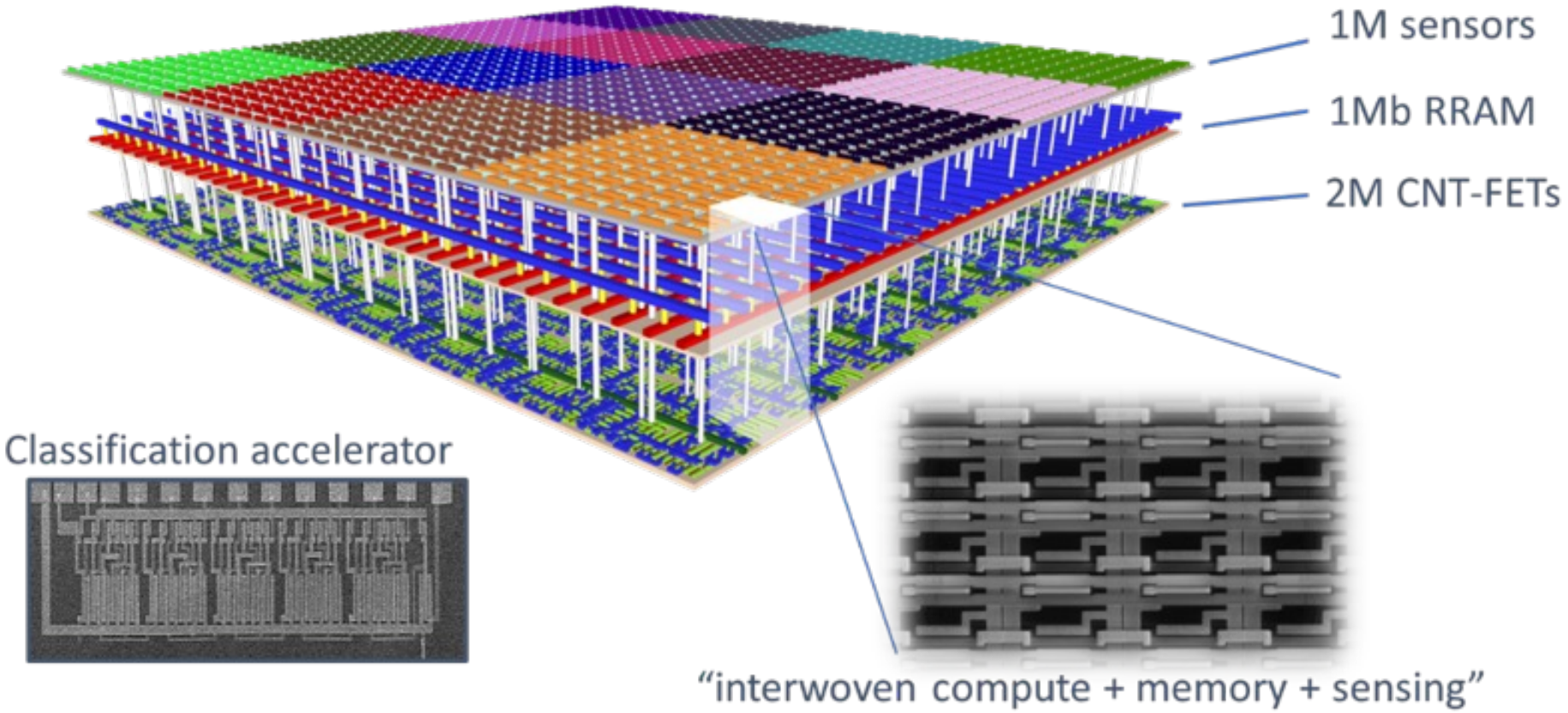
**SCE: Short-Channel Effects*



Emerging Technologies: SEE

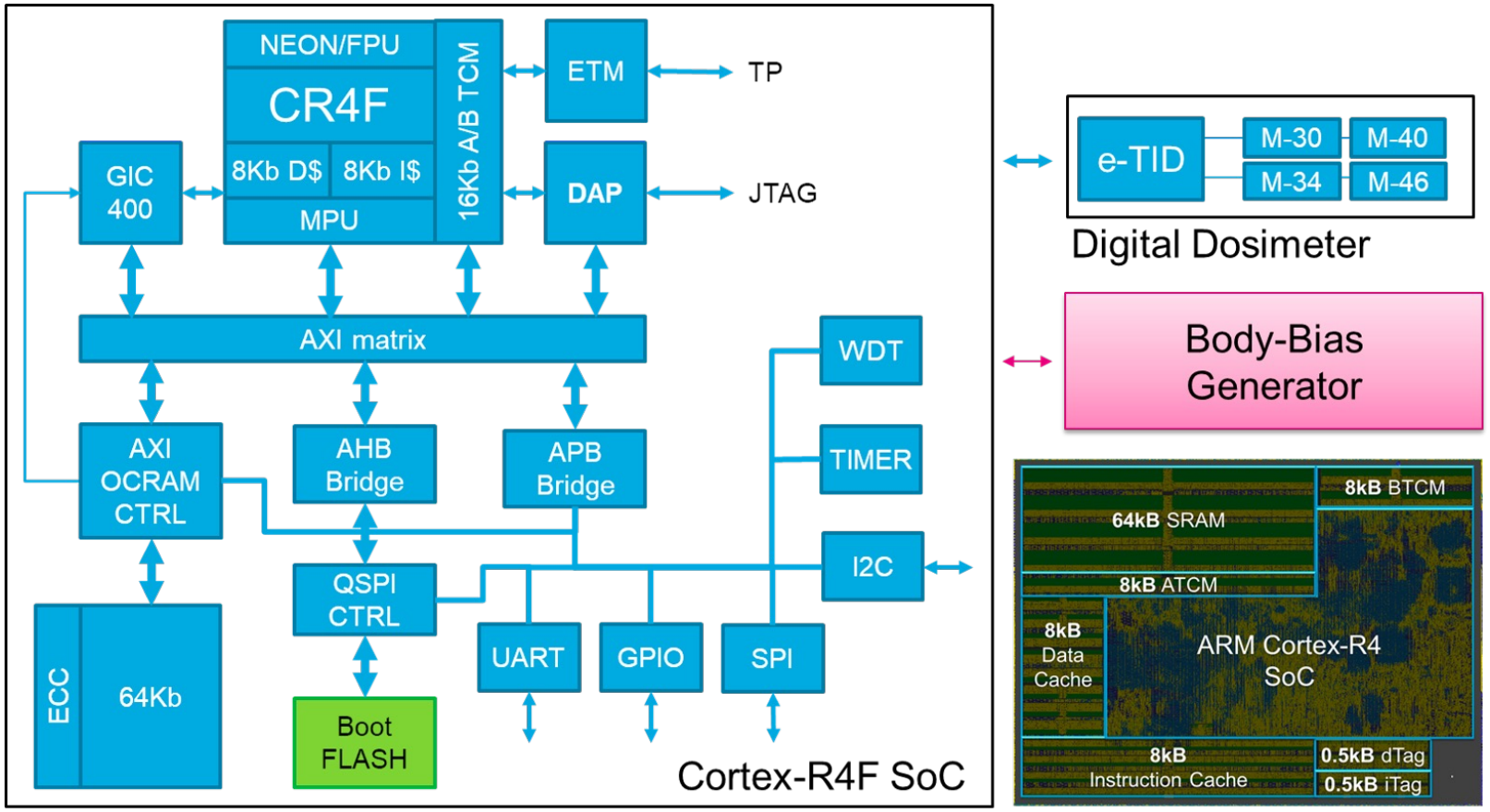


Radiation Hardening by Design



3D-SoC sensor/machine learning IC from Stanford (2017)

Integrated Rad-Hard SoC



Rad-Hard ARM SoC Prototype *Abouzeid 2021*

Hardening Techniques for AMS Circuits

- Radiation Effects in AMS Circuits
  - *Unique issues and considerations*
  - *Total Ionizing Dose*
  - *Single Event Effects*
- Total Ionizing Dose Mitigation Strategies
- Single Event Effects Mitigation Strategies
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Summary

- The ability to put entire systems on a single chip has increased the demand for mixed analog/digital (mixed-signal) circuits
- Total ionizing dose (TID) and single-event (SE) phenomena present challenges for analog & mixed-signal (A/MS) systems
  - *TID-induced mismatch can result in a variety of performance penalties and non-monotonic responses*
  - *Single-event transients (SET) are subject to cross-domain response mechanisms*
  - *SE mechanisms may not be tractable using conventional analysis techniques*
  - *New error metrics may be required due to the complexity and functionality*
- However, there is a common thread:
  - *Reduce positive hole trapping or the influence of positive hole trapping in oxides*
  - *Reduce of the sensitivity to TID-induced mismatch*
  - *Reduce collected charge and/or increase critical charge*
  - *SE performance of AMS tends to be dominated by:*
    - gain-bandwidth
    - speed
    - drive strength
    - high-impedance nodes