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SEE effects on VLSI devices challenges and solutions

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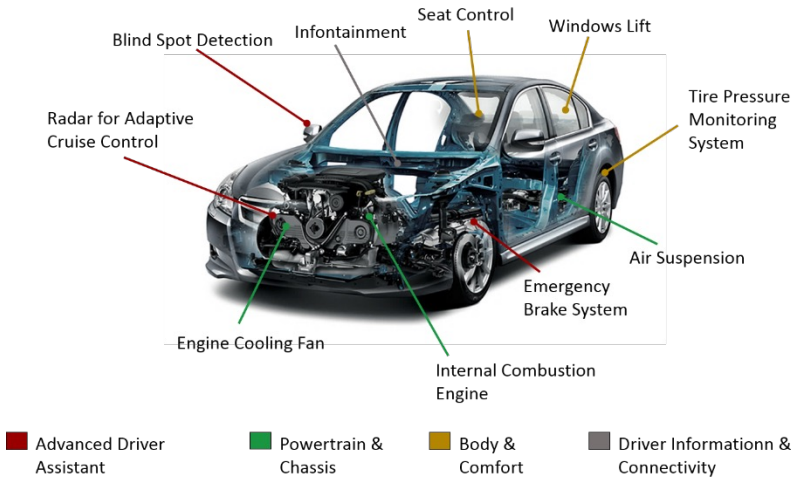
Outlines

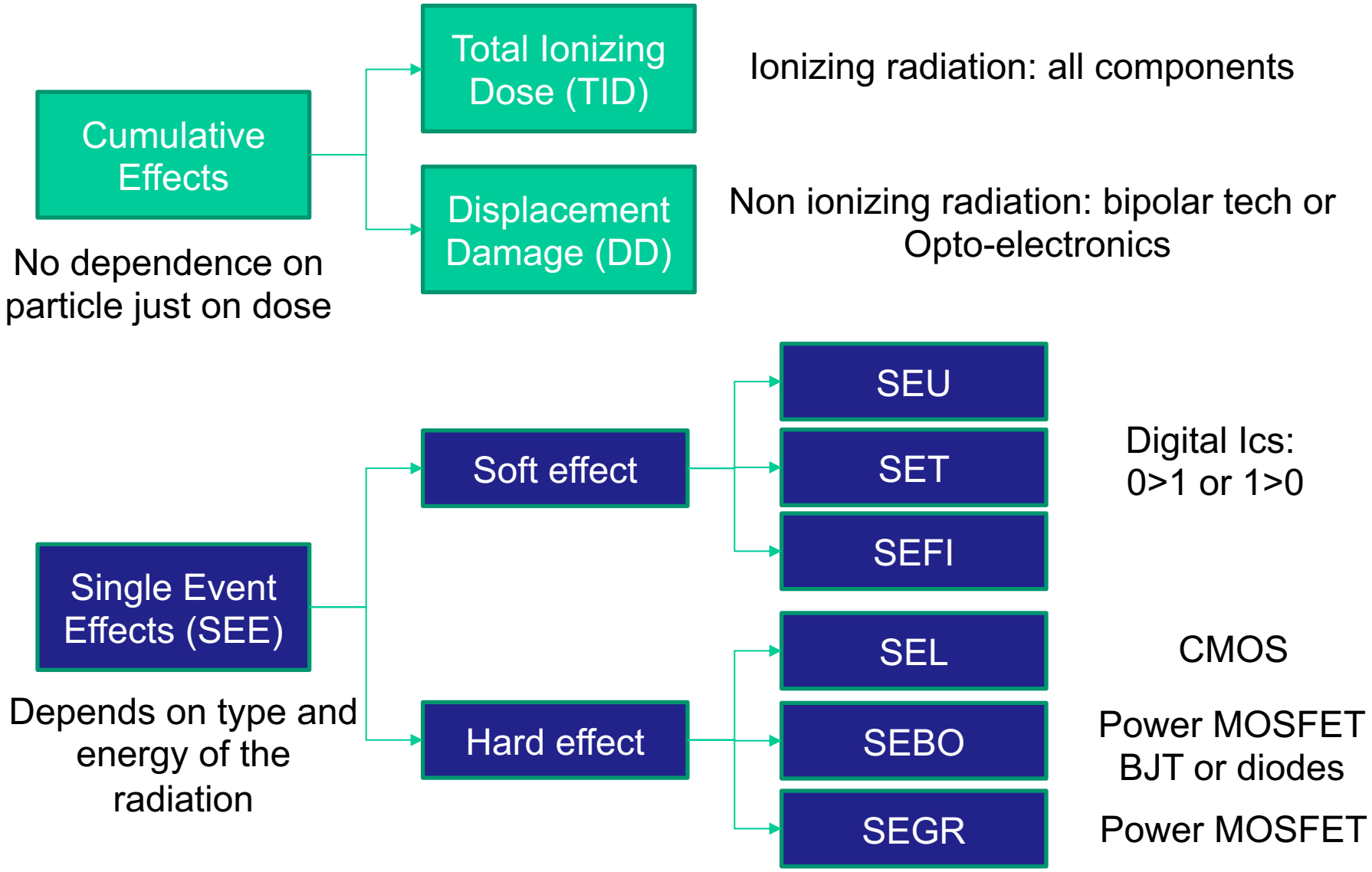
- Introduction
- Radiation effects on CMOS devices
- SEE effects in ASIC
- SEE effects in FPGA
- SEE mitigation techniques
- CAD tools: analysis and mitigation
- Applications and Experimental Results
- Conclusions

Introduction

- The need of rad-tolerant electronic devices is wide
  - Space applications
  - Avionics
  - Nuclear plants control instrumentation
  - High energy physics
  - Automotive

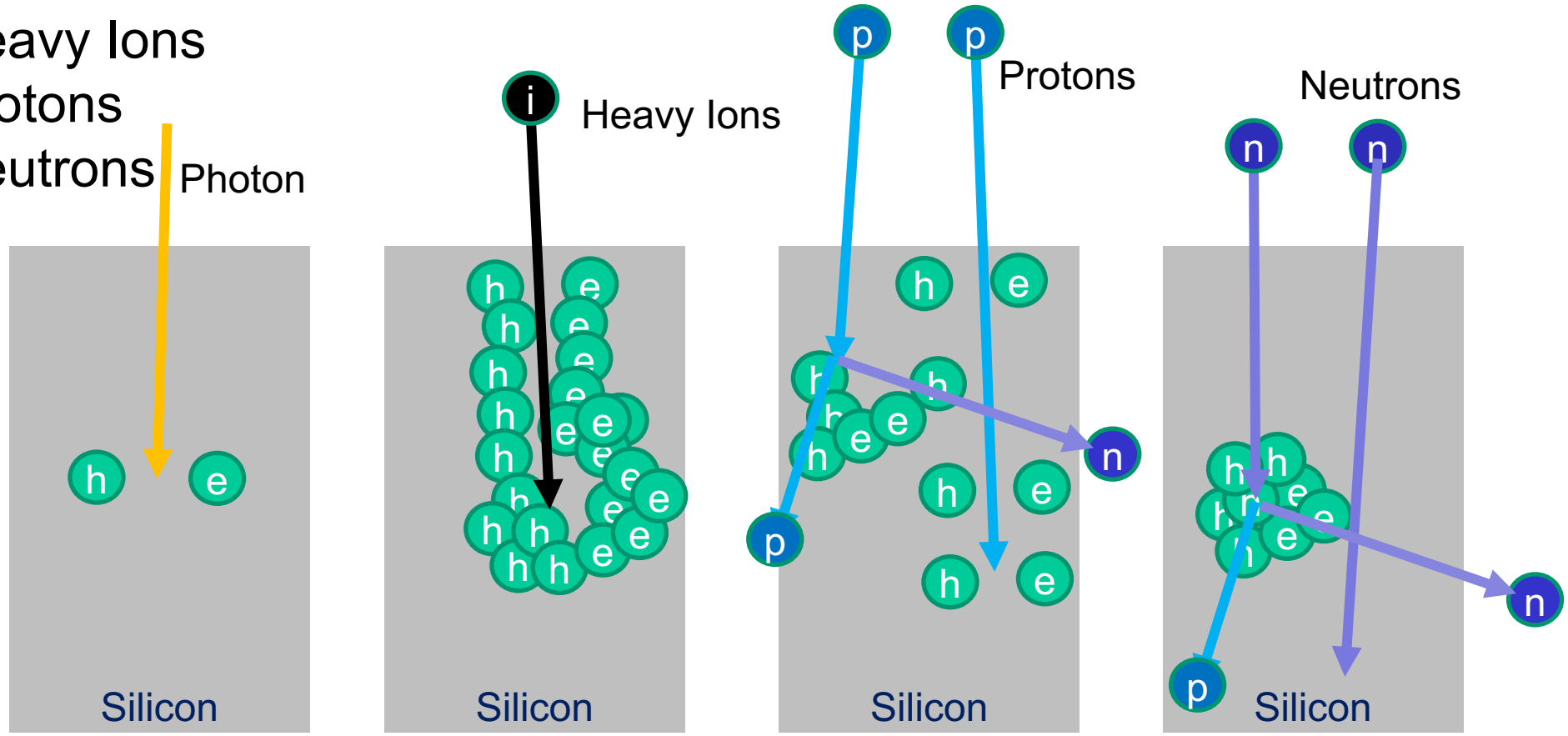


Introduction



Introduction

- The most relevant particle basic mechanisms in Si are related to
  - Photons
  - Heavy Ions
  - Protons
  - Neutrons



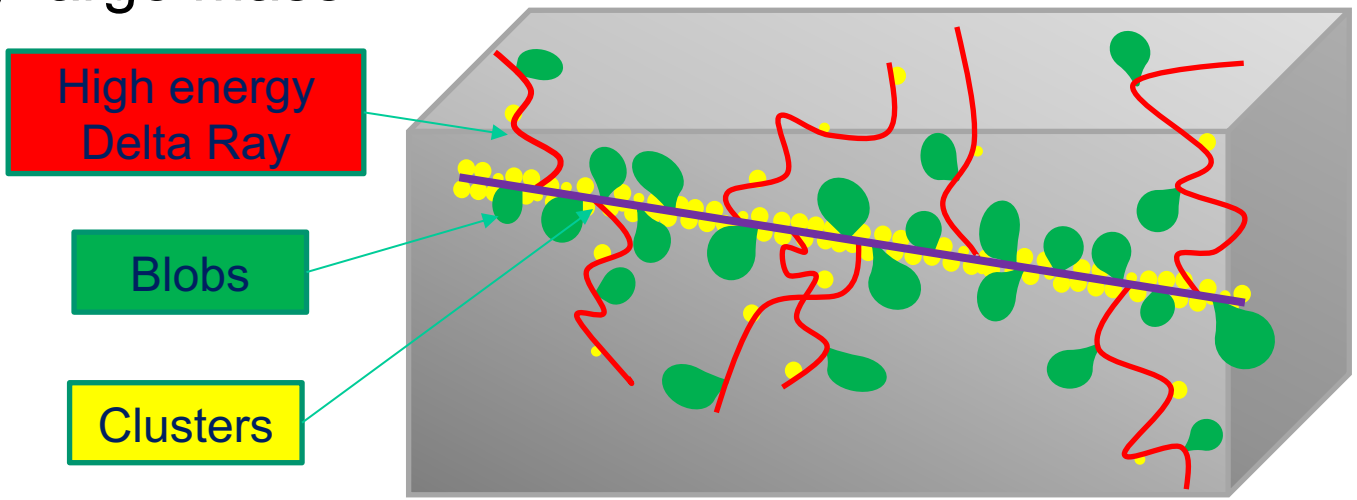
Small density e-h

Large density e-h

Small density for direct ionization.
High density from HI from nuc interation with Si nuclei

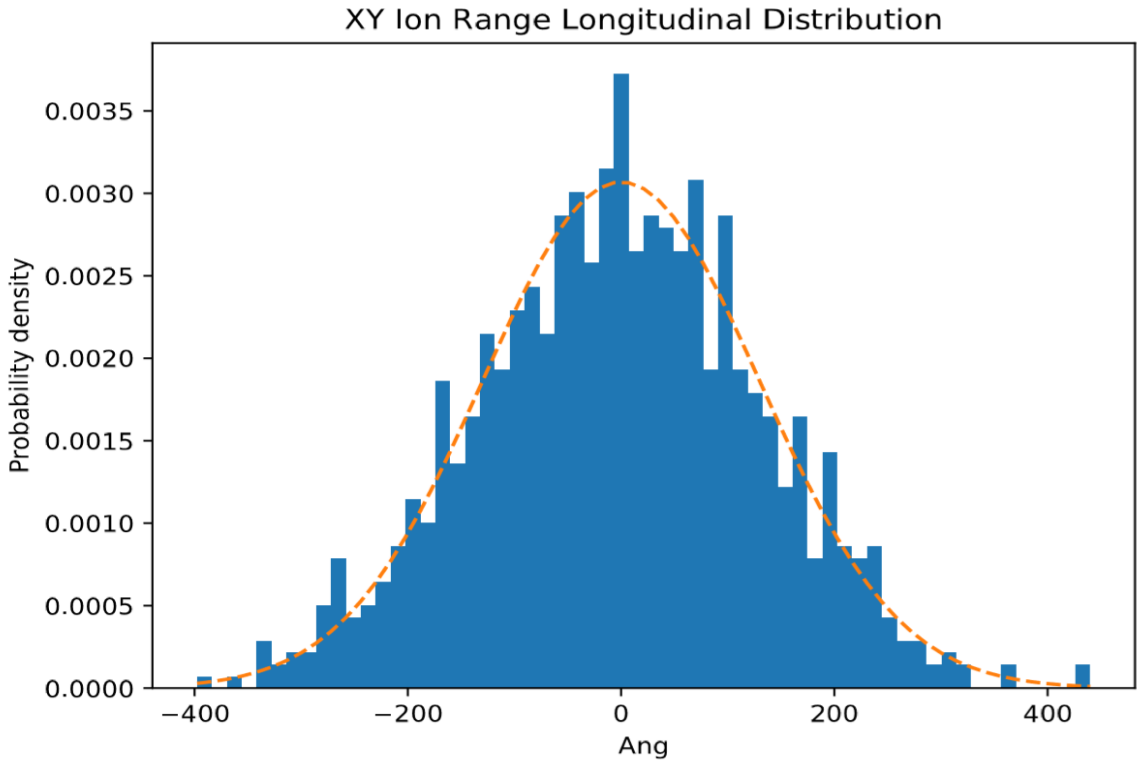
Introduction

- The ion interacts with the electrons of the surrounding medium exciting or ionizing molecules
- The ion energy may create:
  - «clusters» of other ionized or excited molecules
  - «delta ray» or blobs
  - «high energy delta ray»: secondary trajectories with possibly large mass



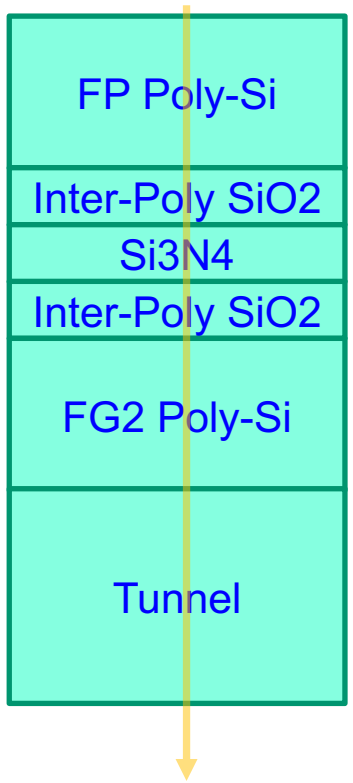
Radiation effects on CMOS devices

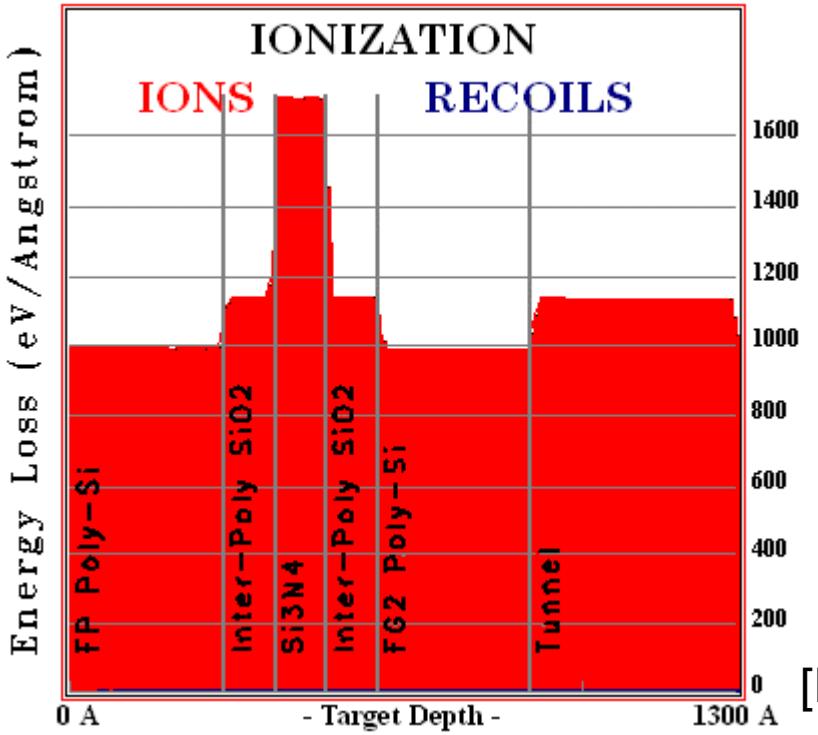
- The Ion range longitudinal energy distribution can be modeled as a probabilistic density
- The range with respect to the center (0 Ang) may represent the probability of side phenomena
  - Clusters
  - Blobs
  - High Energy Delta Ray



Radiation effects on CMOS devices

- A particle ray crosses multiple layers
- Ionization Energy loss per layer is related to the type of composite Si material



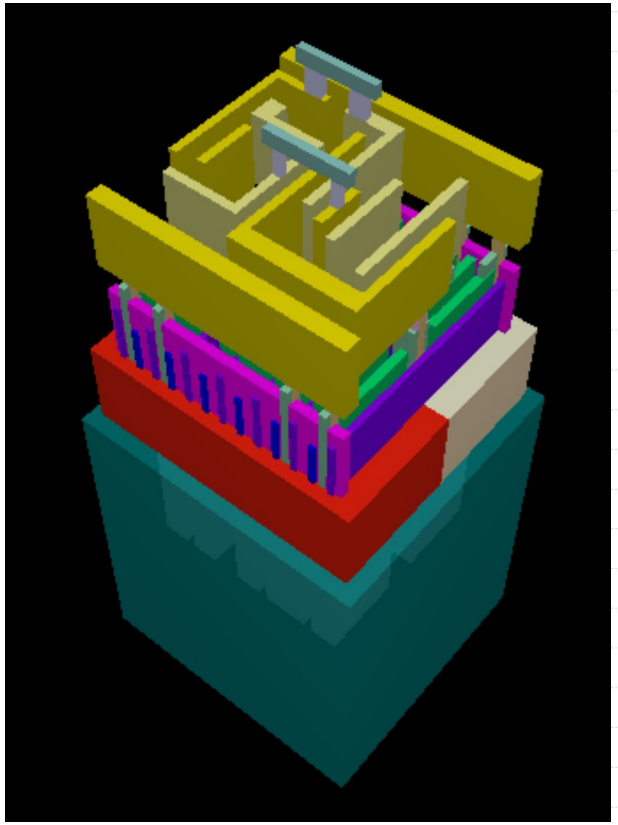


[IEEE ETS 2018]

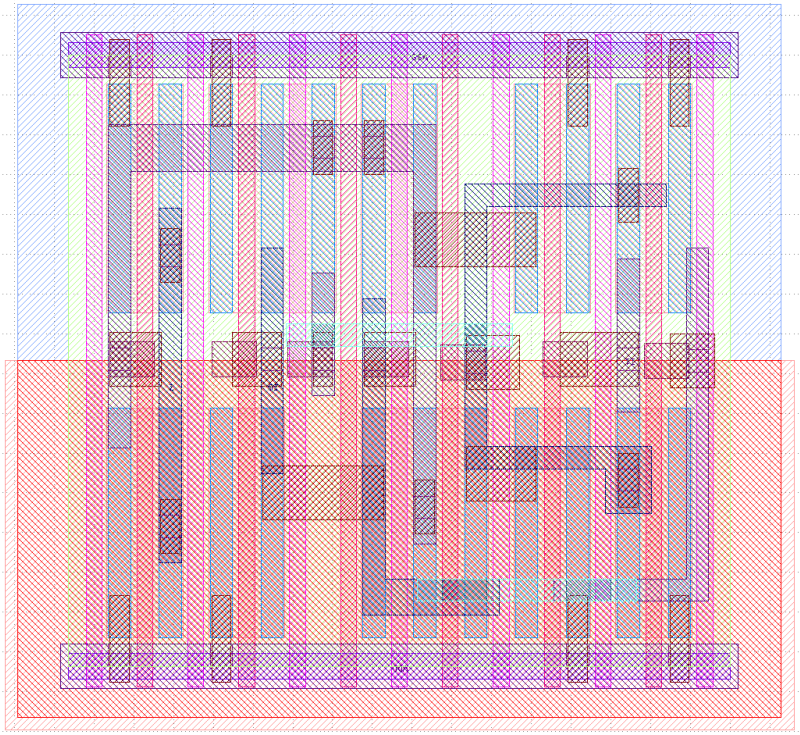
A Floating Gate cross section and the Energy Loss (eV/Ang) considering Xe ion at 62.5 MeV

Radiation effects on CMOS devices

- Example: A MUX2_X1 logic cell at 28nm technology



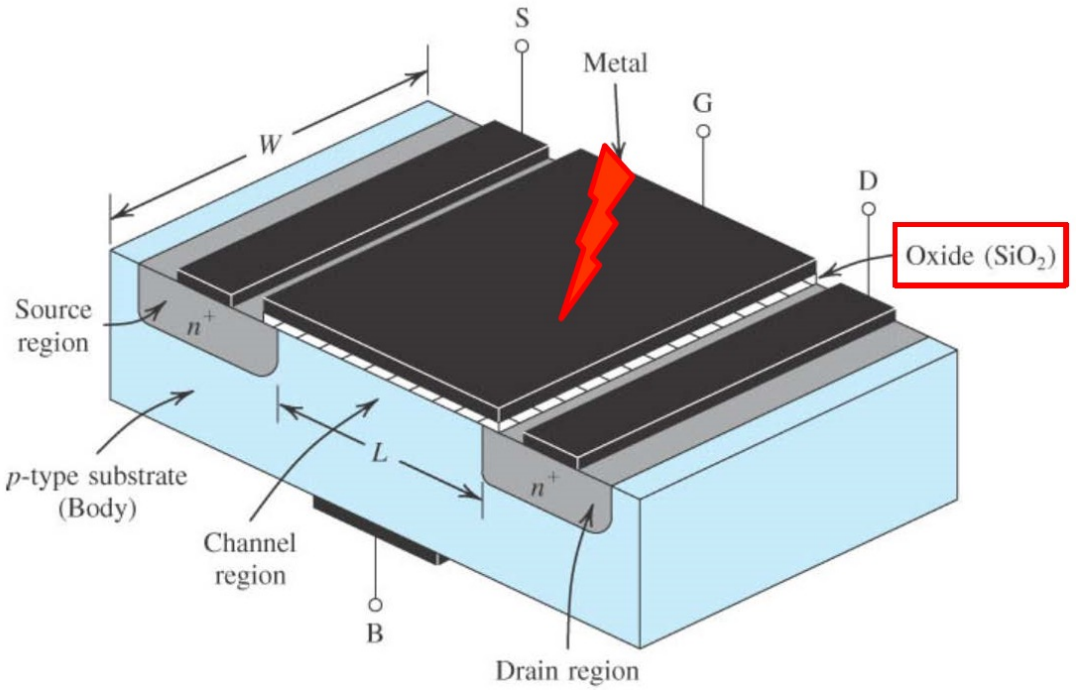
[GDS 3D View]

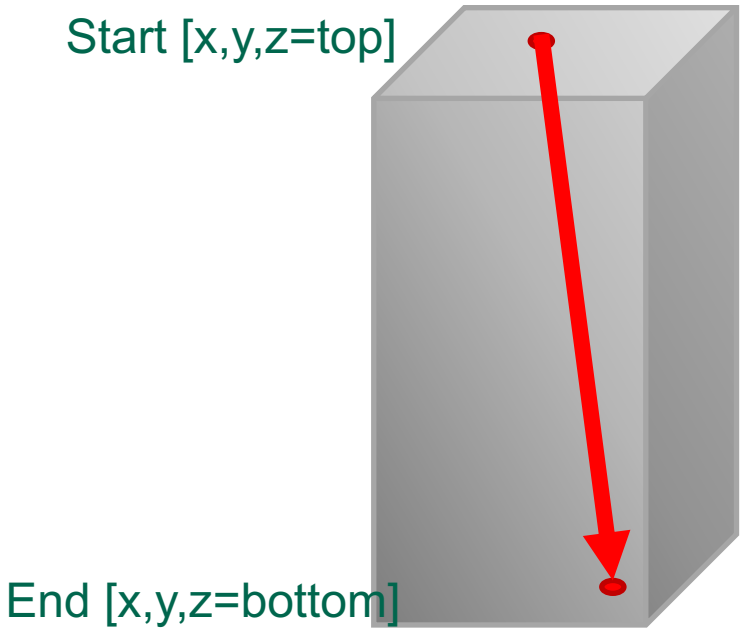


[GDS 2D view]

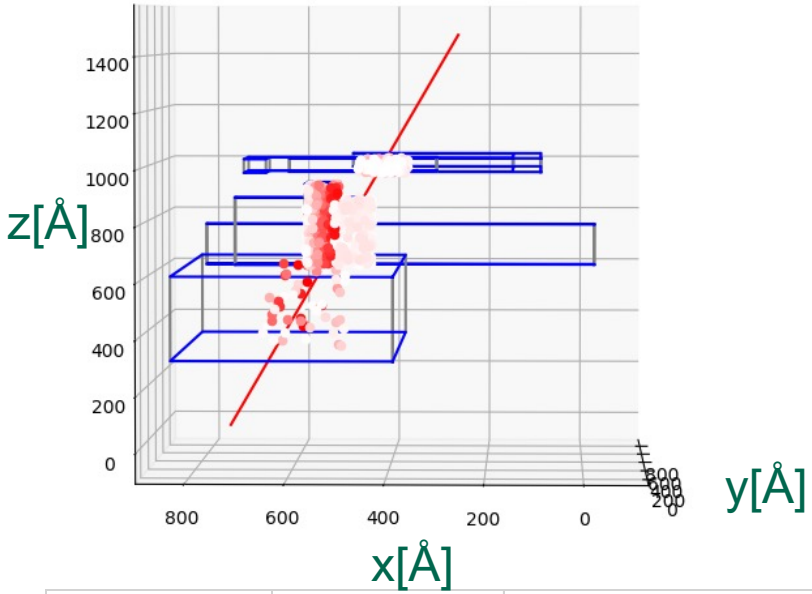
SEE effects in VLSI

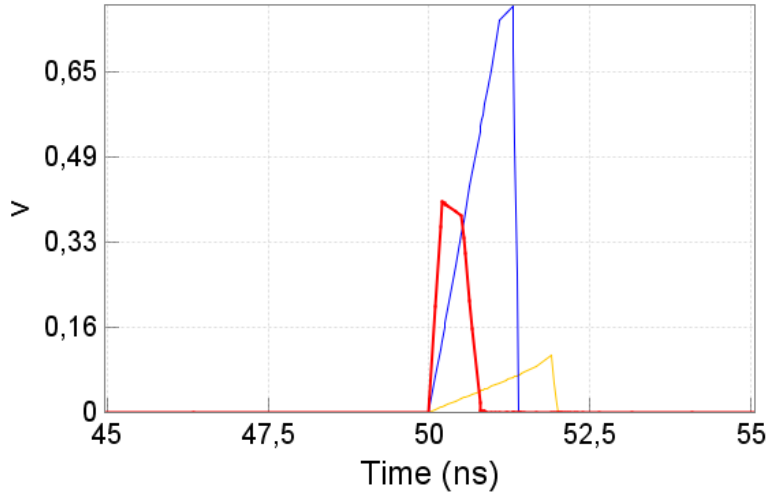
- Single Event Effects (SEEs) depend (not only) on
  - the type of radiation
  - the geometry
  - type and order of traversed layers





Radiation effects on CMOS devices

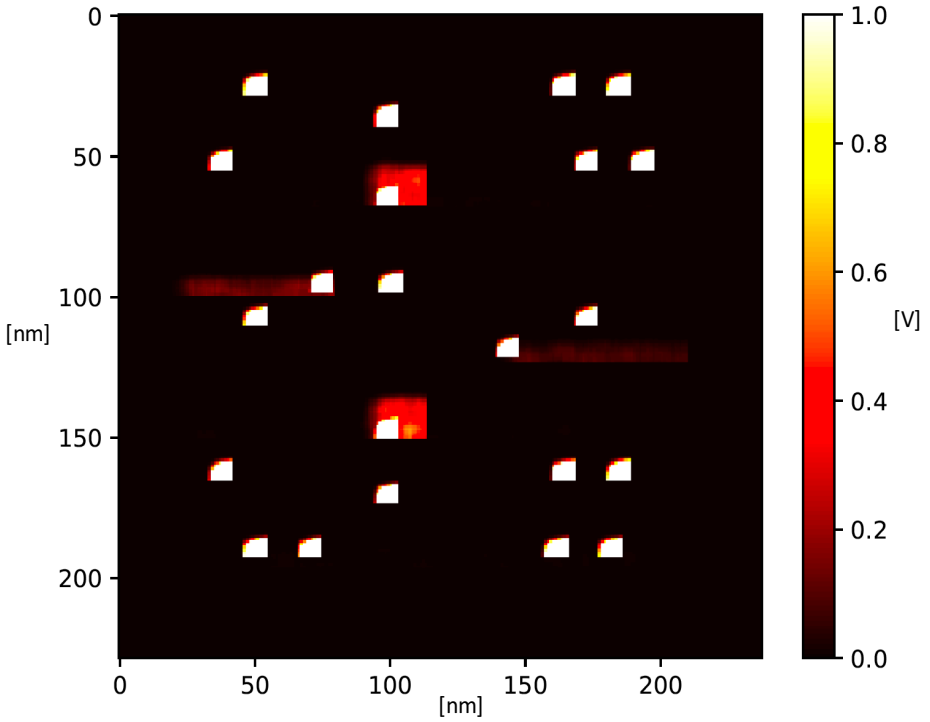


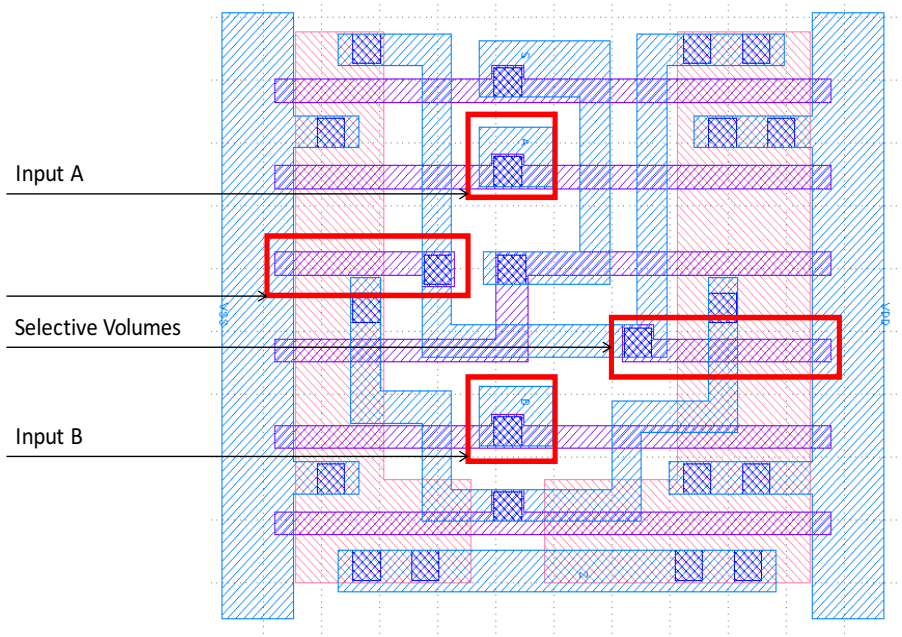


Cube ID [#]	Layer ID [#]	Energy Distribution/Cube [%]	Energy KeV/Cube	Maximal Expected Peak [V]
19	8	10,1	0,26	1,20E-04
27	6	6,5	7,93	9,00E-06
35	11	33,7	7,8	5,80E-03
36	11	19,3	0,66	4,90E-04
111	16	11,6	4,94	2,16E-03

A 3-D Simulation-Based Approach to Analyze Heavy Ions-Induced SET on Digital Circuits [IEEE Trans. on Nuclear Science 67 (9), 2034-2041]

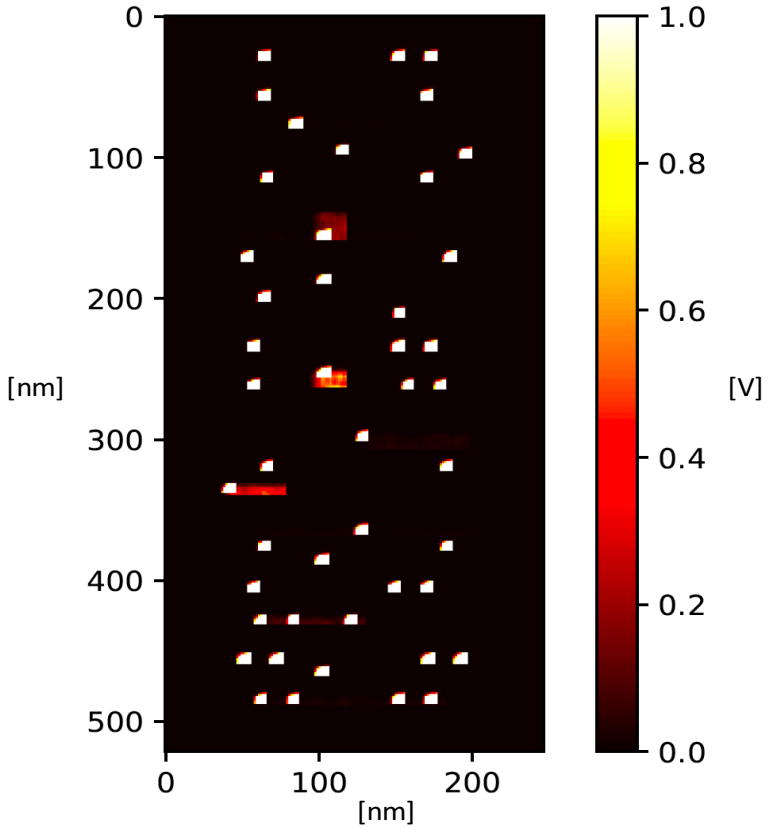
Radiation effects on CMOS devices

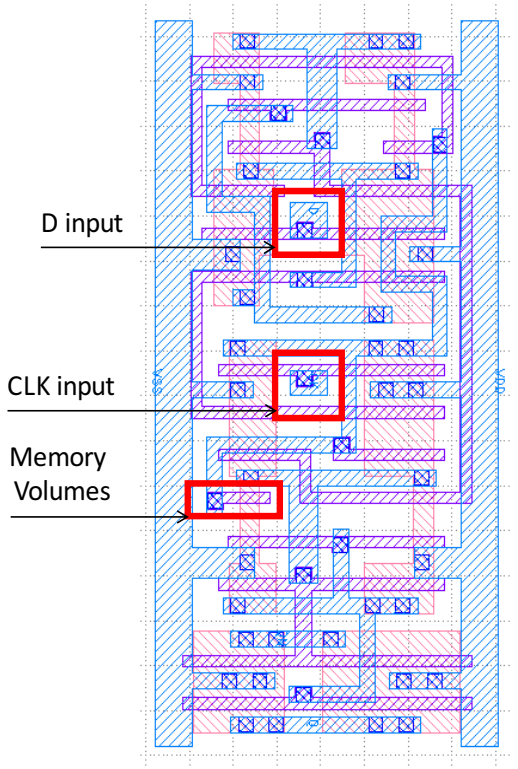




[MUX21 at 65nm]

Radiation effects on CMOS devices

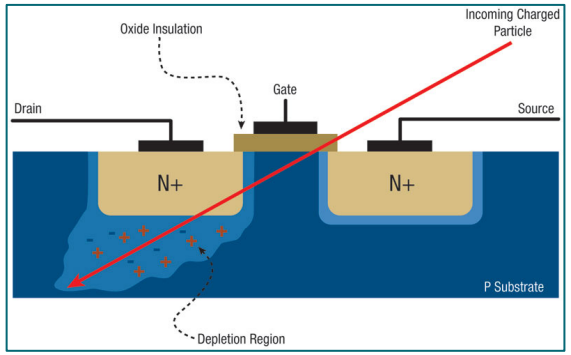


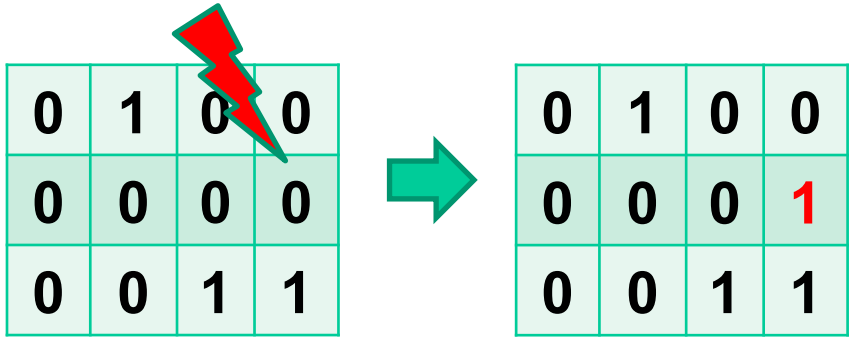


[FF at 65nm]

SEE effects in ASIC

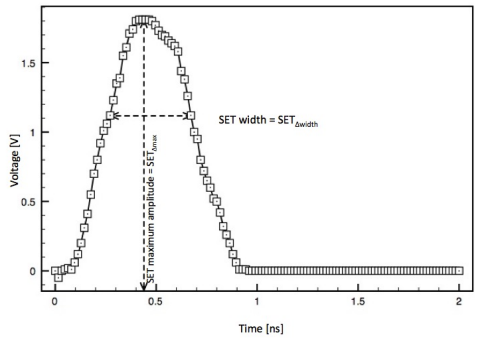
- A radiation particle can generate a Single Event Upset (**SEU**) if affecting a memory element: Data FF or RAM bit-flip





Single Event Upsets (SEUs)

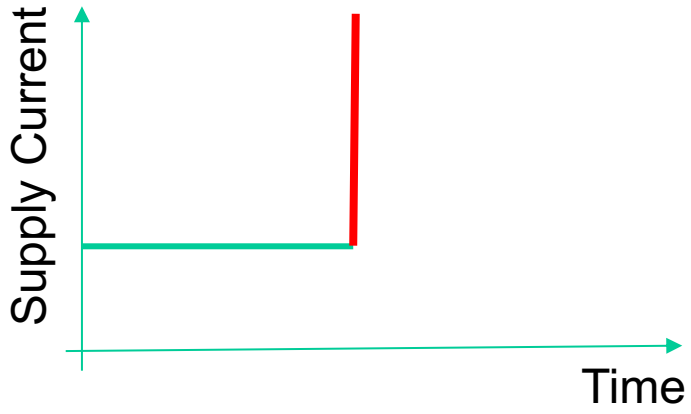
- A radiation particle can generate a Single Event Transient (**SET**) if affecting a logic element: combinational standard cell.



An **SET** is critical if sampled: higher is the sampling frequency, higher is the probability the error is propagated

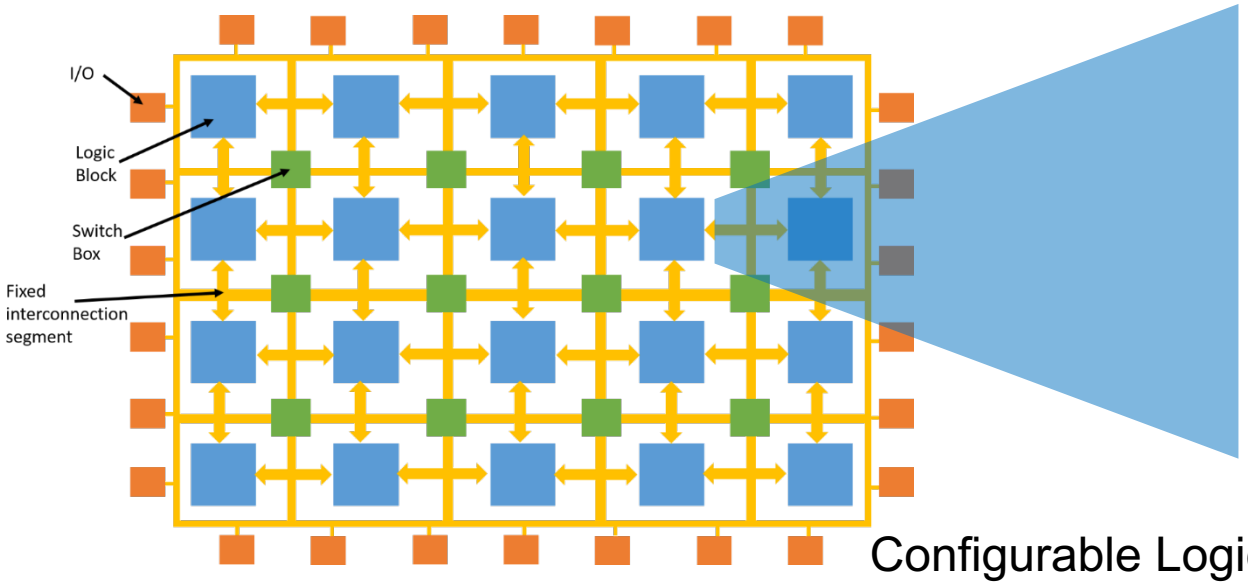
SEE effects in ASIC

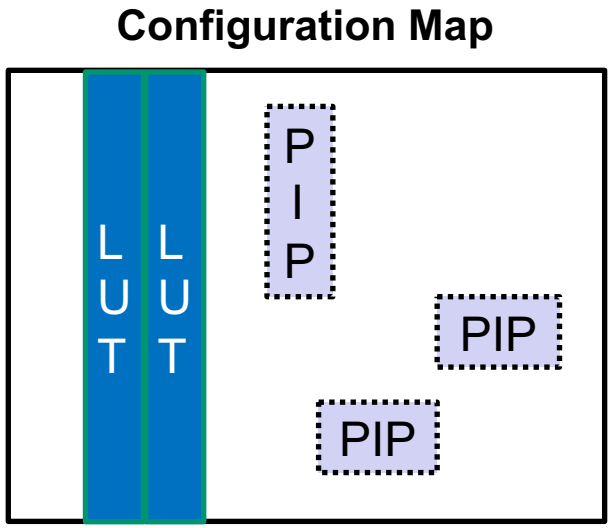
- A radiation particle can generate a Single Event Latch-up (**SEL**) if affecting any element of the ASIC in particular in case:
  - Electrical transient on I/O lines
  - High temperature
  - Bad sequencing of power bias
- SELs are **hard SEU** effects
- The supplied current should be monitored and shutting off power and I/Os if a **current bump** is detected.



Field Programmable Gate Array

- An FPGA is a user-programmable matrix of logic blocks with programmable interconnections that can implement any logic function or algorithm





Configurable Logic Block (CLB) on coordinates (X,Y)

SEE effects in FPGA

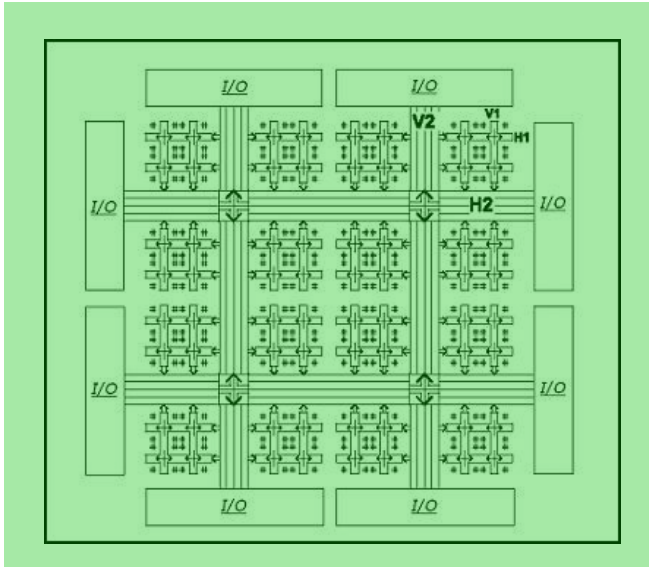
- Considering soft SEE, an **SEU** might result in data corruption, transient disturbance, high current conditions
- Depending on the FPGA configuration memory technology, it is possible to distinguish
  - SEU in User Memory (SRAM and Flash)
  - SEU in Configuration Memory (SRAM)
    - Logic
    - Routing
  - SET in the Look Up Tables (LUTs) or Logic Element (SRAM and Flash)

SEU effects in SRAM-based FPGA

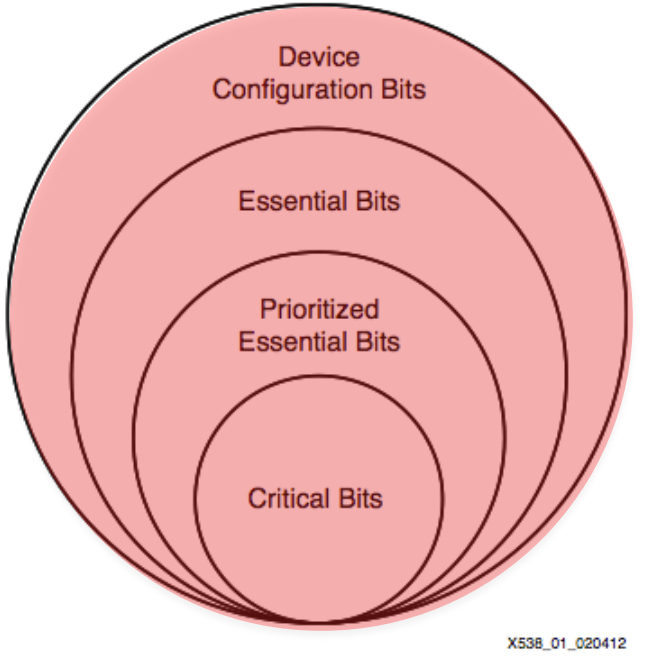
- **SEU** within the configuration memory
  - FPGA resource not affected : **NO ERROR**
  - FPGA resource affected : **ERROR**
- **SEU** induced architectural modification
  - Logic Element: LUT, MUX, FF Configuration
  - Interconnections: Switchbox

SEU effects on FPGA Configuration Memory

- **Several tools focus on the identification of essential and critical bits**

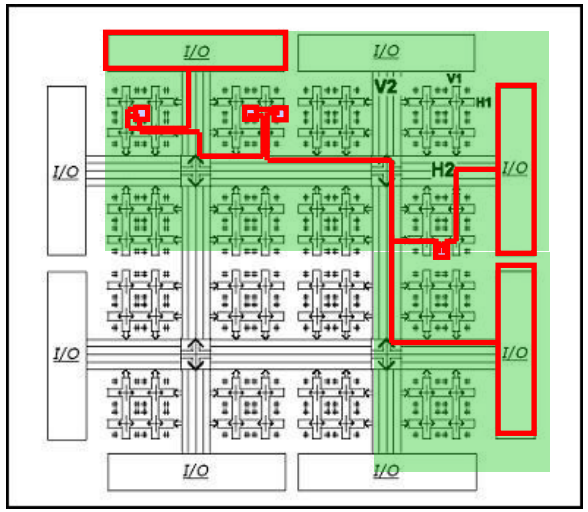


0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0

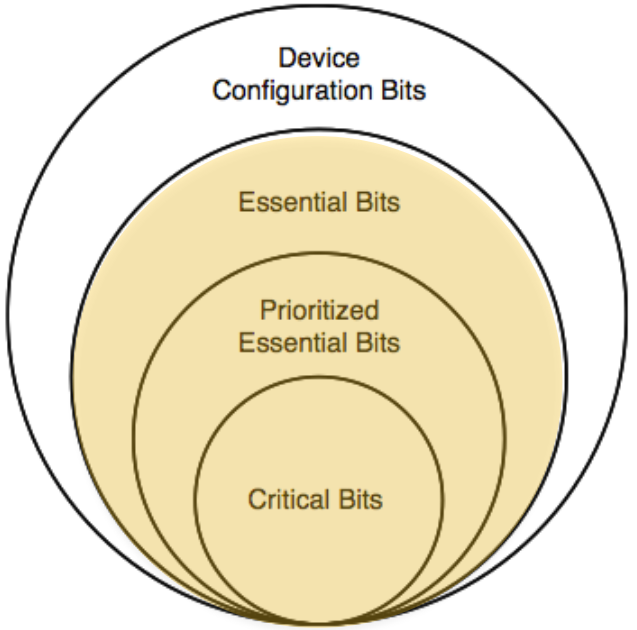


SEU effects on FPGA Configuration Memory

- **Several tools focus on the identification of essential and critical bits**

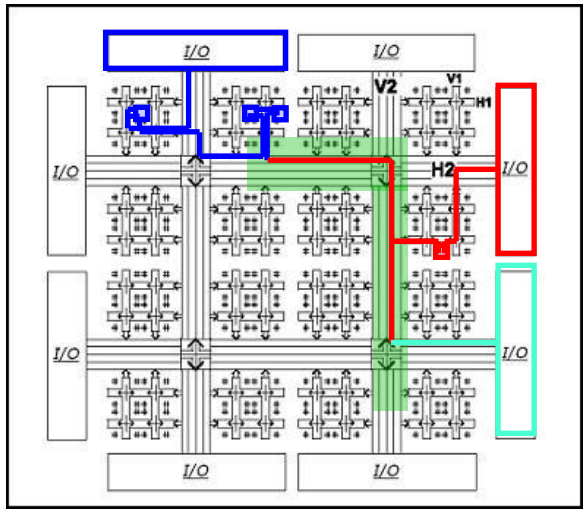


0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0

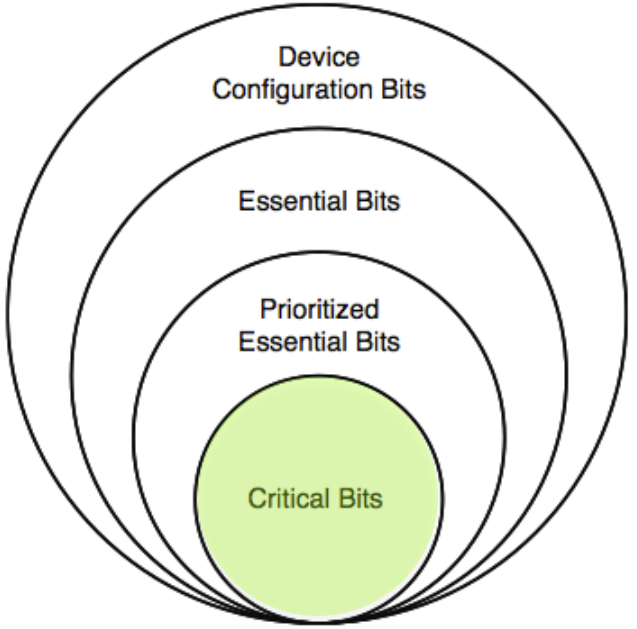


Identification of Critical Bits

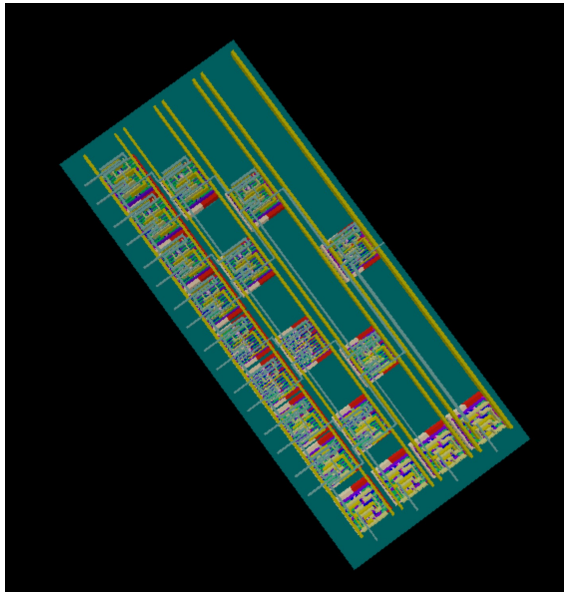
- Identify single point of failures of TMR circuits
- Critical bits are used to compute the FPGA circuit error cross-section

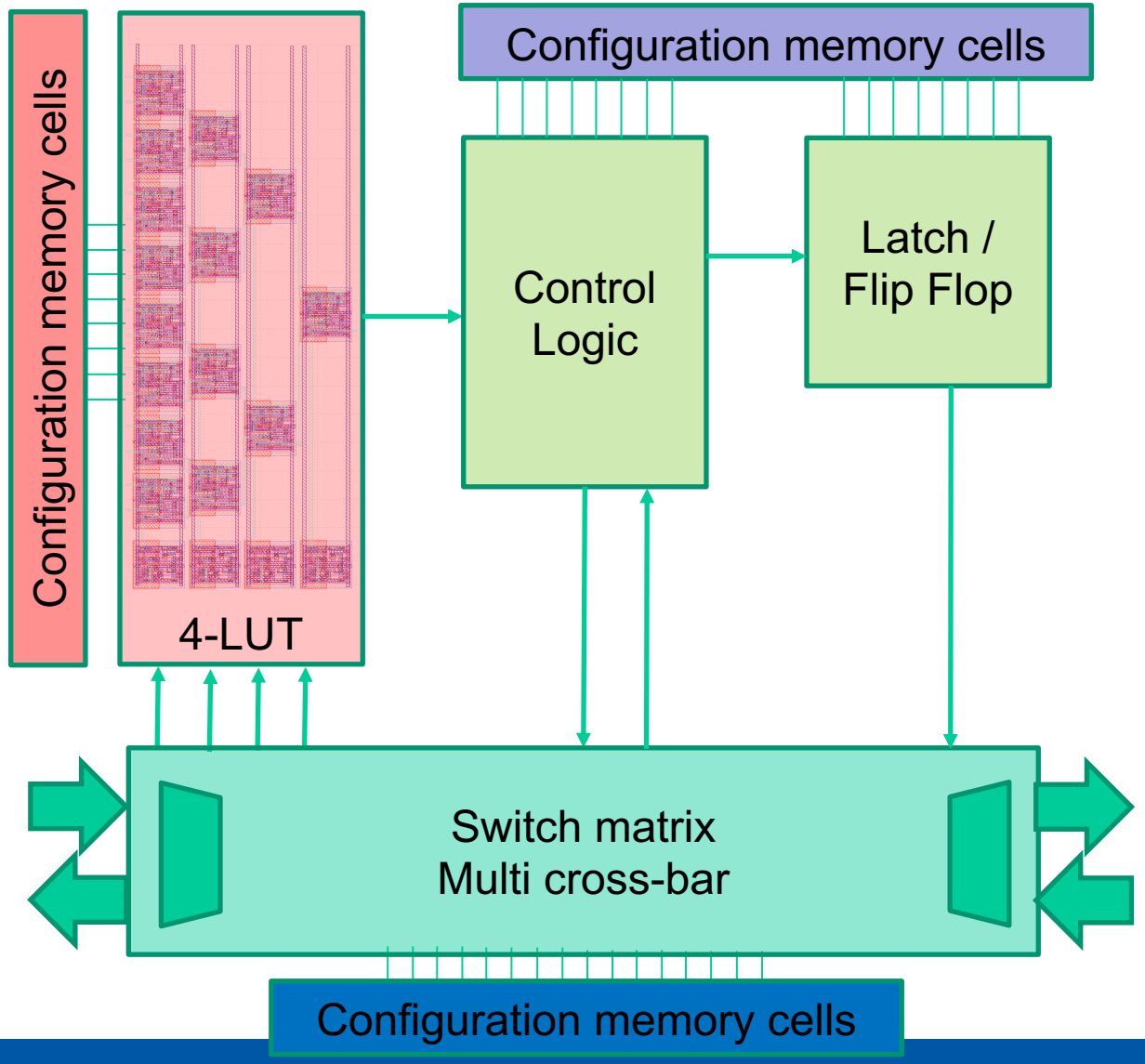


0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0



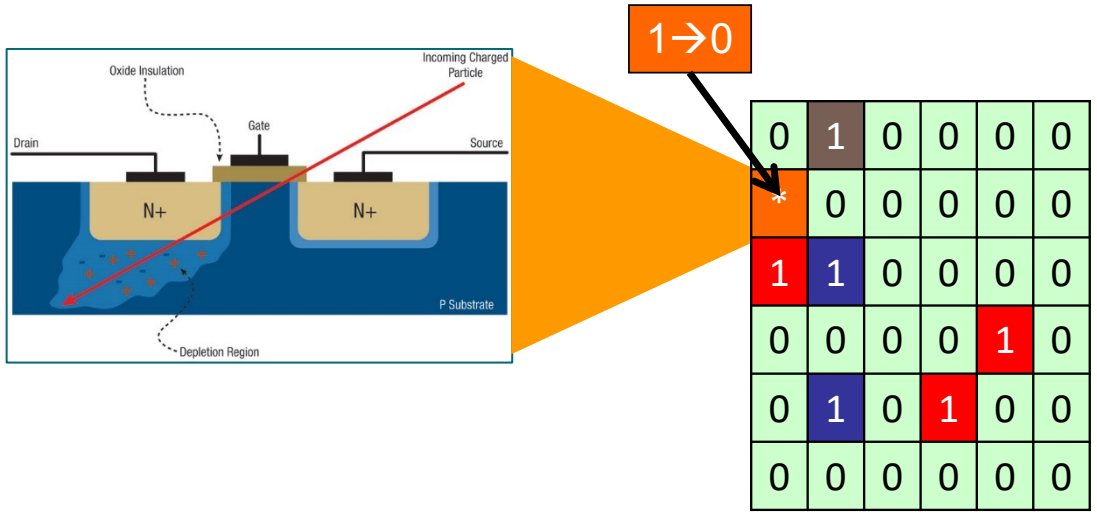
SEE effects in FPGA

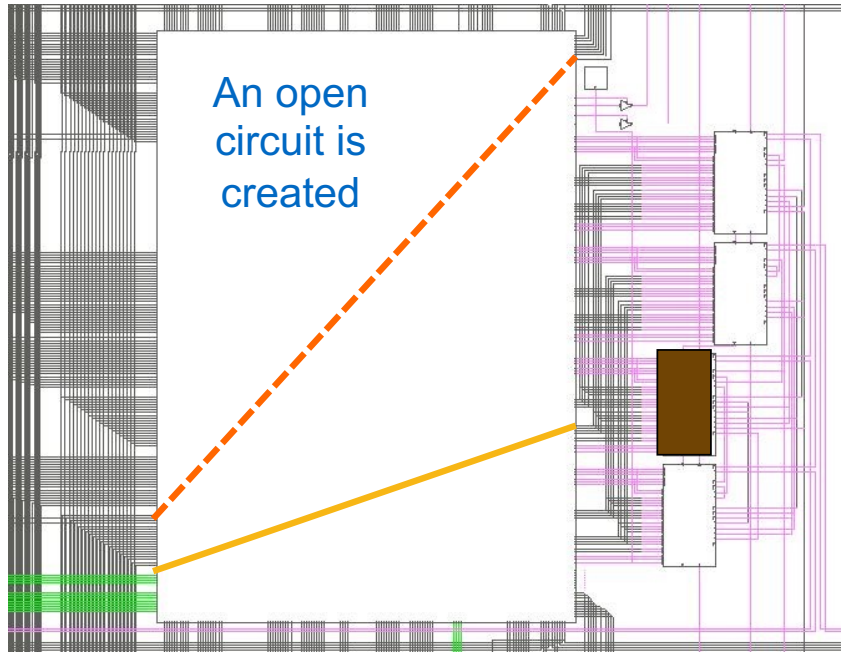




SEE effects in FPGA

- SEUs may cause structural changes in the circuit implemented on the FPGA
- TMR techniques suffer cross-domain failure induced by single and multiple bitflips within the configuration memory

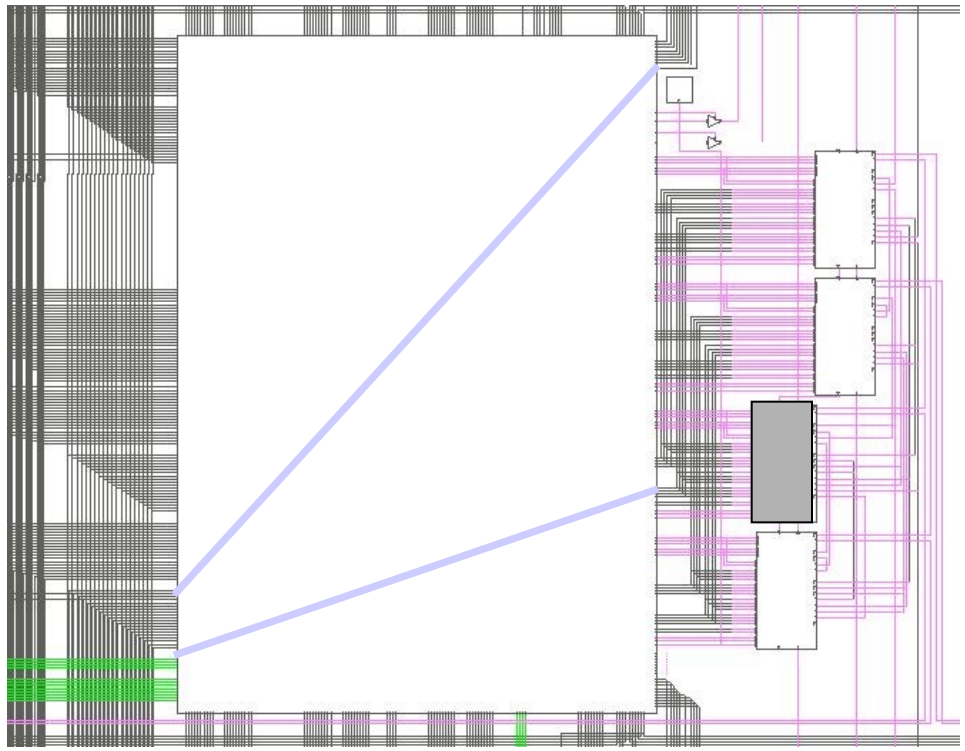




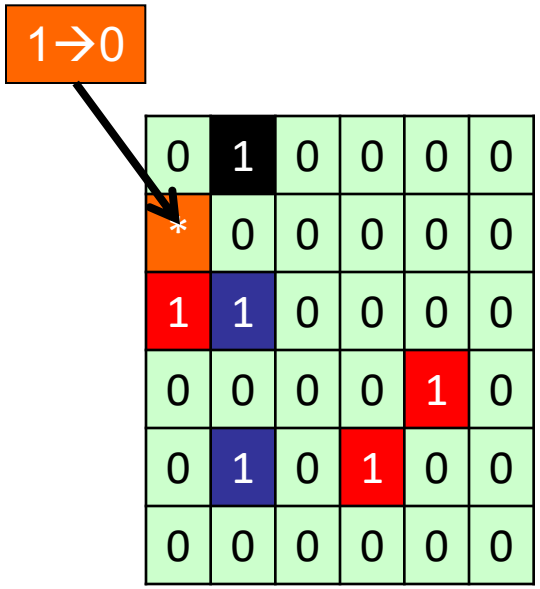
SEU effects in SRAM-based FPGA

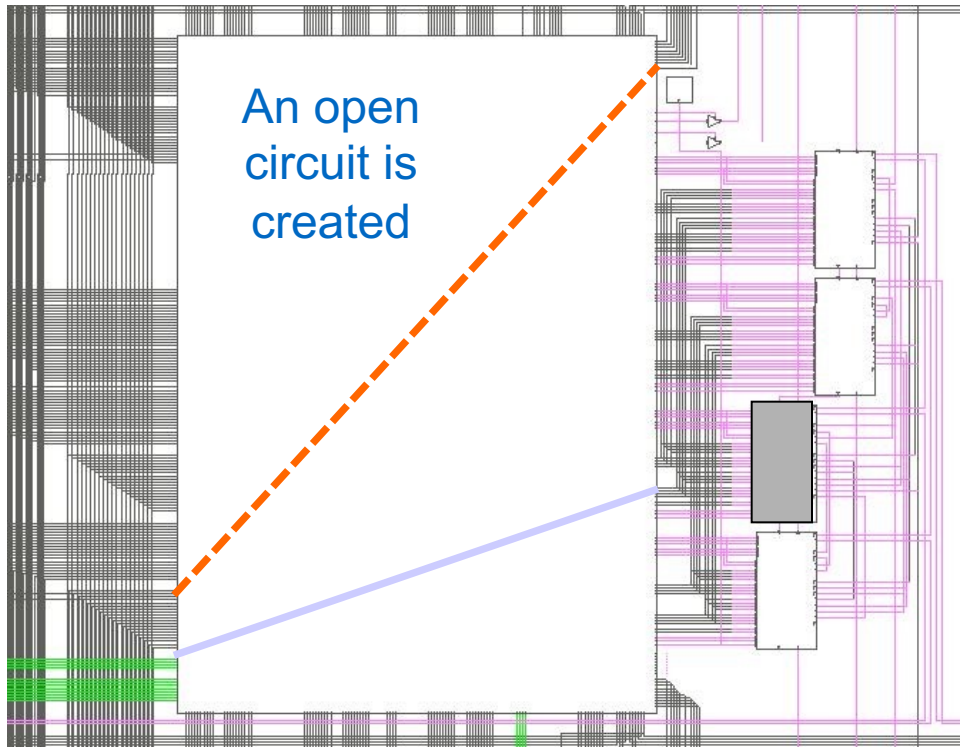
- Original configuration memory data, also called, bitstream
- An architectural configuration corresponds to an unique bitstream

0	1	0	0	0	0
1	0	0	0	0	0
1	1	0	0	0	0
0	0	0	0	1	0
0	1	0	1	0	0
0	0	0	0	0	0

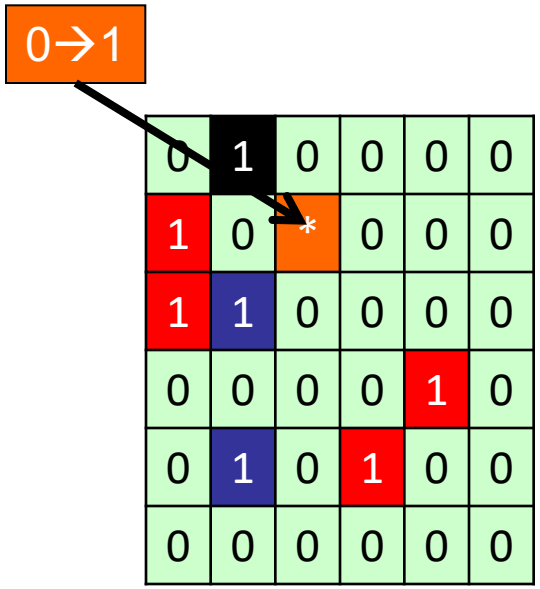


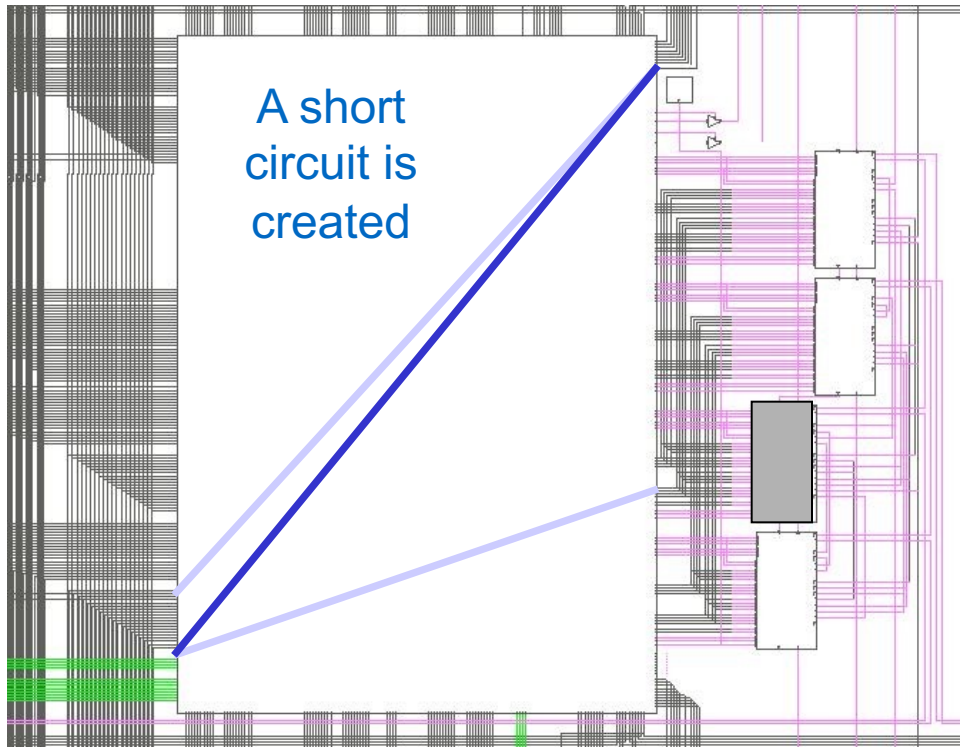
SEU effects in SRAM-based FPGA



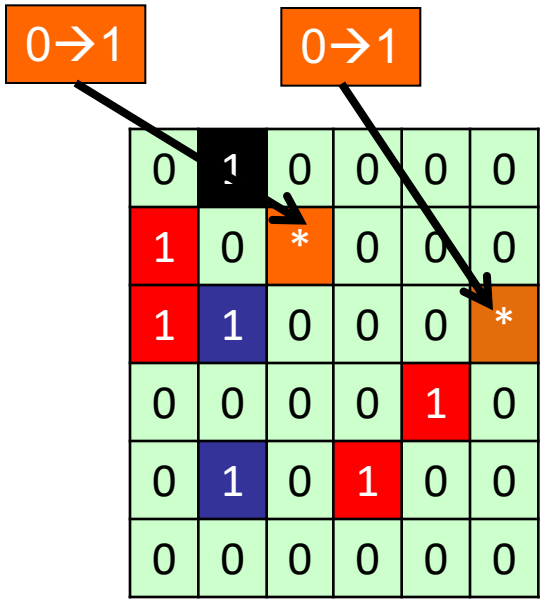


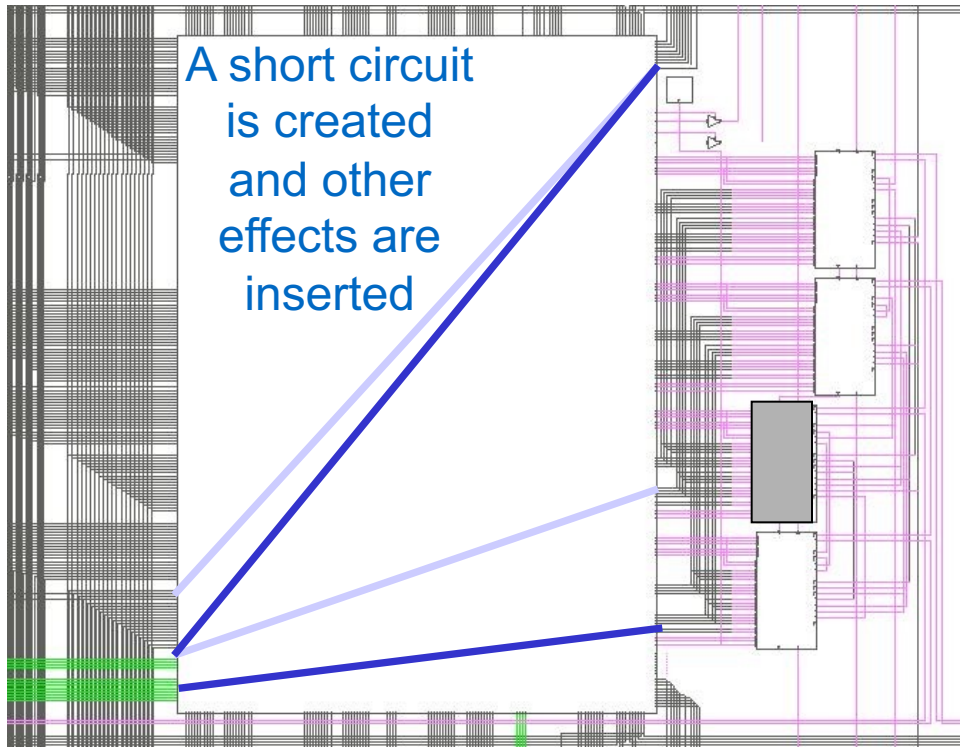
SEU effects in SRAM-based FPGA





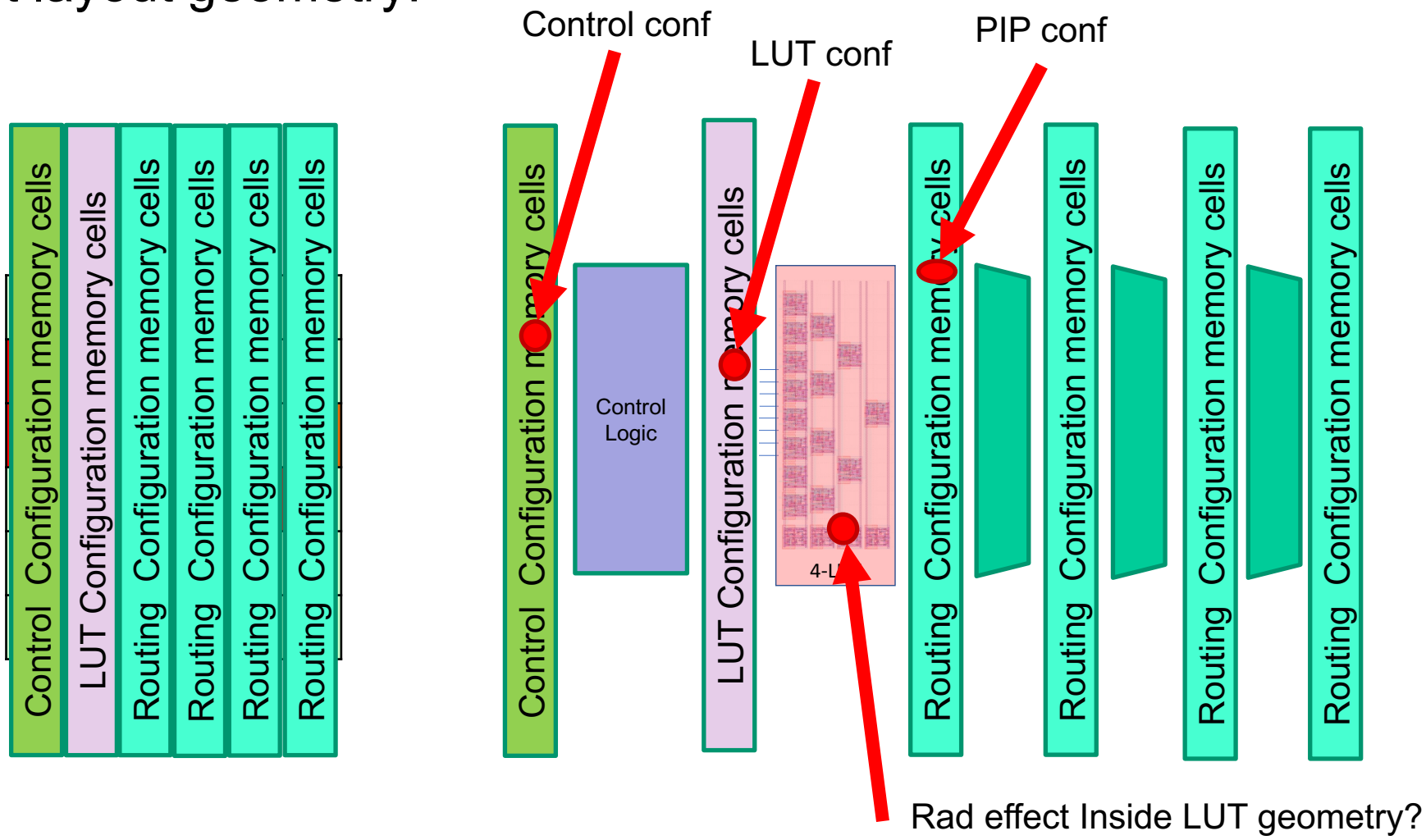
SEU effects in SRAM-based FPGA





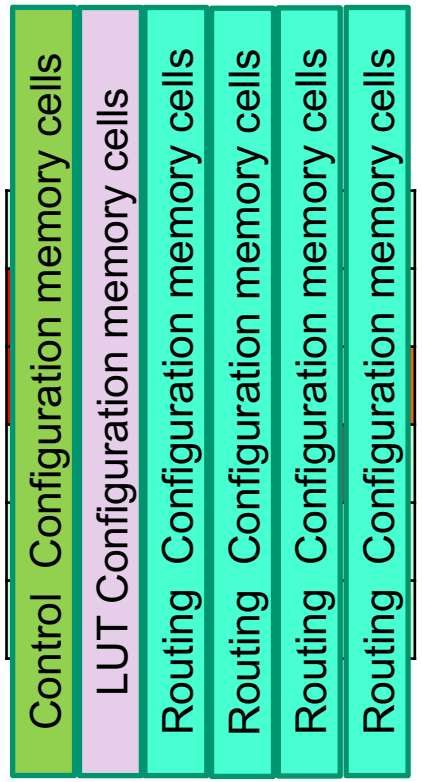
SEU effects in SRAM-based FPGA

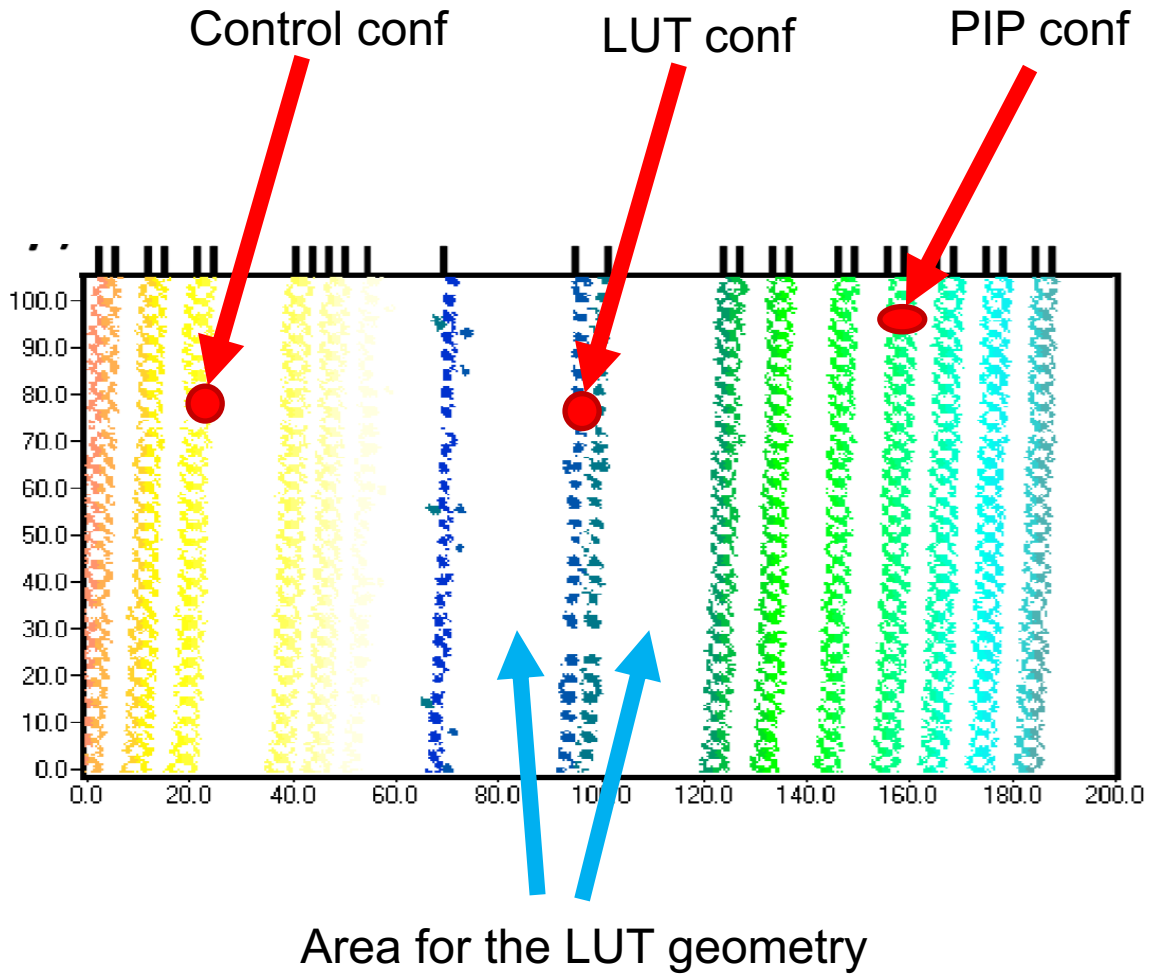
- Configuration memory frames are interleaved with layout
- Don't forget layout geometry!



SEU effects in SRAM-based FPGA

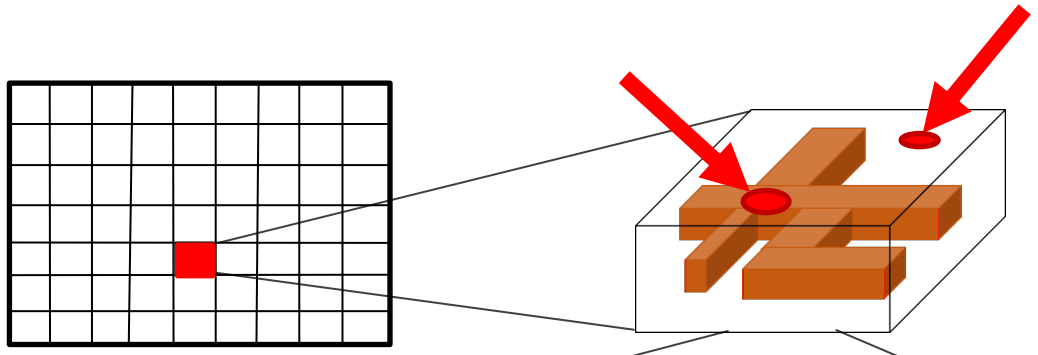
- A laser-induced SEUs on the configuration memory of a Xilinx SRAM-based FPGA device (Virtex-II)



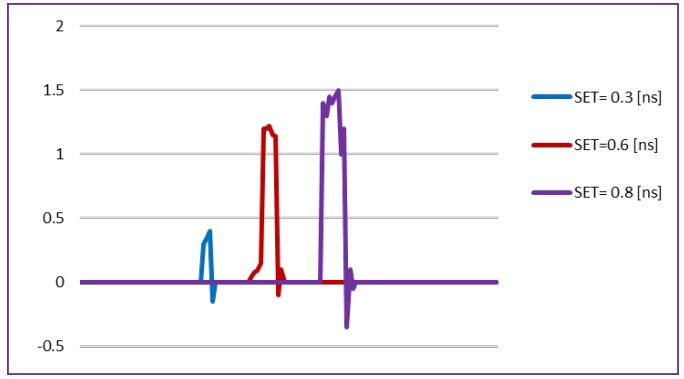


SET effects in FPGAs

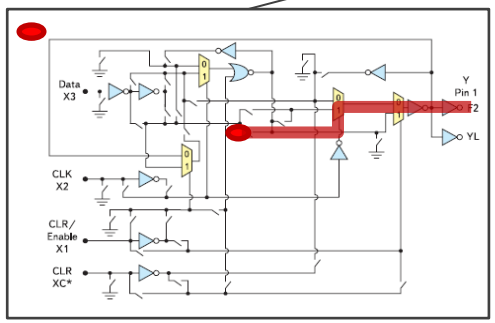
- A radiation particle hitting the geometry of a LUT/Logic Element may create a Single Event Transient pulse



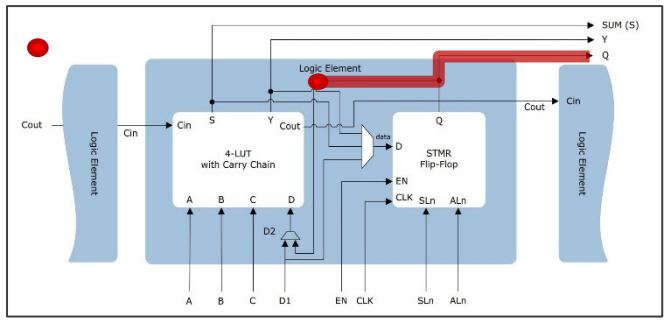
FPGA array



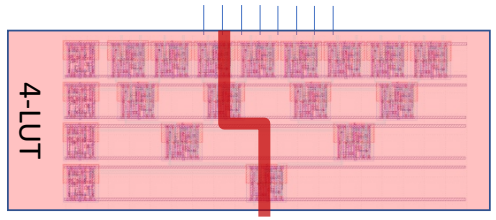
Examples of transient pulses generated by particle incident



Versatile of ProASIC3 (Actel)



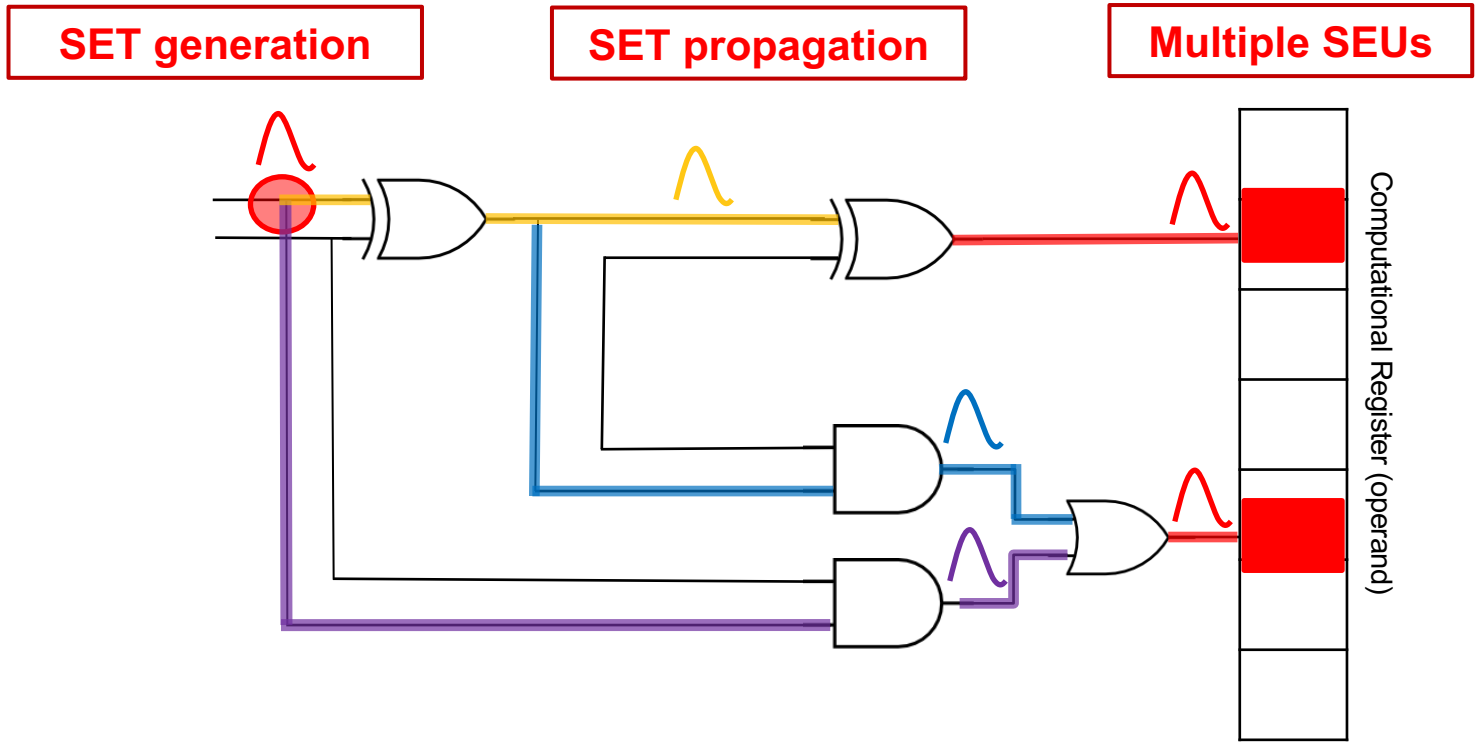
Logic Element of RTG4 (Microchip / Microsemi)



LUT-based (Xilinx and Altera)

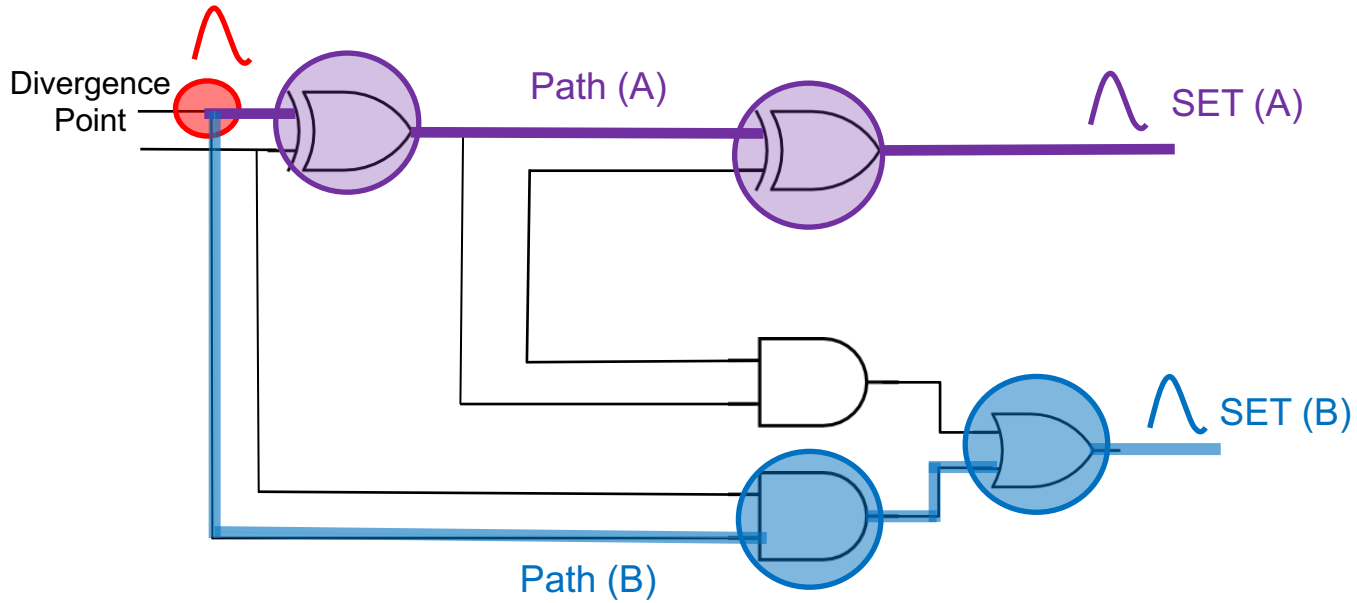
SET effects in SRAM-based FPGA

- SET may propagate through multiple circuit paths
- Generation of **Multiple SEUs** on registers

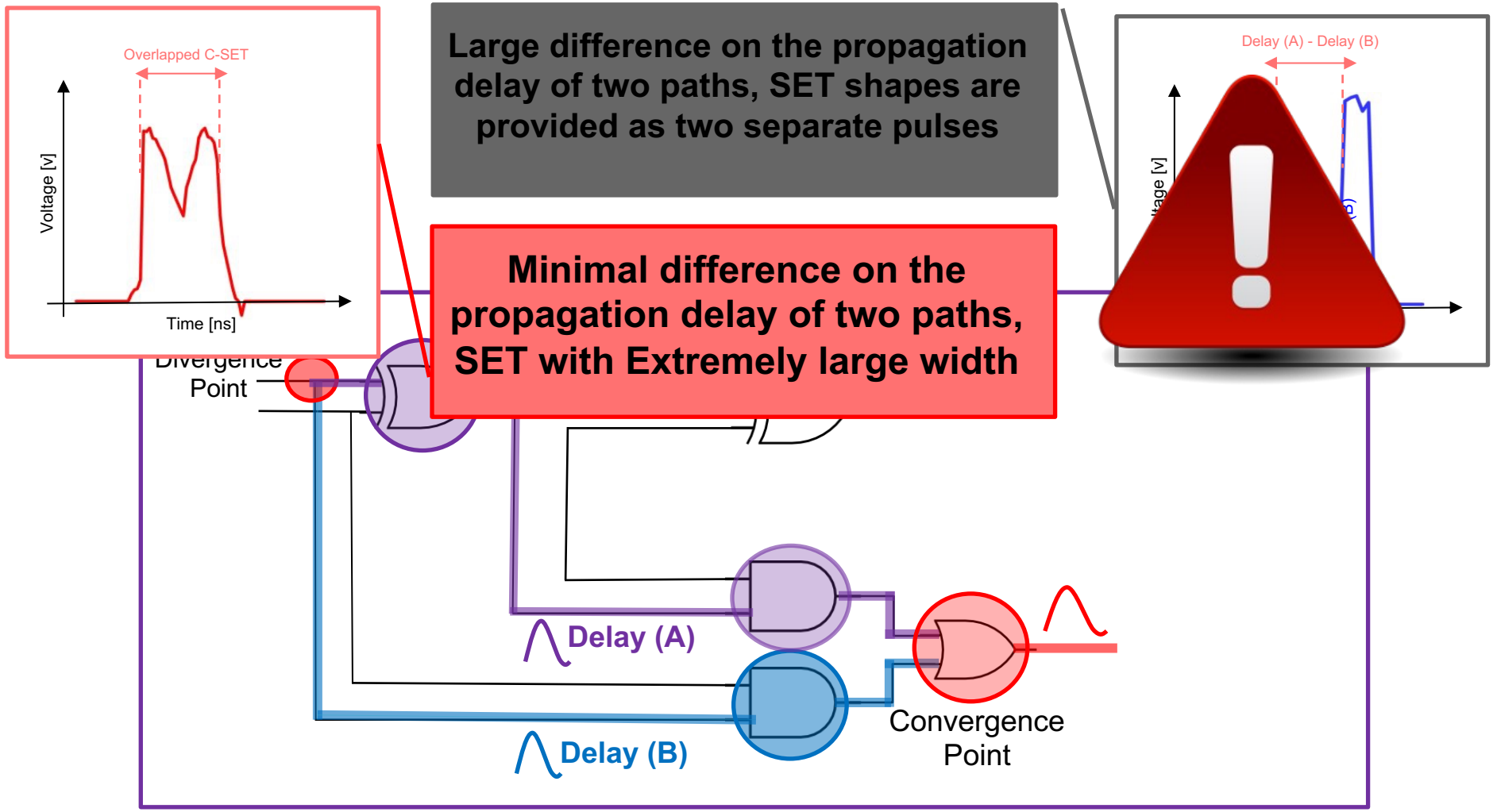


SET effects in SRAM-based FPGA

- During propagation SET may have a modified width and amplitude
- Propagation of SET pulse from a divergence point to different destination points

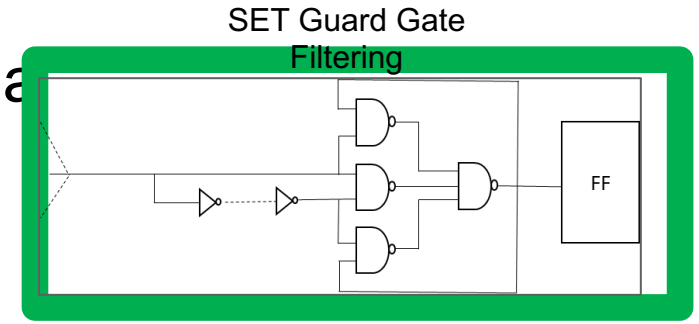


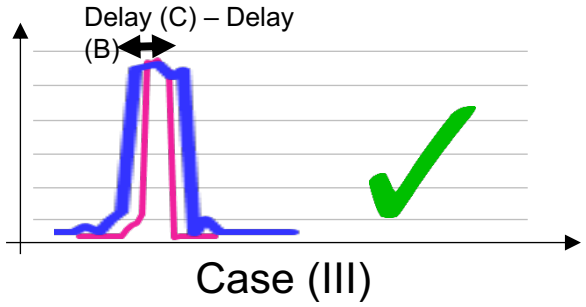
SET effects in SRAM-based FPGA

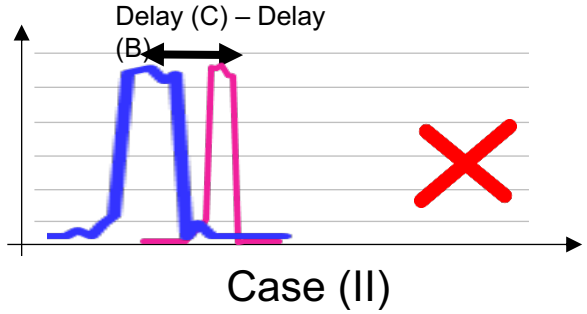


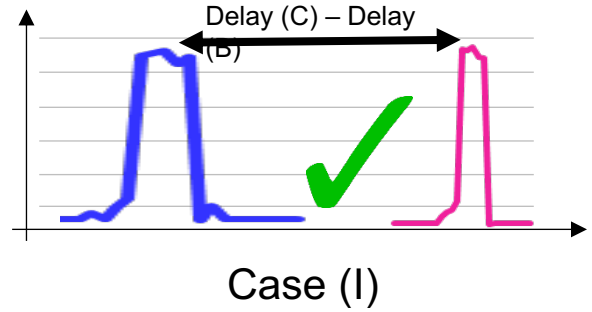
SET effects in SRAM-based FPGA

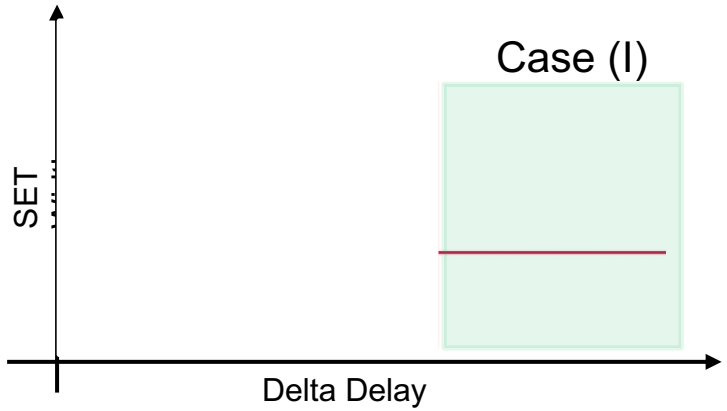
- The convergence SET (C-SET) phenomena











[RADECS18]

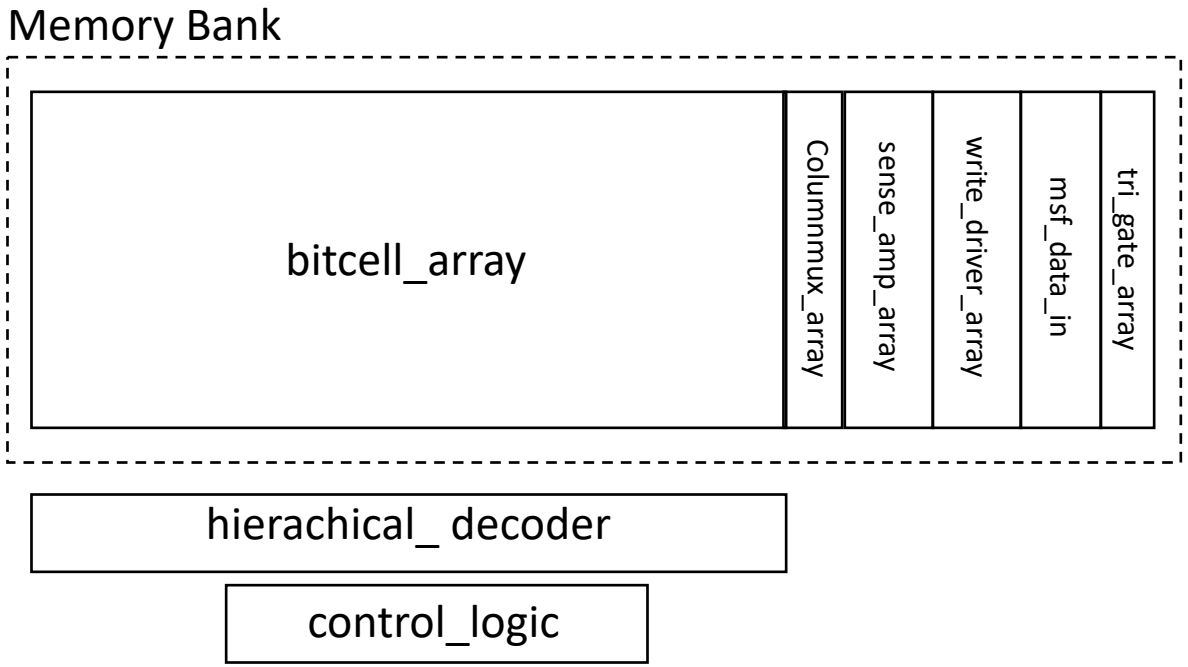
SEE mitigation techniques

- Hardening techniques are applied:
  - layout: modifying the device geometrical layout
  - architecture: modifying one or more module of the architecture
  - design: improve the HW/SW design rule to be rad-tolerant

- Some SEE mitigation techniques on ASIC have been consolidate over the time:
  - Layout (DICE)
  - Architecture (EDA)
  - Design (TMR)

SEE mitigation techniques: layout

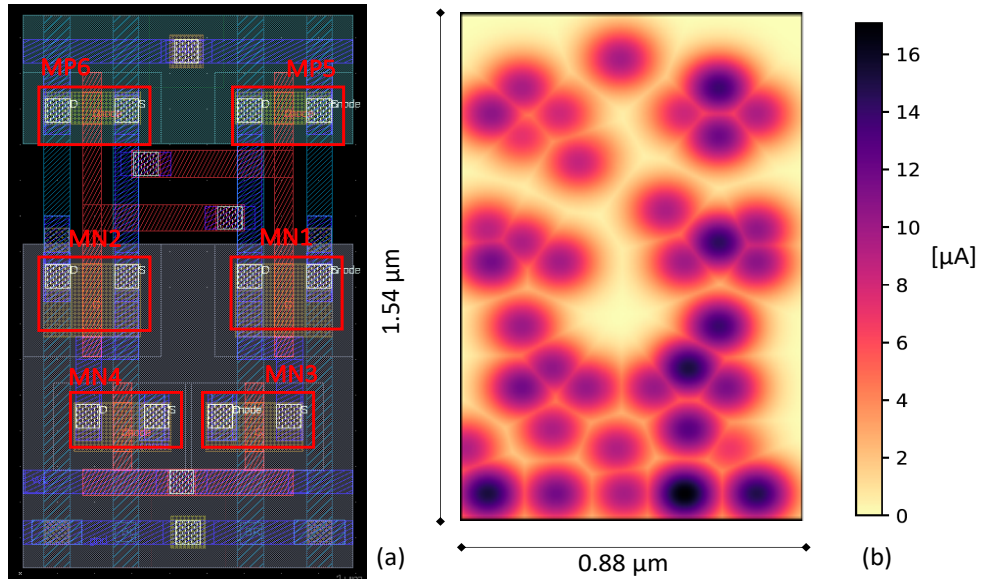
- **The hierarchical blocks of the memory bank are based on six main logic cells:**
  - Data Flip-Flop (DFF)
  - Master and Slave Flip-Flip (MS-Flop)
  - Write Drivers
  - Three states buffer
  - Sense Amplifier
  - 6 Transistors RAM cell
- **Hierarchical decoder and control logic**
  - outside of the memory bank
- **The memory bank cells have been analyzed with 10,000 particles per each heavy ions using the 3D simulation approach**

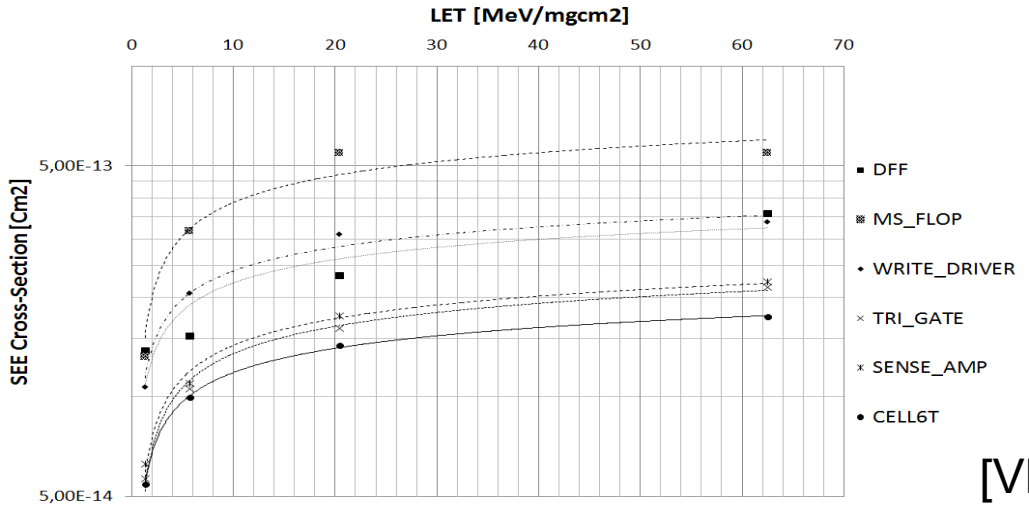


[VLSISoC21]

SEE mitigation techniques: layout

- **The SEE cross-section may vary from $5.44 \cdot 10^{-14}$ up to $5.46 \cdot 10^{-13}$**
- **Distribution of the current pulses observing that 96.62% of the radiation particle**
  - over the 40,000 particles are generating current pulse below 0.5 μA
- **Maximal peak of 17.4 μA**
- **DFFs and the MS-Flops are the most sensitive cells**
- **6T-RAM cell is the cell with the lowest cross-section**

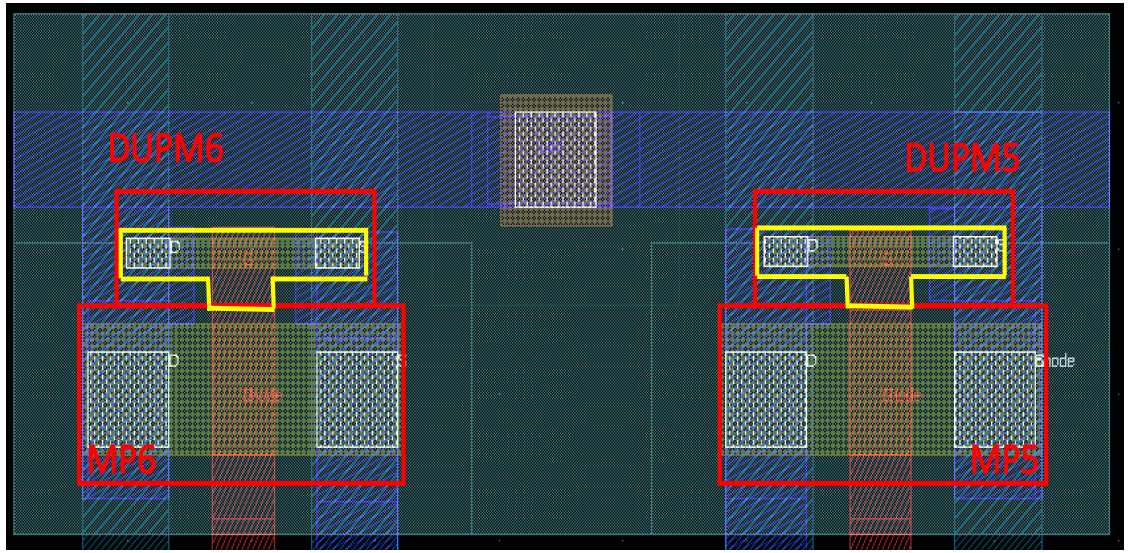


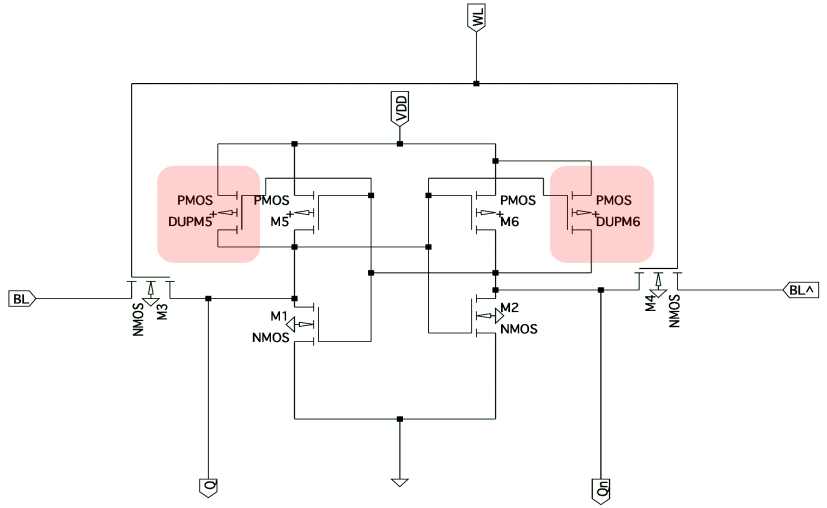


[VLSISoC21]

SEE mitigation techniques: layout

- **The main purpose of our approach is to insert two redundant transistors (DUP) in parallel to the original PMOS transistors**
  - A ***T-structure*** added on the top of the original transistor
- **The radiation particle charge injected by those particles directly crossing MP5 and MP6 is distributed**
  - The overall **Q_{crit} margins are increased**
- **The modified the 6T-SRAM original layout available regions without introducing area overhead to the cell**
  - MP6 and MP5 transistors have enough physical space to introduce to redundant transistors



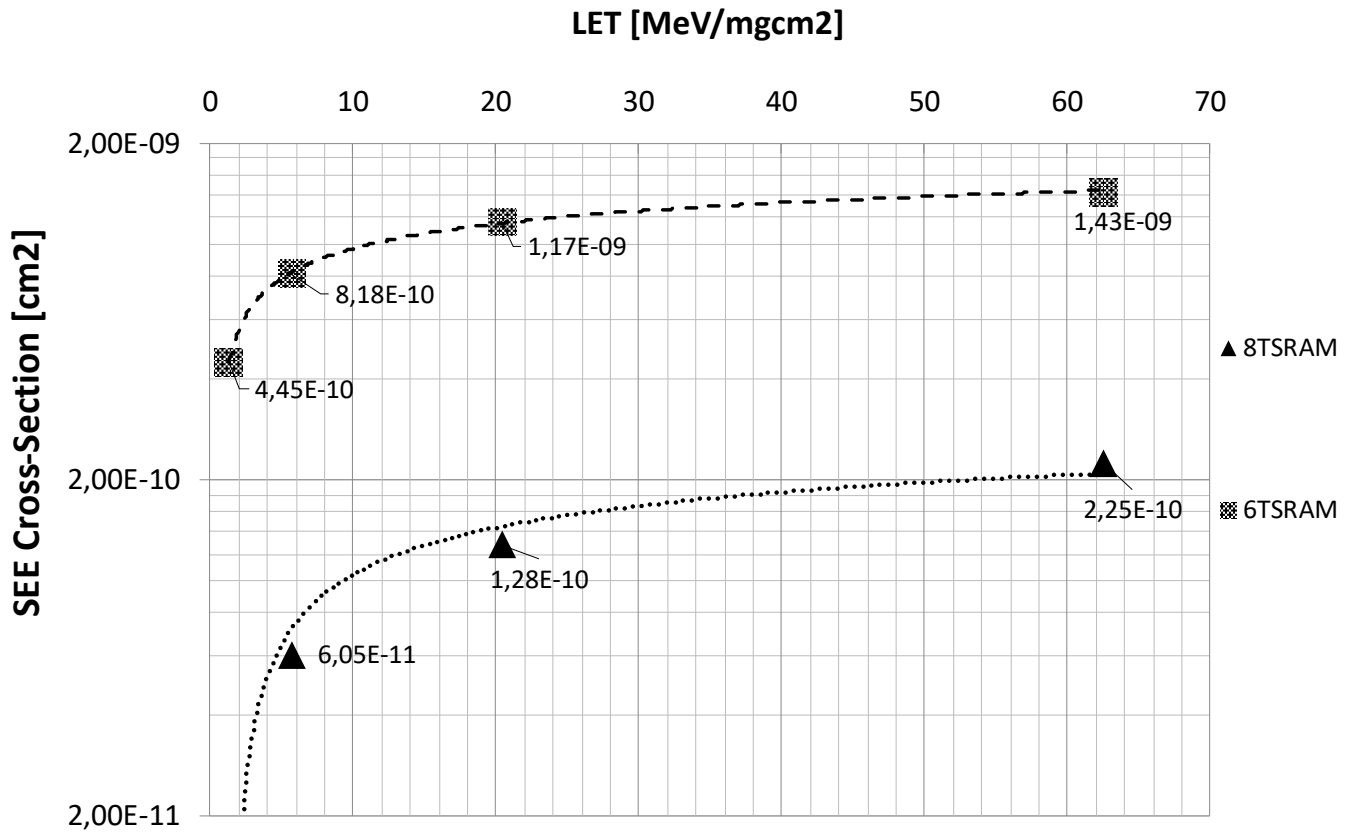


[VLSISoC21]

SEE mitigation techniques: layout

SRAM Configuration	SEE Threshold Current Pulse [μA]	
	Q=1 Q_n=0	Q=0 Q_n=1
6T-Original	0.93	0.46
8T-Proposed	3.83	2.12

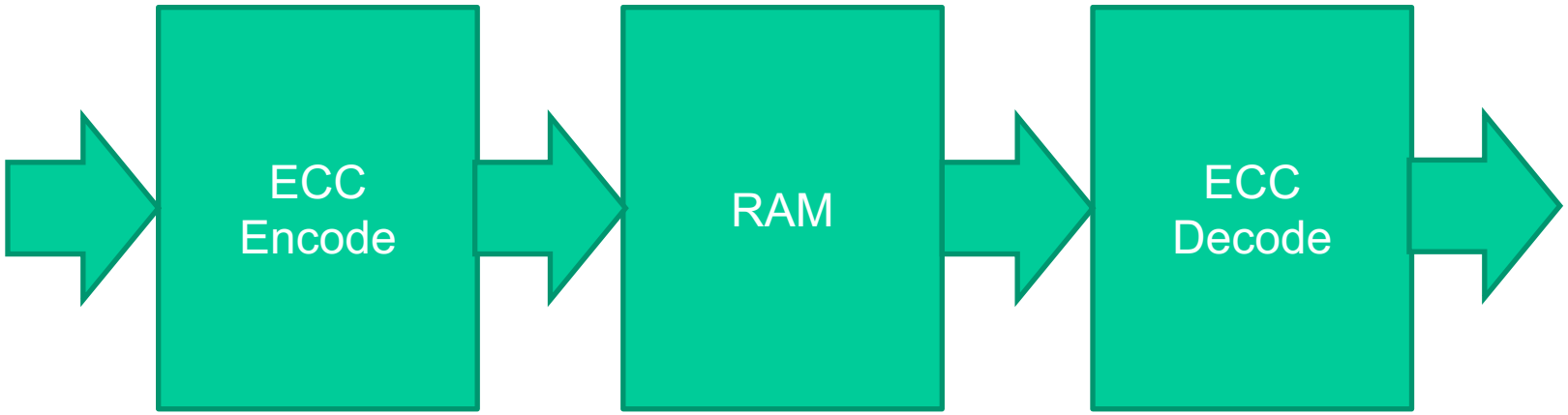
- **8Kb memory bank with the 8T-SRAM cell**
- **The developed mitigated 8T-SRAM is 6 times more robust of the original 6T-SRAM cell**



[VLSISoC21]

SEE mitigation techniques: architecture

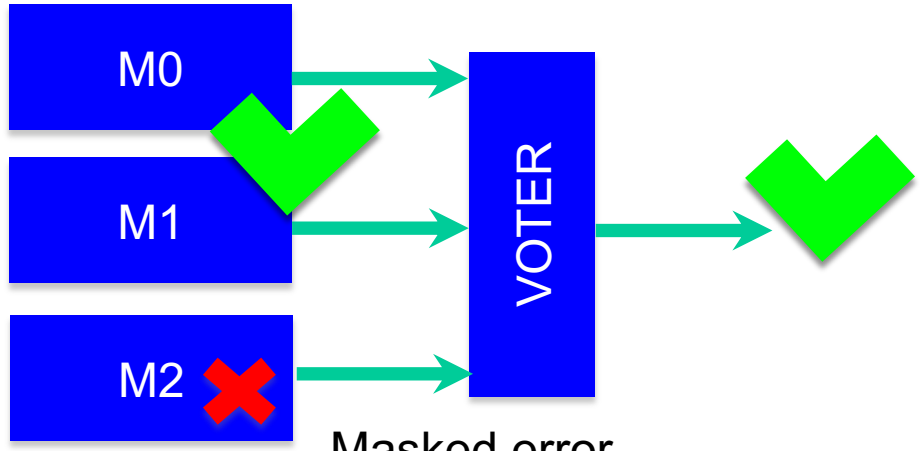
- Error Detection and Correction: **EDAC**
- An error-correcting code (ECC) or forward error correction (FEC) is a process to add redundant data (parity data) to a message
- The error can be recovered by a receiver even when a number of errors are introduced
- Applied to RAM modules



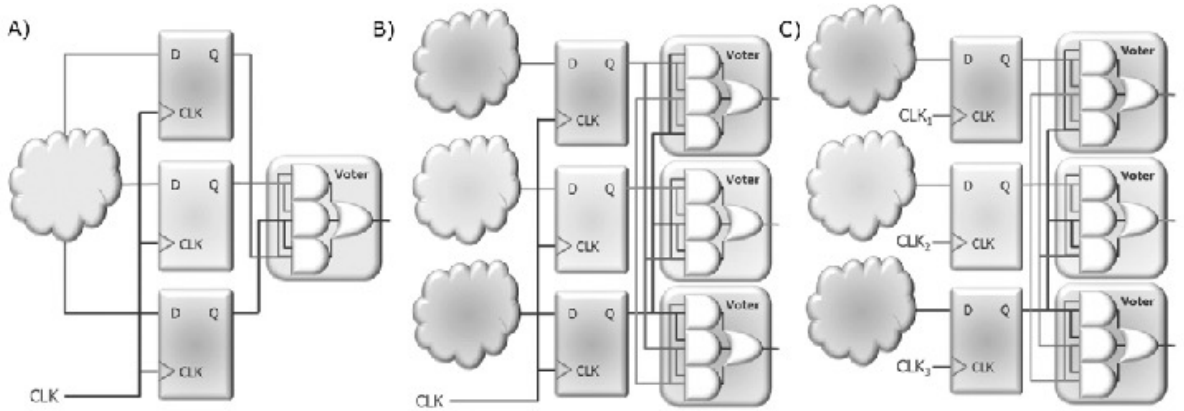
Hsiao, M.Y. "A Class of Optimal Minimum Odd-Weight-Column SEC-DED Codes".
IBM Journal of Research and Development
14, no. 4 (July 1970). Available from World Wide Web:
Lin, Shu and Daniel J. Costello, Jr. Error Control Coding: Fundamentals and Applications.
New Jersey: Prentice Hall, 1983.

SEE mitigation techniques: architecture

Triple Modular Redundancy



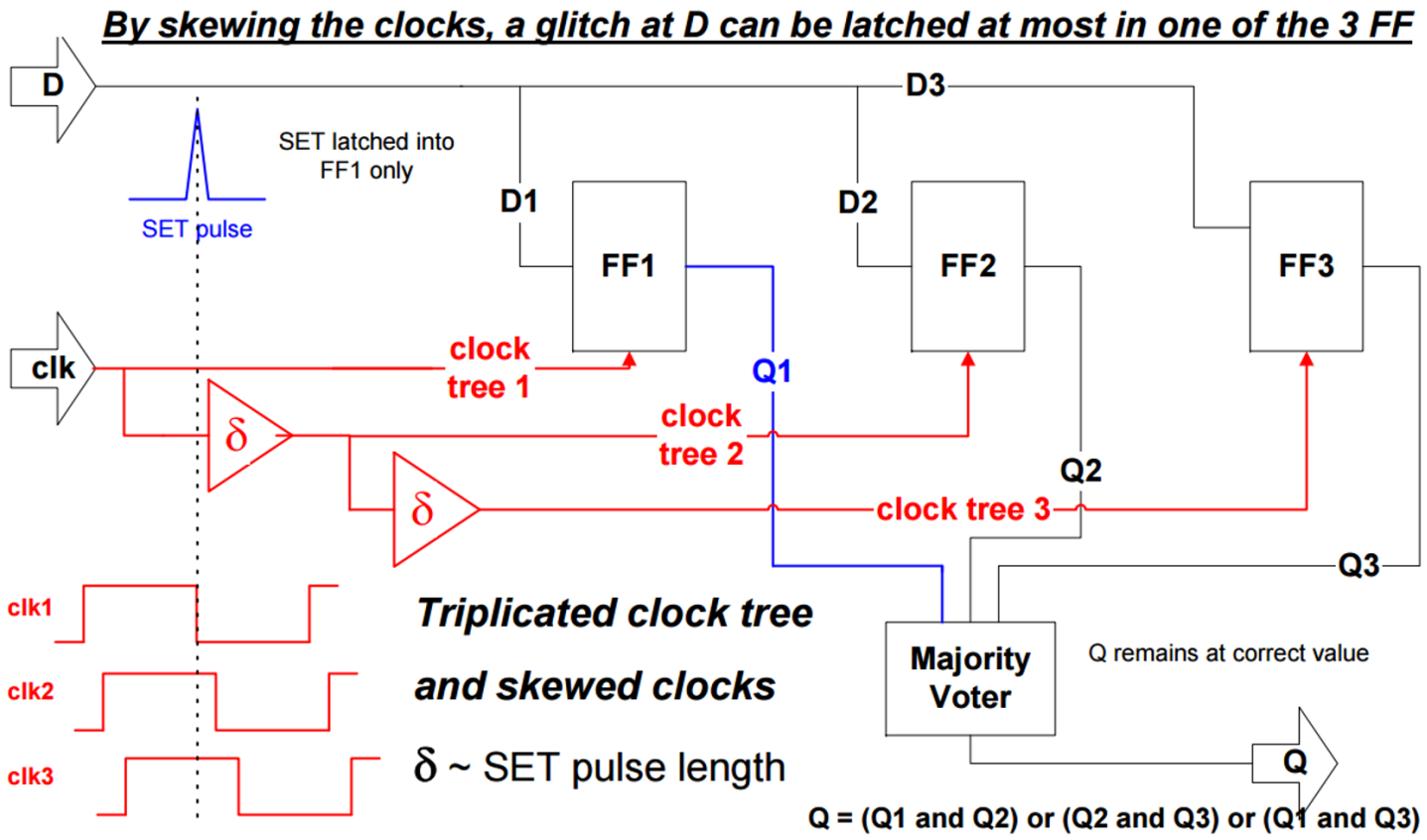
Masked error



[Courtesy of A. Menicucci]

W. G. Brown, J. Tierney and R. Wasserman, “Improvement of Electronic- Computer Reliability Through the Use of Redundancy.” IRE Trans. on 2. G. Buzzell, W. Nutting and R. Wasserman, “Majority Gate Logic Improves Elec. Comp., EC-IO, No. 3, 407 (1961).

SET mitigation techniques: clock skew

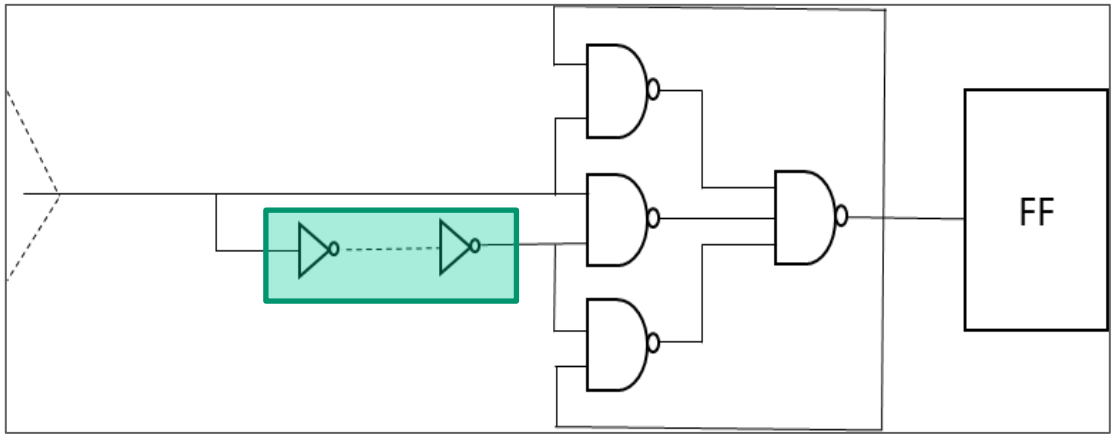


[From European Space Agency presentation]

SET mitigation techniques: guard gate

- Filtering transient pulses by INV delay at the input of a guard gate logic gate structure

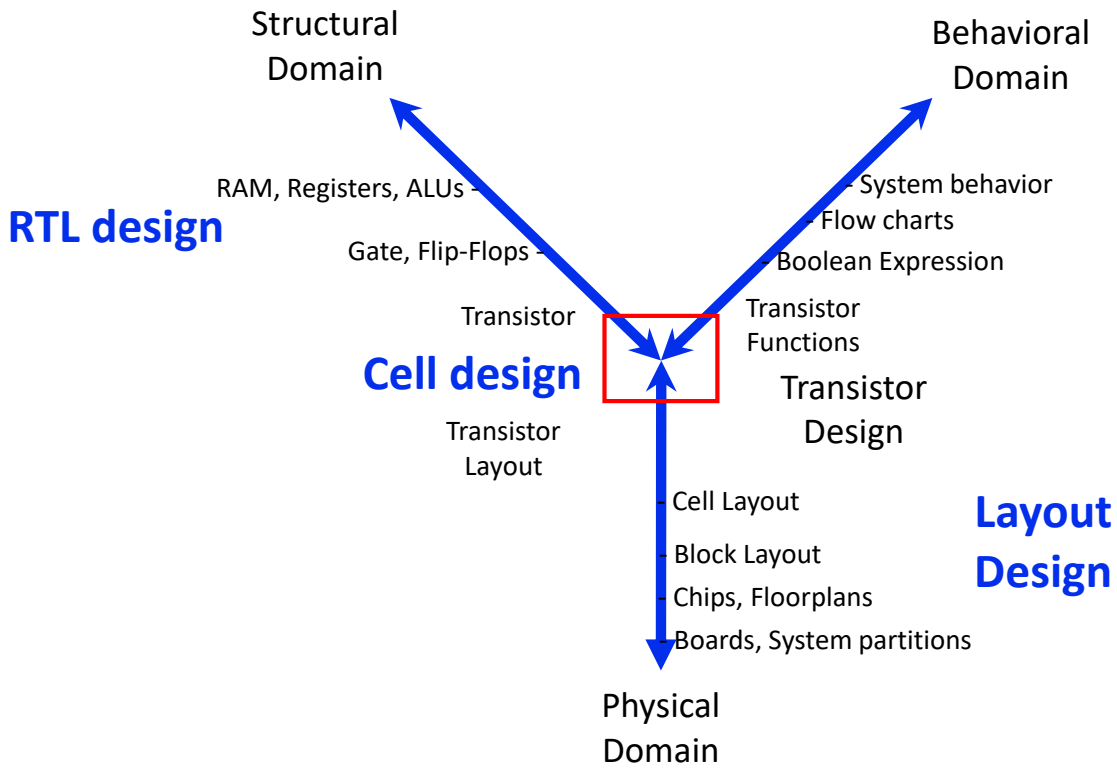
SET Guard Gate Filtering



[Mongkolkachit, P., et. al., IEEE Transactions on Materials Reliability, 2003]

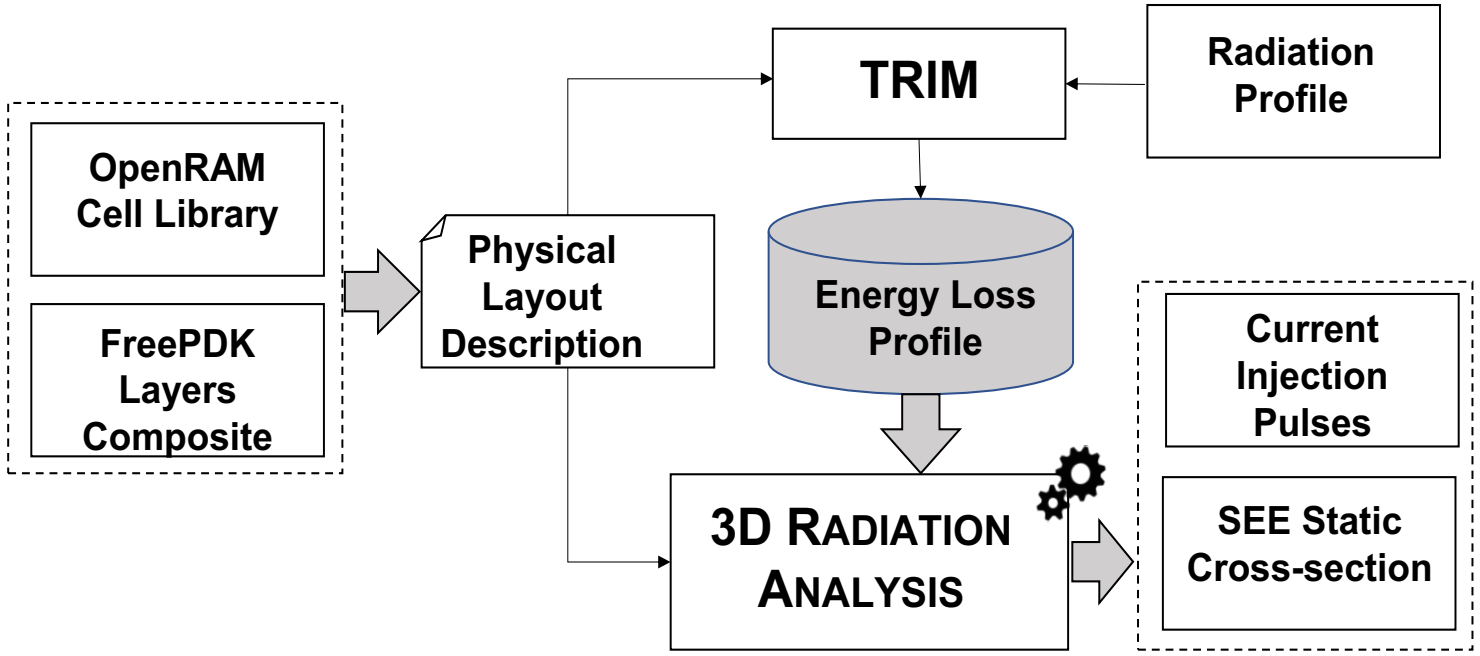
The need of CAD tools

- A new Radiation-oriented CAD tool paradigm focusing on radiation analysis and mitigation



Radiation Sensitivity Tools

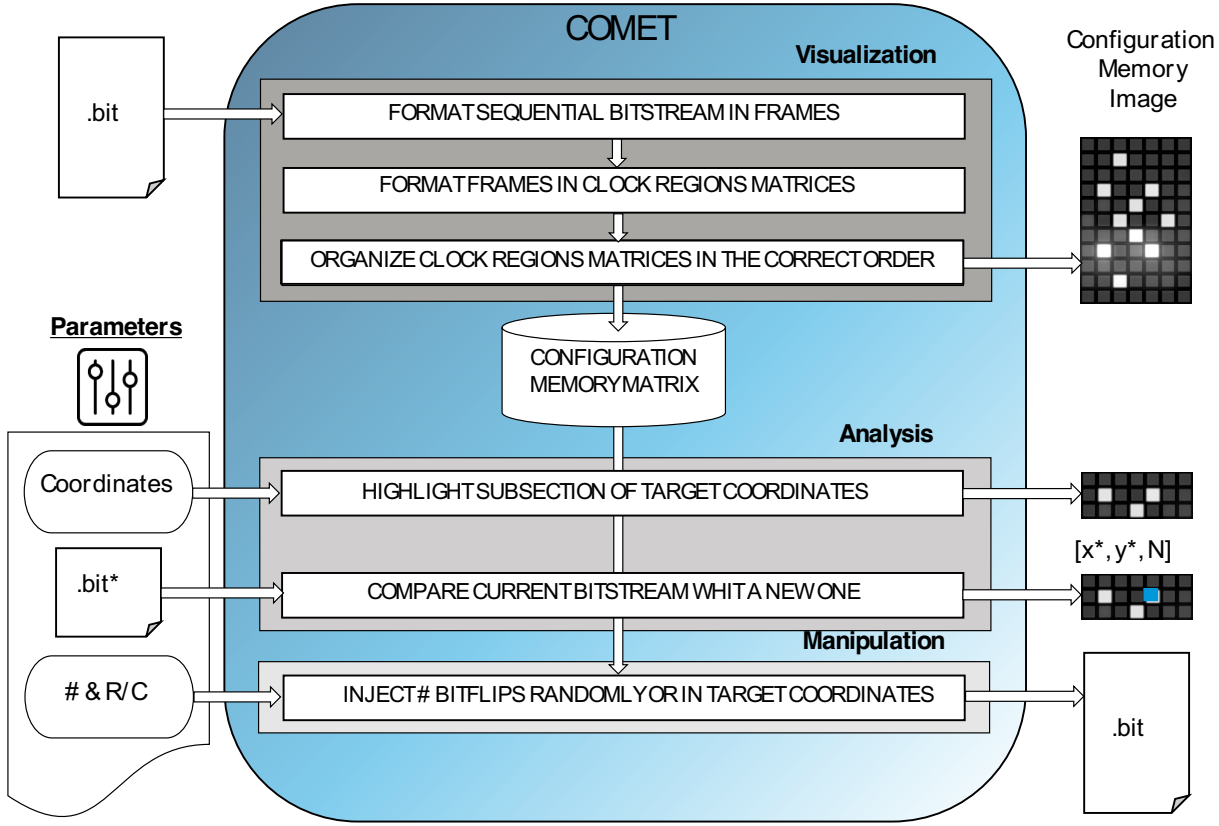
- **Radiation analysis tool simulates the effects of highly charged particles traversing the silicon junction**
  - Calculate the generated eV transmitted to the Silicon
  - Provide the current profile for each particle strike



[IEEE TNS 2019]

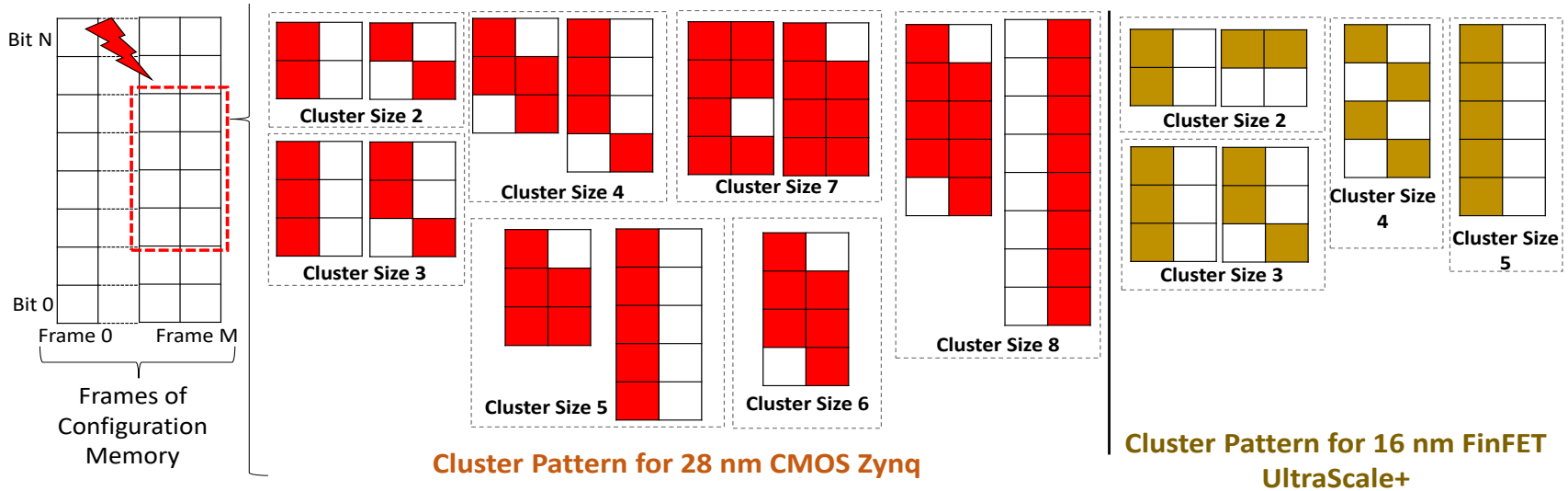
CAD tools for SEE analysis

- Configuration Memory Tool (COMET) for SRAM-based FPGAs
- A CAD tool to link the lowest level beween Physical Resource and Configuration memory layers
  - Compatible with Xilinx 7-series



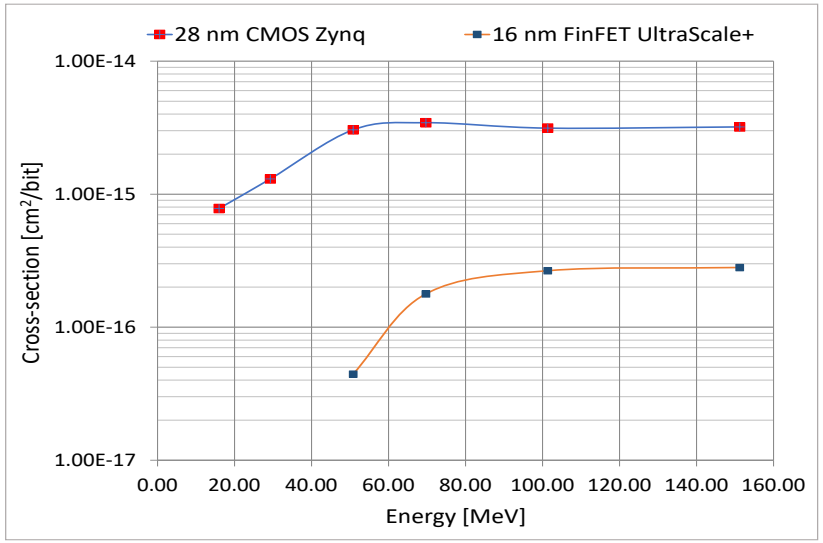
[ACM ARCS CompSPACE 2018]

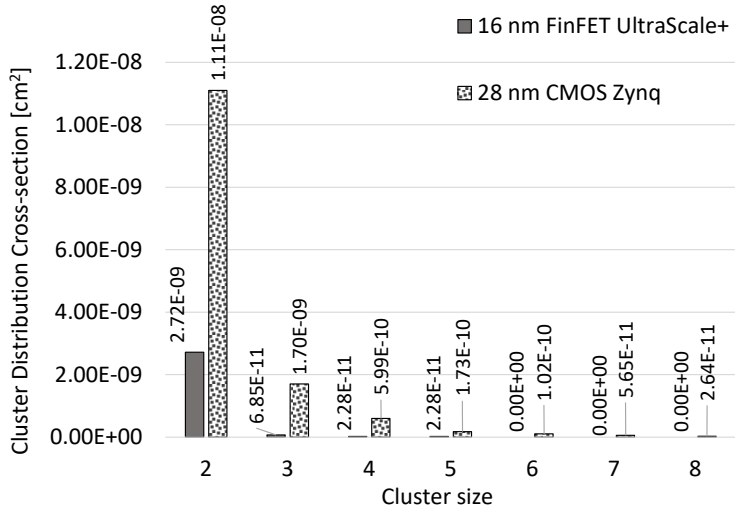
CAD tools for SEE analysis

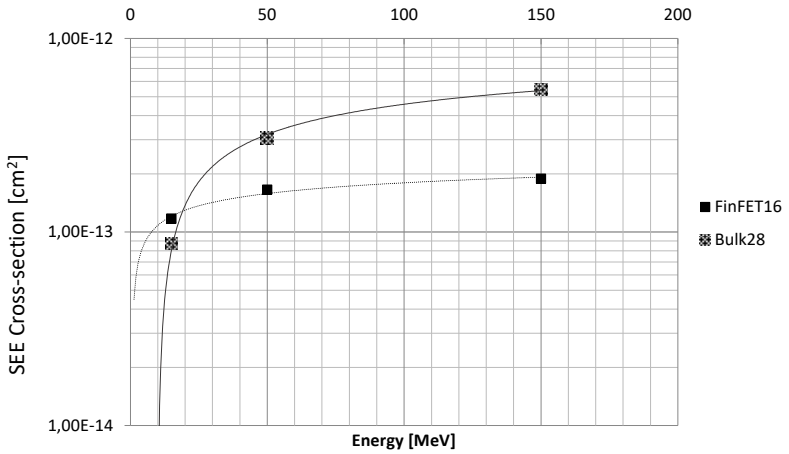


Cluster Pattern for 28 nm CMOS Zynq

Cluster Pattern for 16 nm FinFET UltraScale+



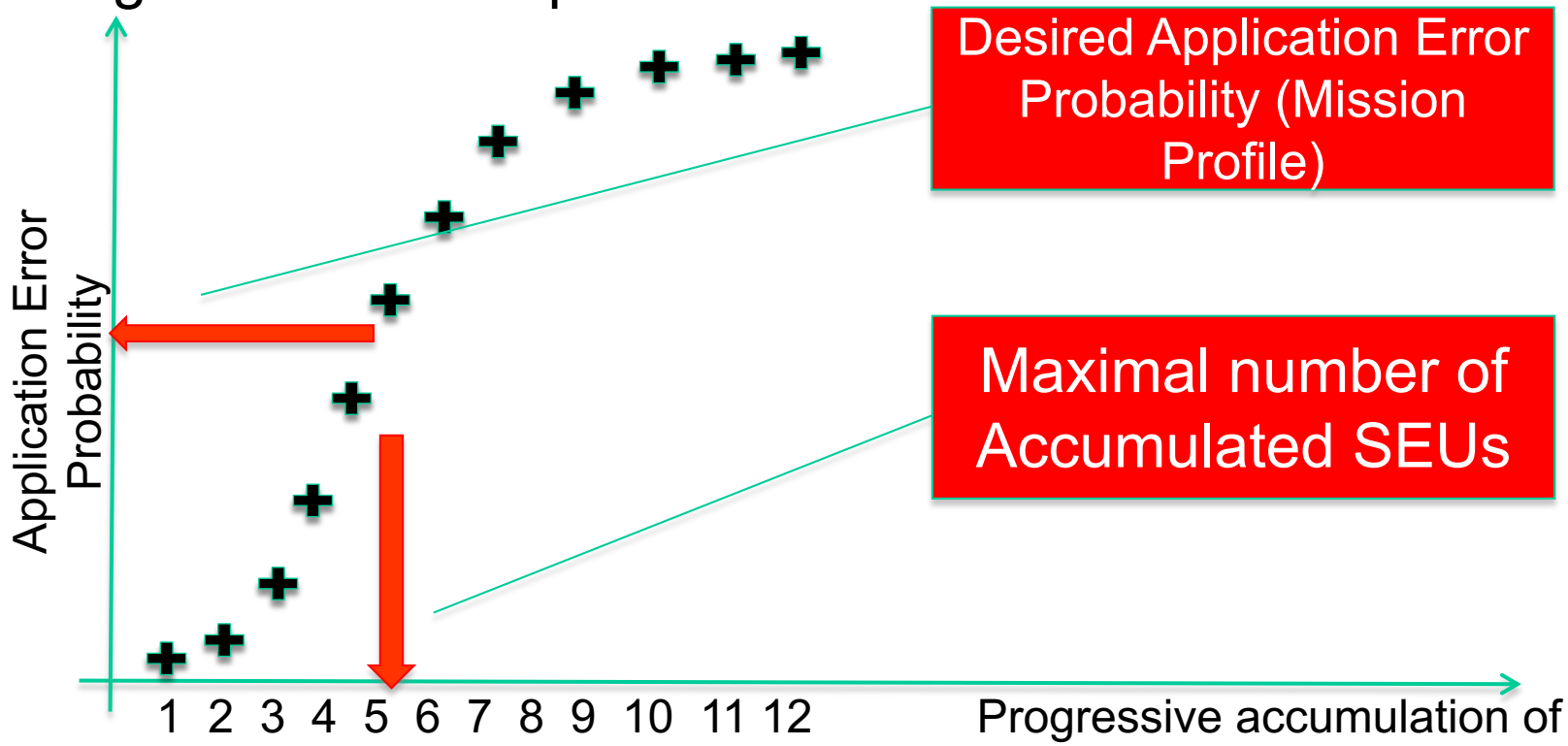




[Microelectronics Reliability 2022]

SEE mitigation techniques: architecture

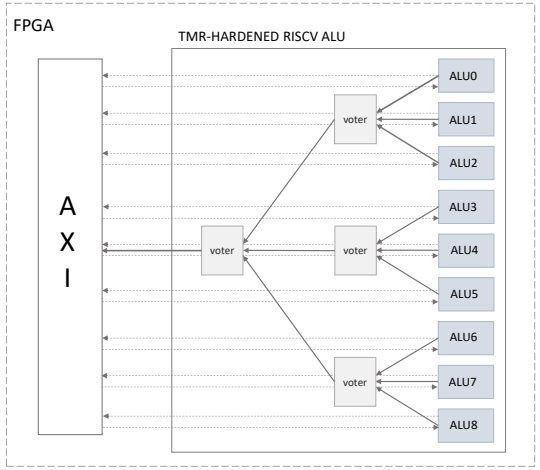
- VERI-Place is a CAD tool for analyze redundant (TMR-like) implementation on SRAM-based FPGAs
- Identification of all the architecturally relevant sensitive bits
- If affected, these configuration memory bits may change the physical structure of the circuit and generate an output error

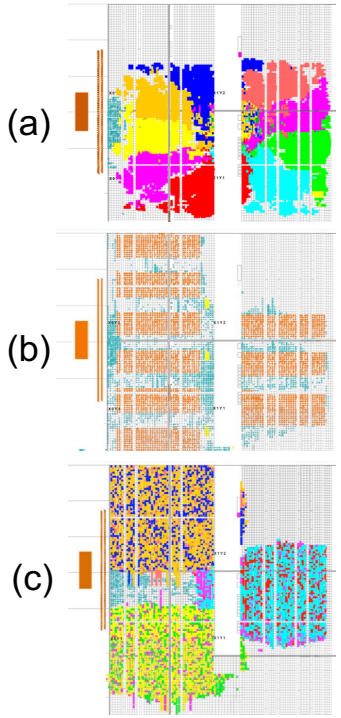


[RADECS22]

Experimental setup for SEU mitigation evaluation

- **AMD-Xilinx Zynq XC7Z020 28nm CMOS SRAM-based FPGAs**
- **The developed tool has been applied to a TMR benchmark**
- **Three different alternative layouts**

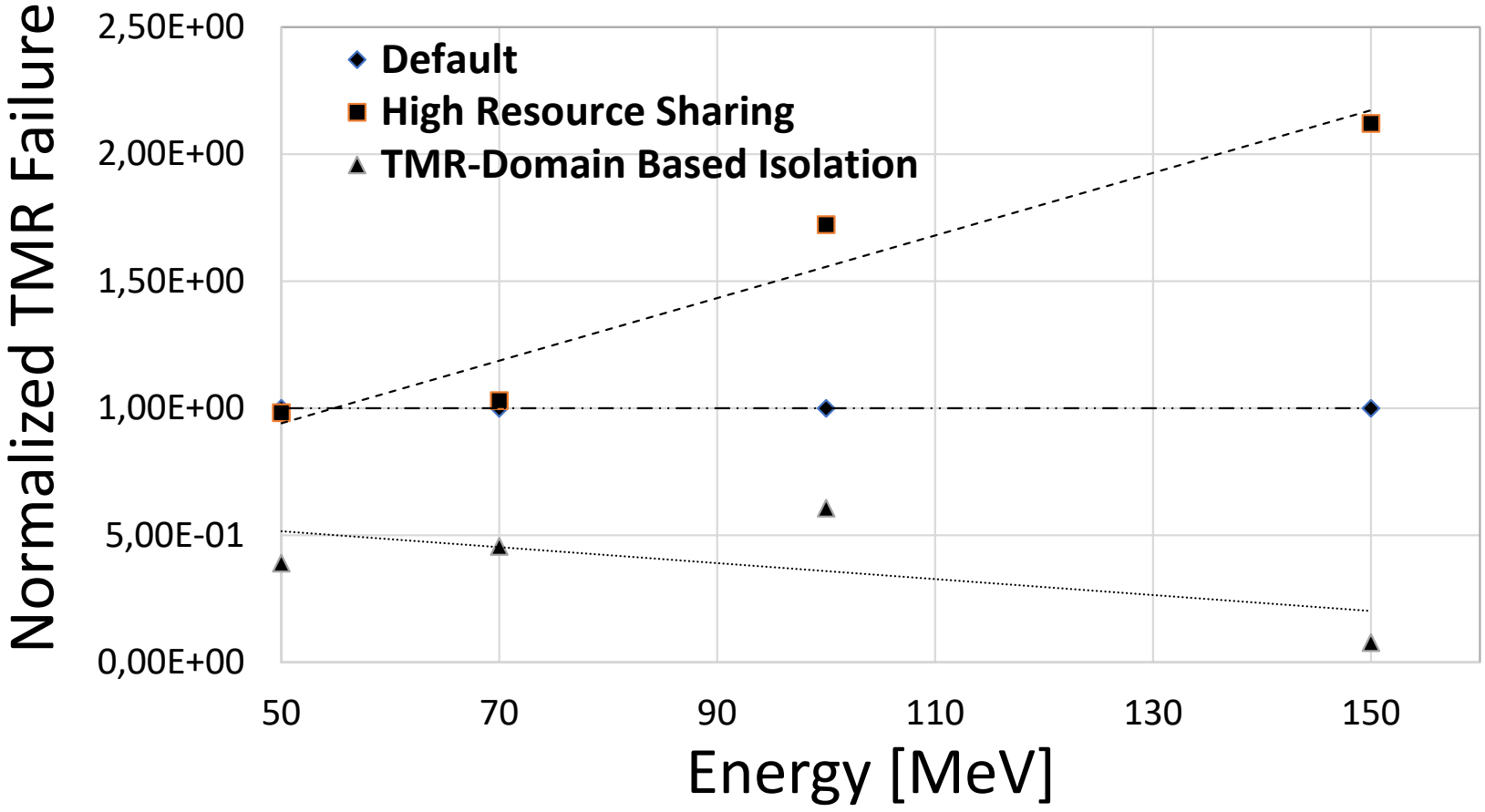




TMR design	LUT [#]	PIP [#]
(a) Original	11,572	13,590
(b) Isolated Domains	11,578	14,642
(c) Resource Sharing	11,572	24,948

Experimental results for SEU mitigation evaluation

- **Energies ranging from 50.80 MeV up to 150 MeV**
- **Average flux 4.134 10^7 proton·$cm^{-2}s^{-1}$**



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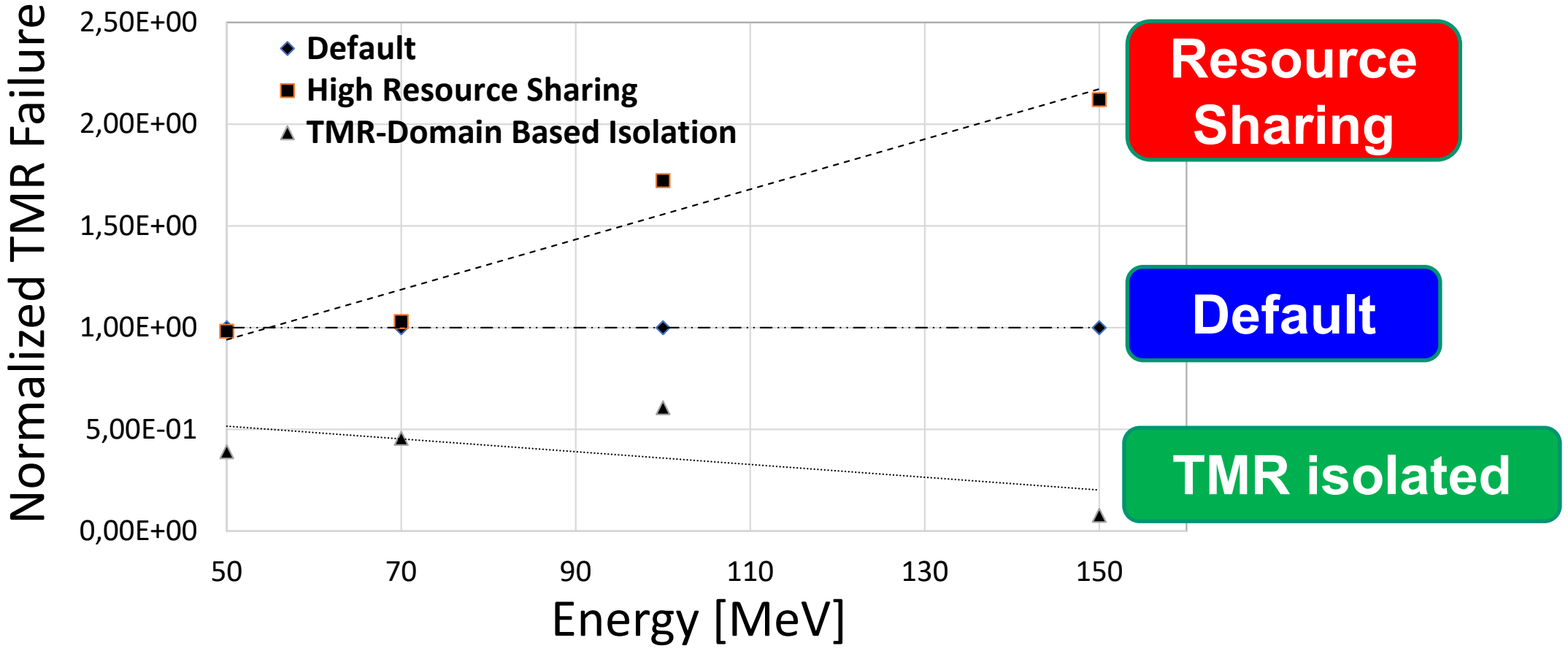
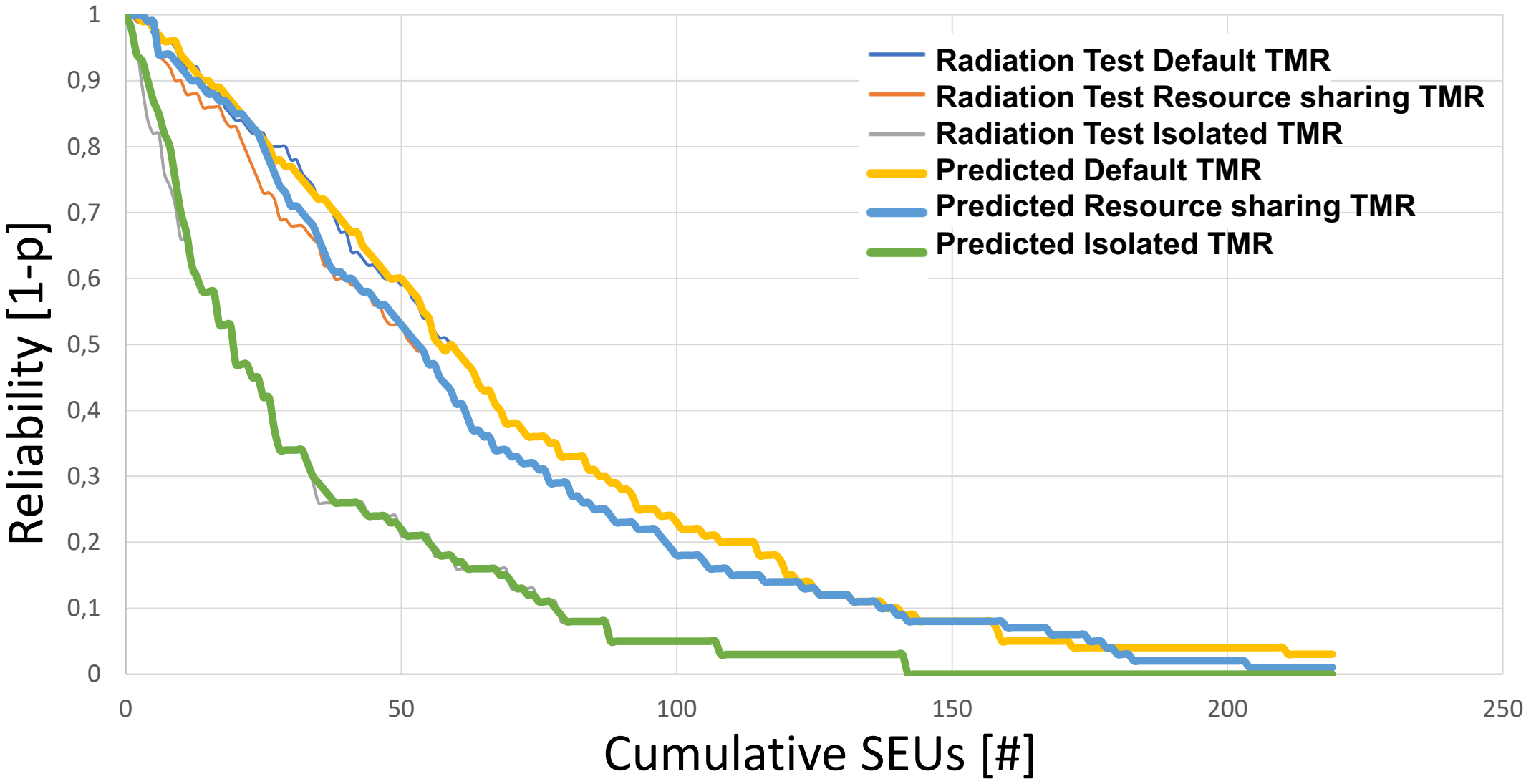
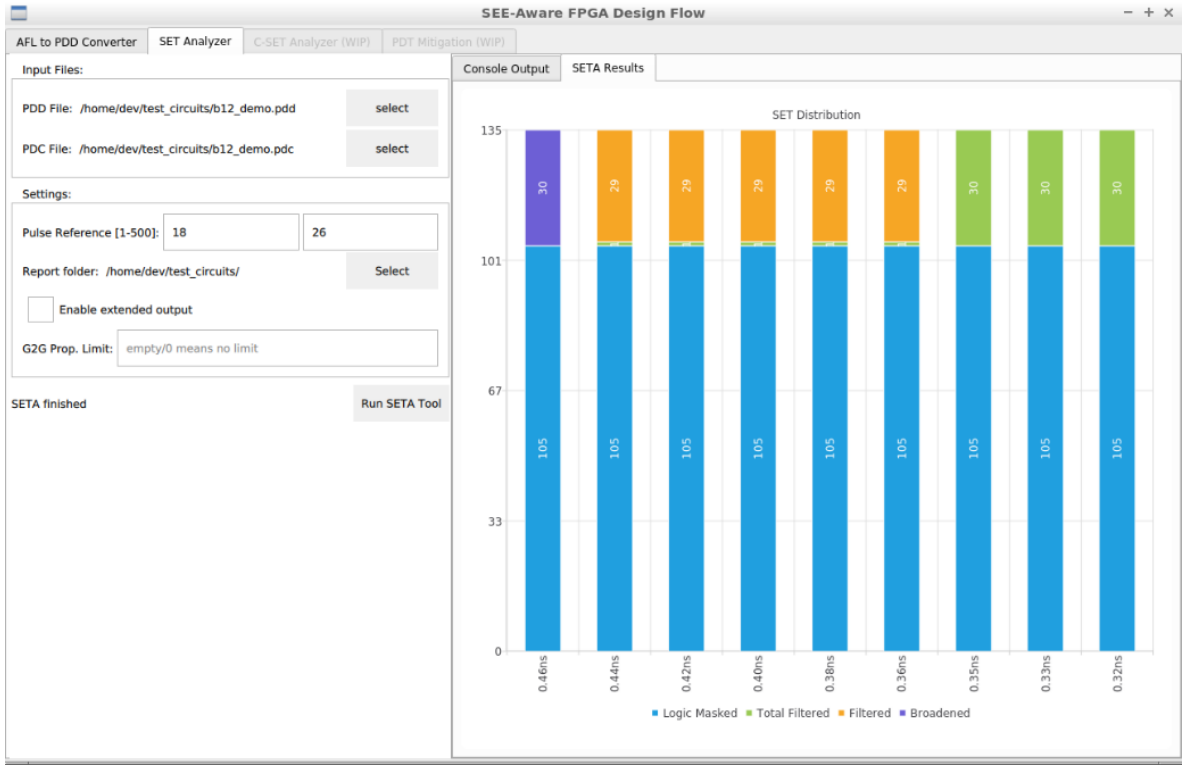


Predicted vs Measured Reliability



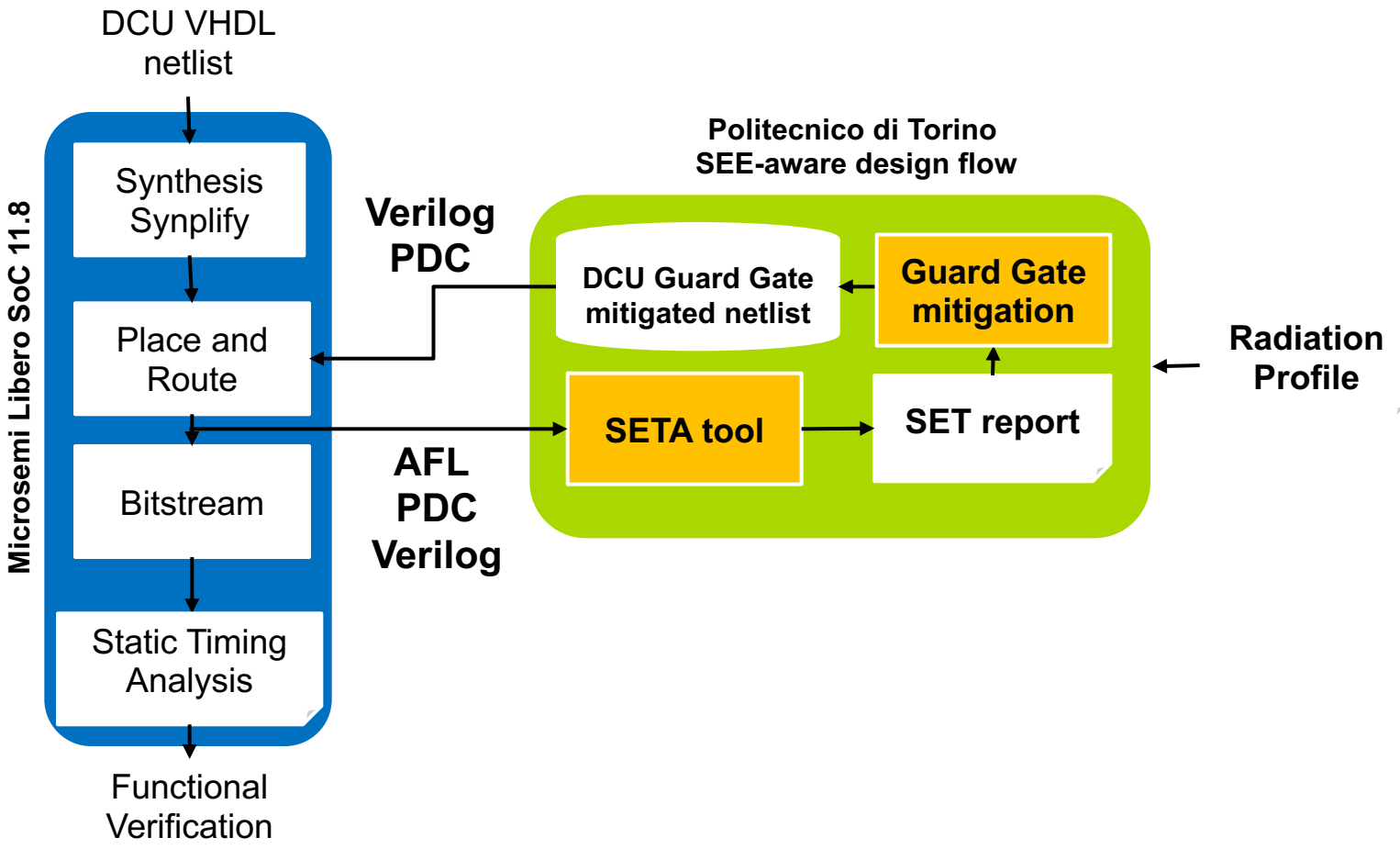
CAD tools for the SET analysis

- A Single Event Transient Analysis and Mitigation tool (SETA) for SET analysis and mitigation on Flash-based FPGAs

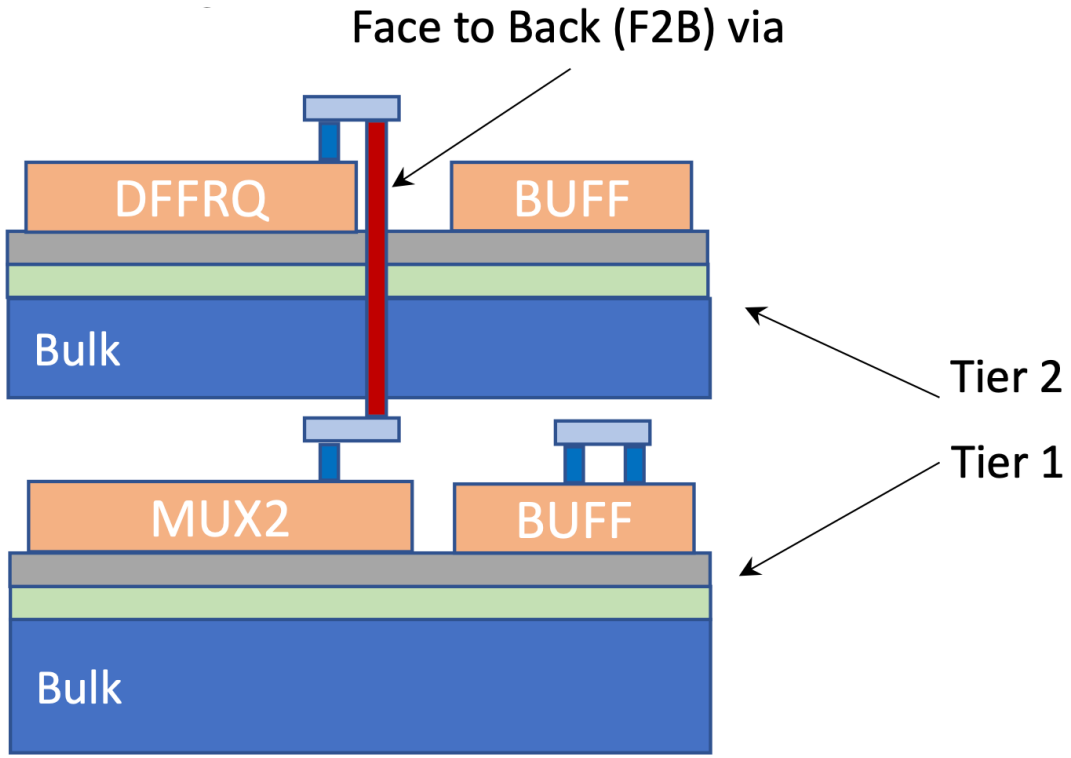


[Best CAD tool at the 15th International Conference on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design, IEEE SMACD 2018]

Implementation Tool chain Integration

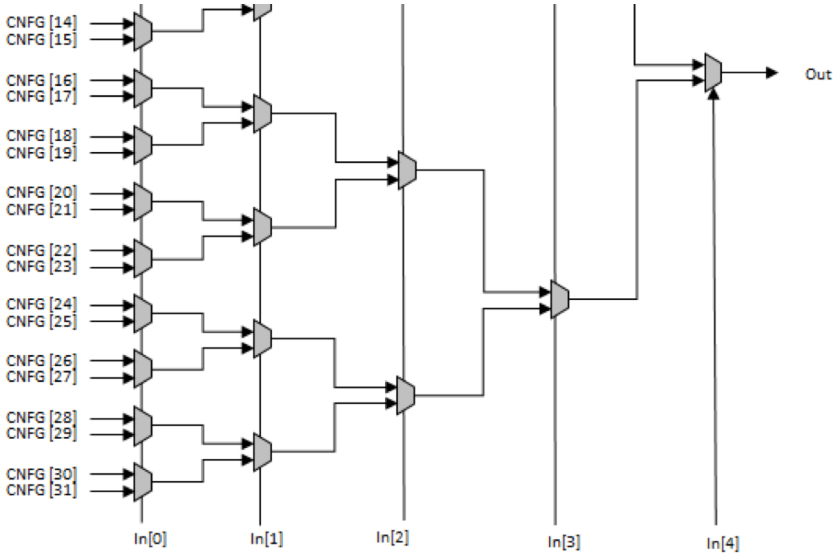


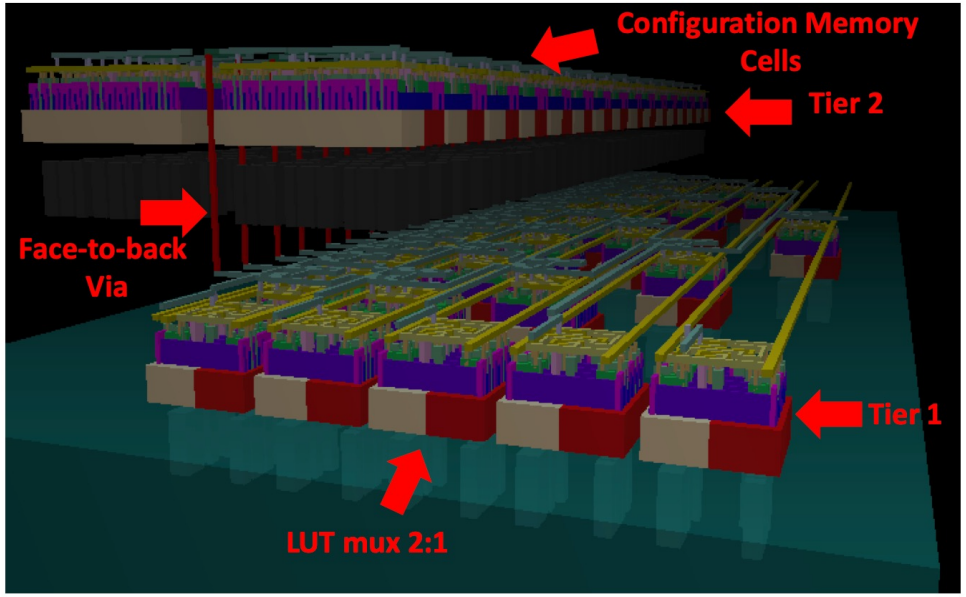
3D LUT Radiation Effects



[RADECS19]

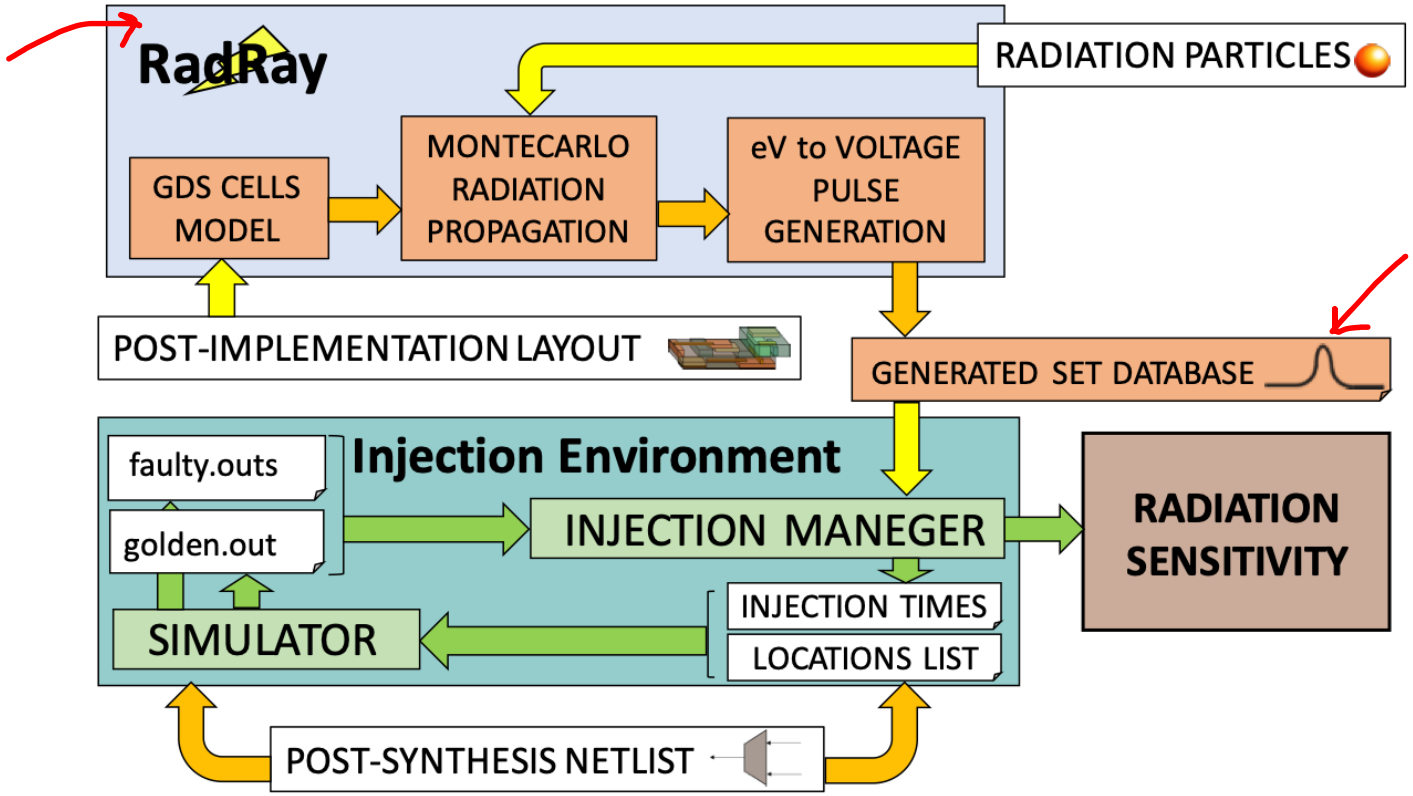
3D LUT Radiation Effects





[RADECS19]

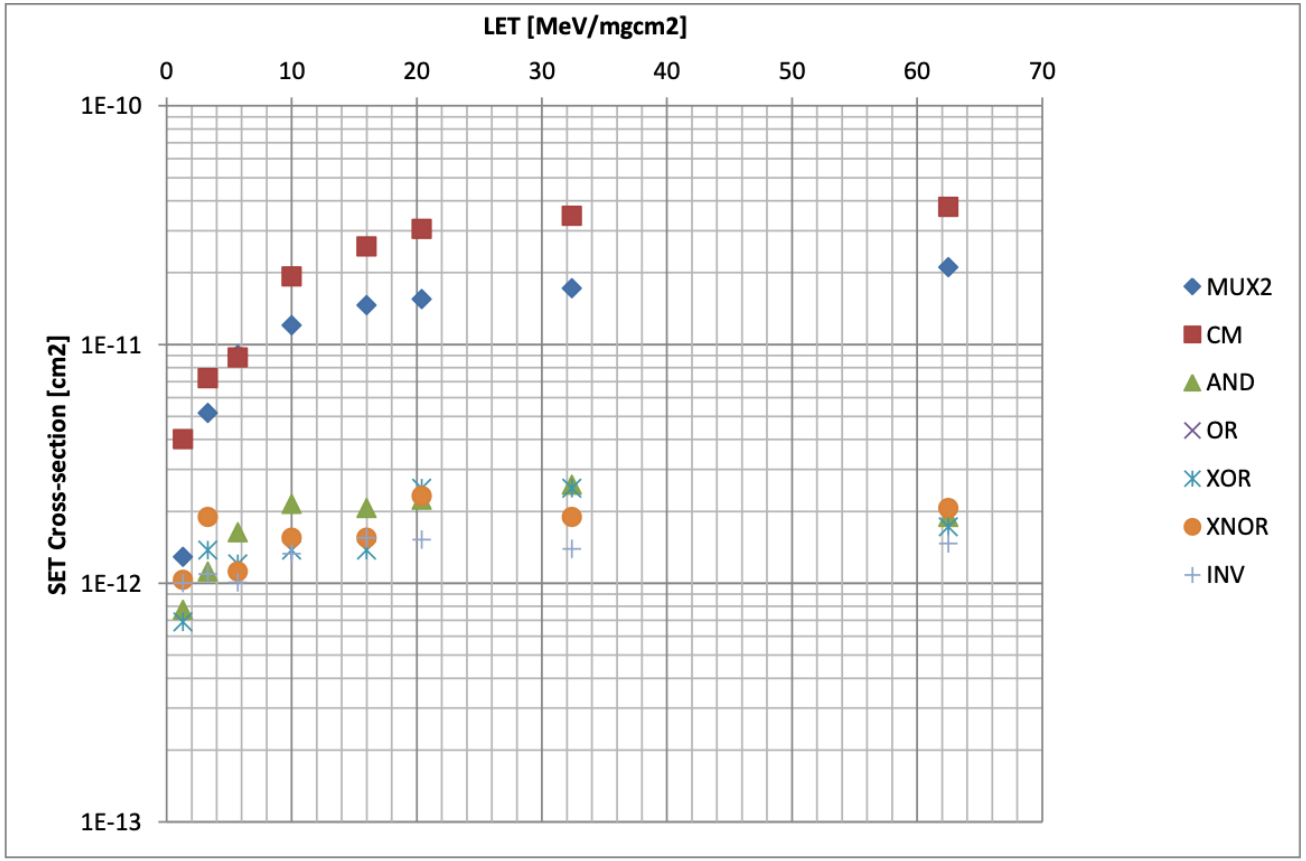
3D LUT Radiation Effects



[RADECS19]

3D LUT Radiation Effects

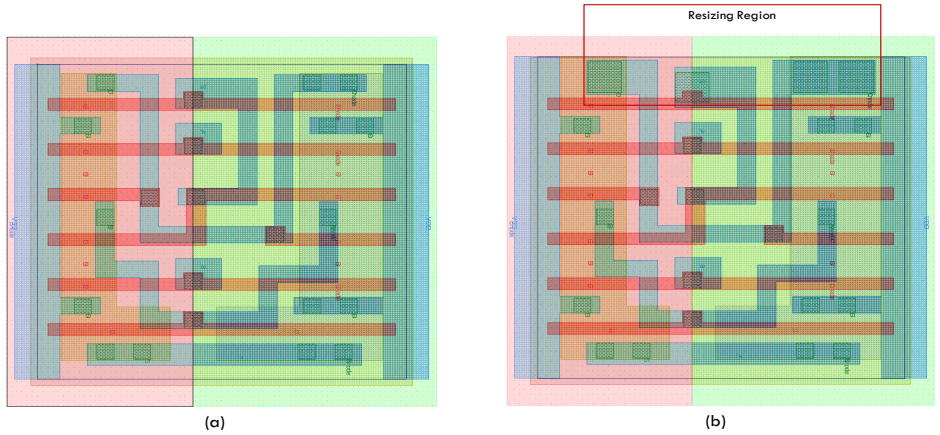
- Single Event Transient (SET) cross-section [cm2] for static radiation analysis (MUX2 and CM)
- Computing the dynamic analysis for five LUT configuration (AND, OR, XOR, XNOR and INV).

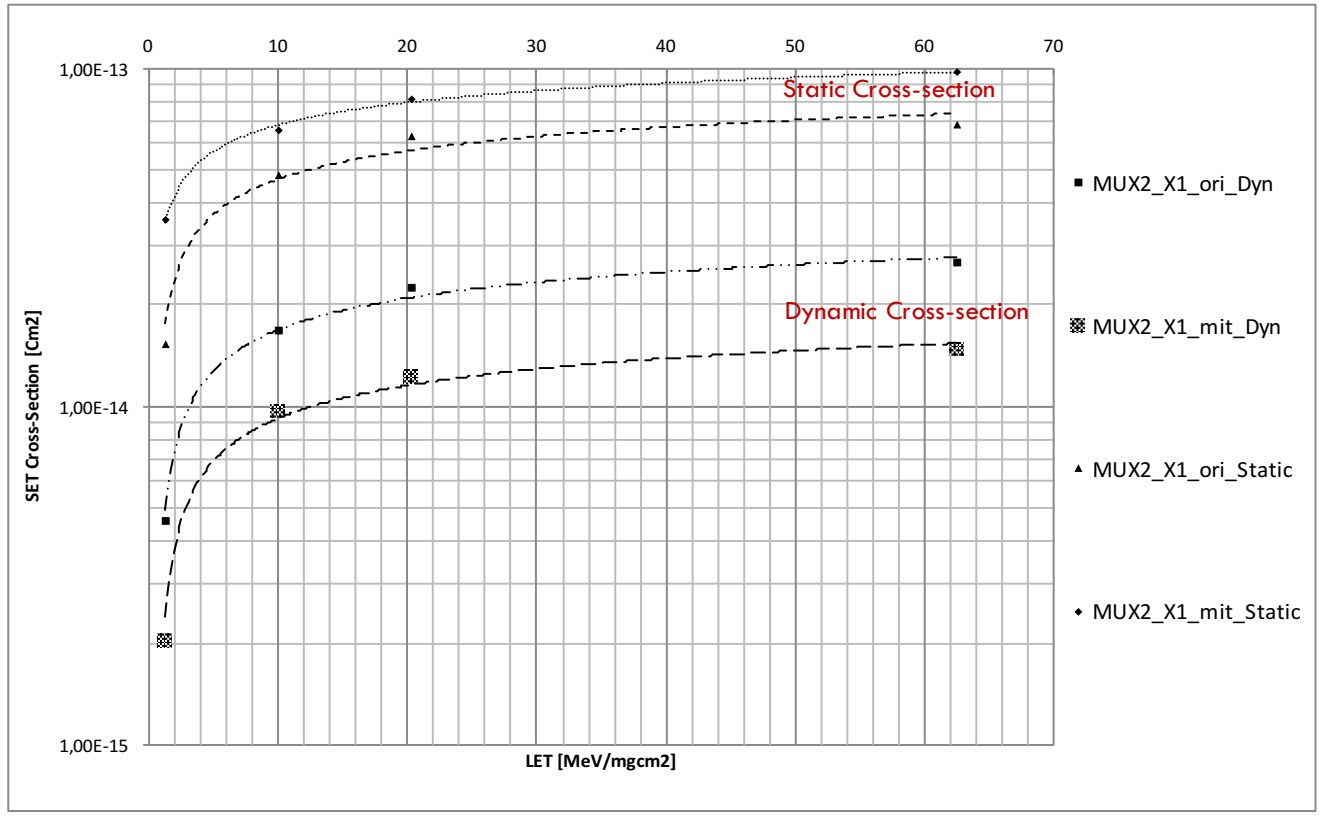


[RADECS19]

3D LUT Radiation Effects

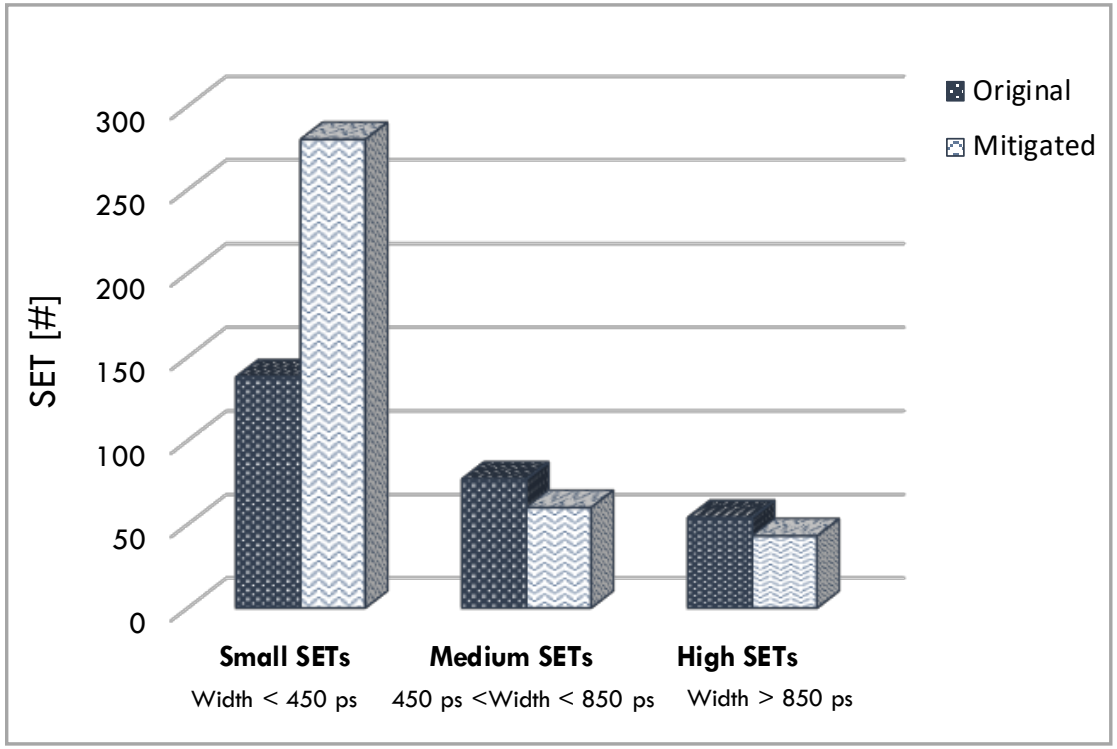
- Selective resizing of vulnerable transistors





[RADECS20] [TVLSI]

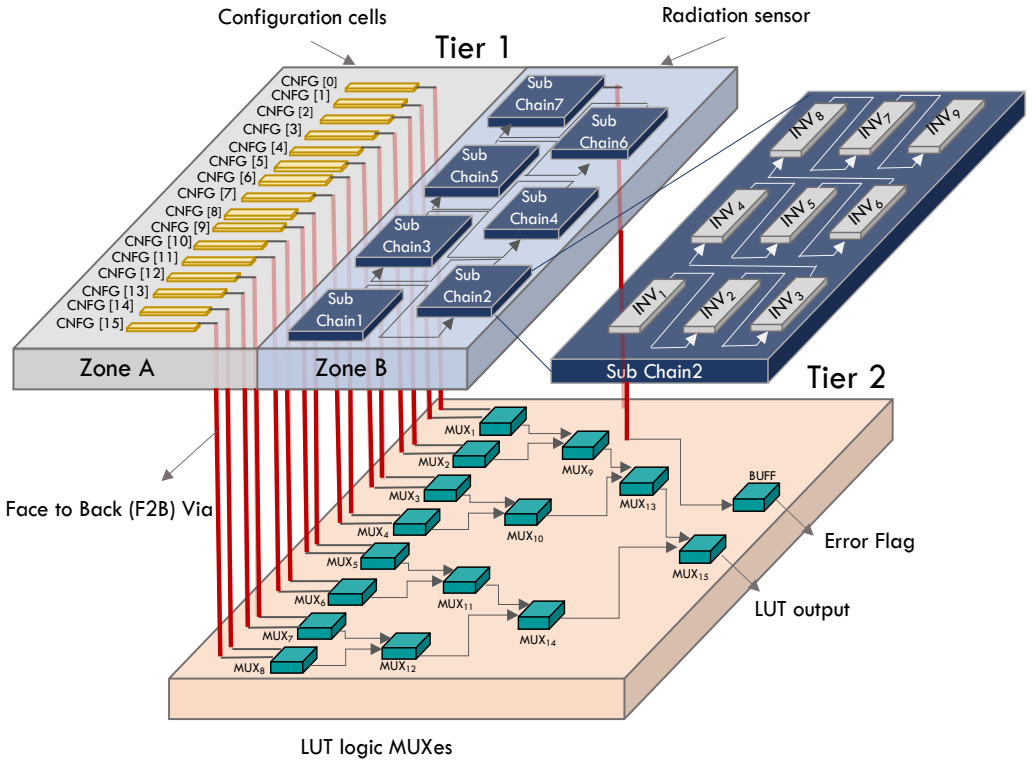
3D LUT Radiation Effects

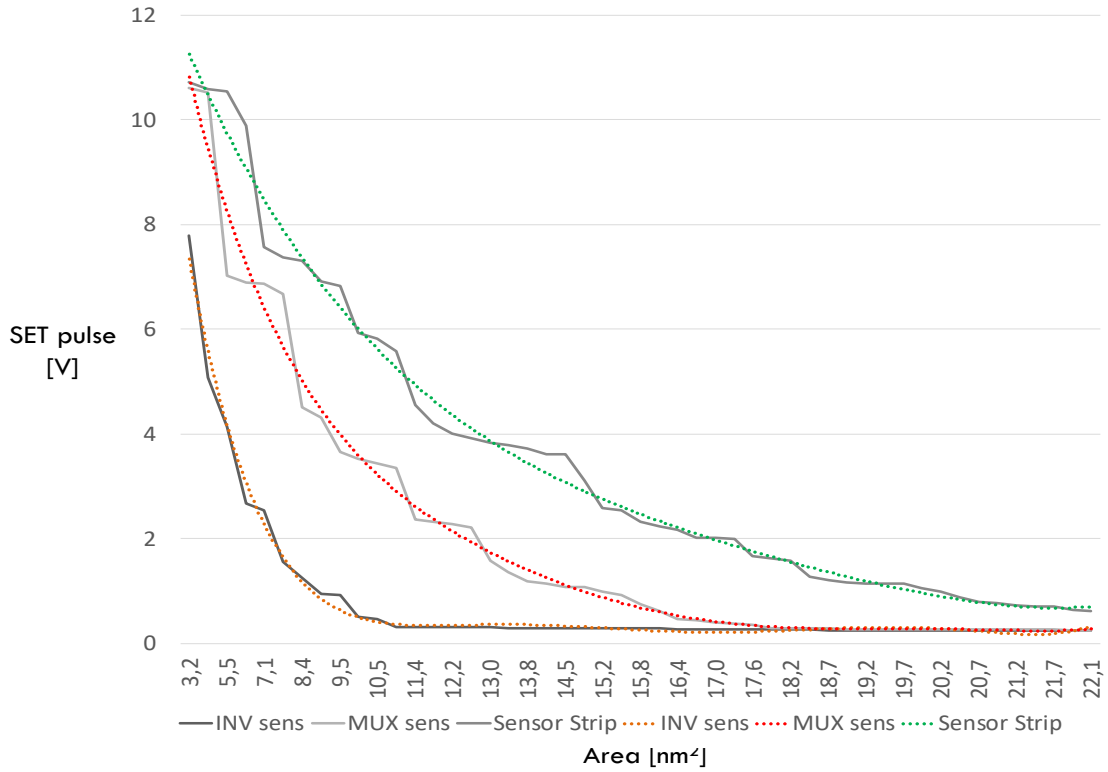


[RADECS20]

Error Detection 3D LUT

❑ In-Silicon Radiation Sensor





[IEEEDATE21]

Conclusions

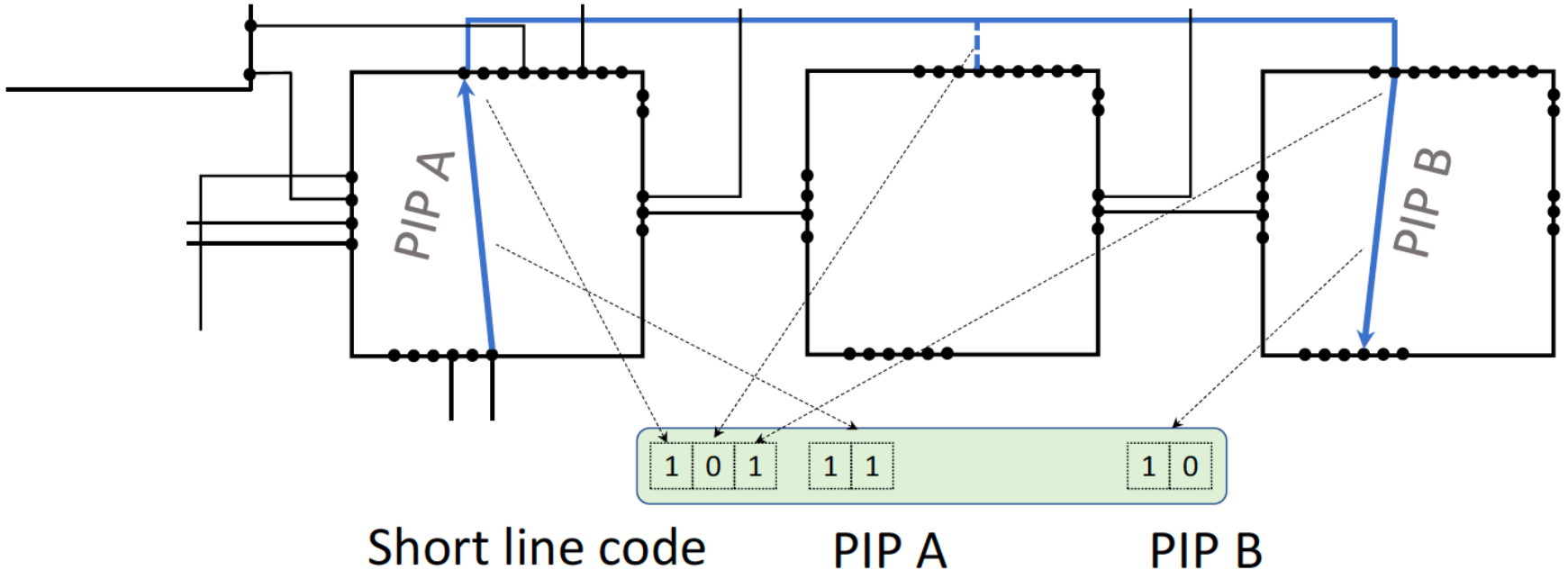
- Consolidated effects but new radiation mechanisms for ultra nanometer technologies
- Traditional mitigation techniques are suitable but require automatized tools for analysis and mitigation
- CAD tools for 3D devices
- Industrial and radiation test experiences are of fundamental support in CAD tool development

Thank you

- luca.sterpone@polito.it

Routing Switch architectural model

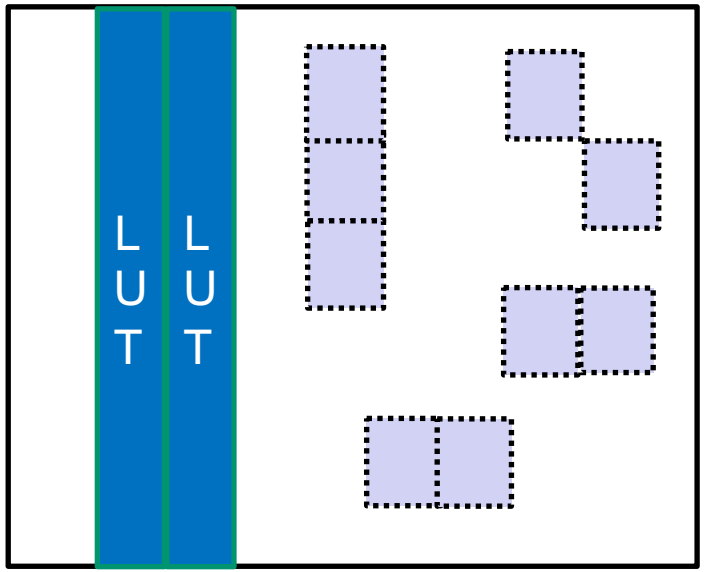
- **The model is based on the routing organization of AMD-Xilinx Series-7 SRAM-based FPGAs**
- **Essential to model the SEU-induced architectural propagation**
  - memory bit coding is associated the relative group of PIPs



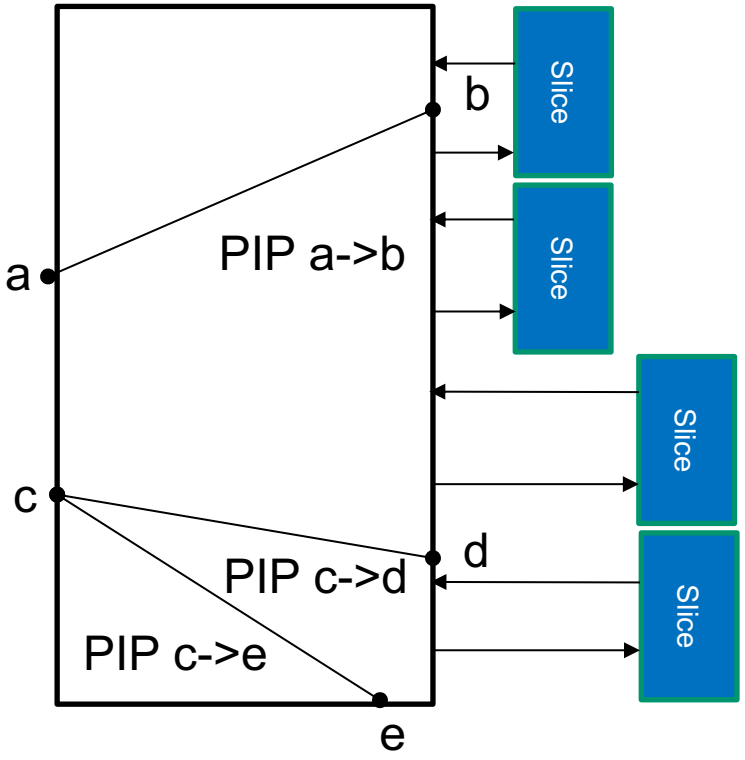
Routing Switch architectural model

- **The configuration memory bitmap models all routing PIPs**
  - Direct PIPs
  - Decoded PIPs

Zynq-7020 Configuration Map



FPGA Architectural Model



Routing Switch architectural model

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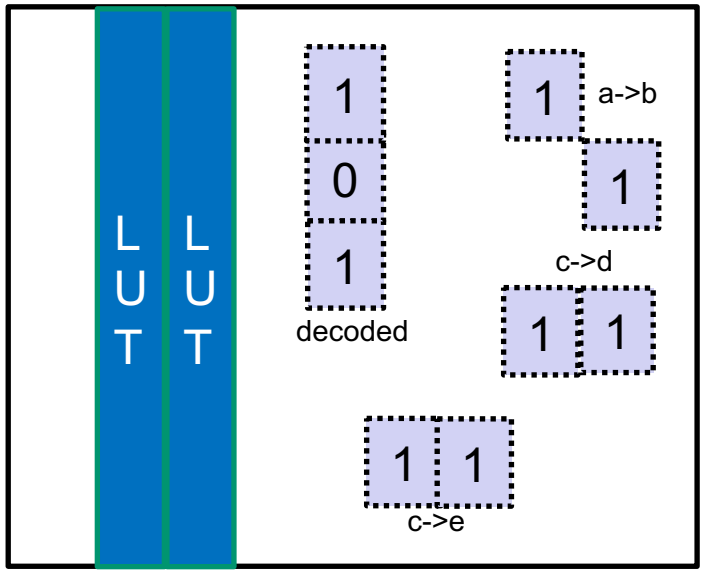
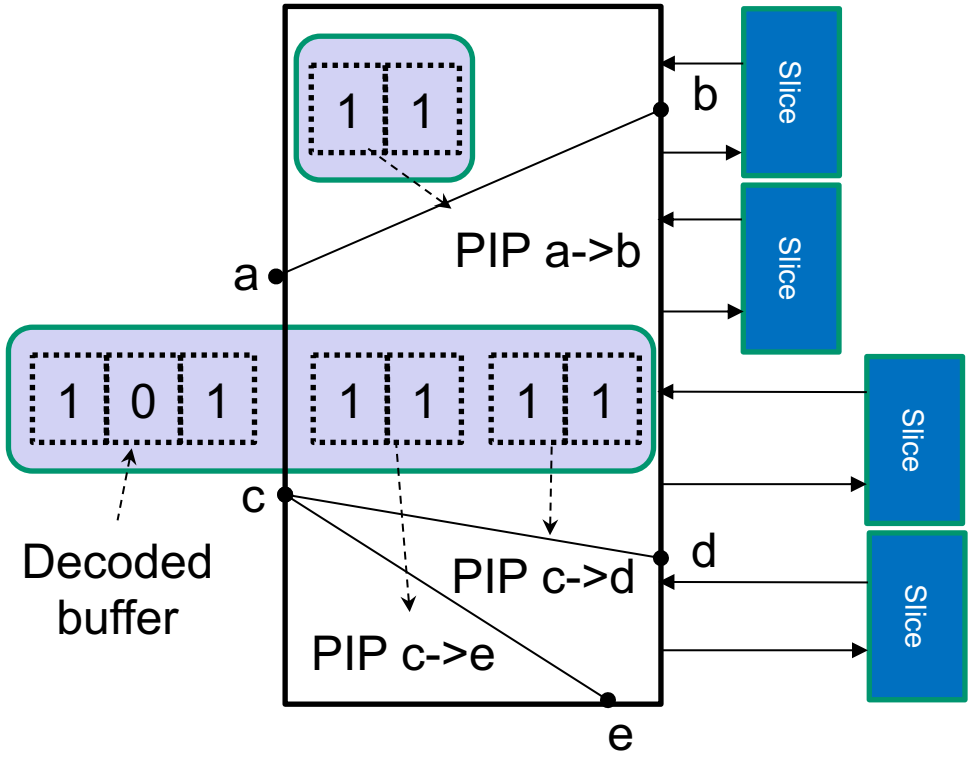
Zynq-7020 Configuration Map

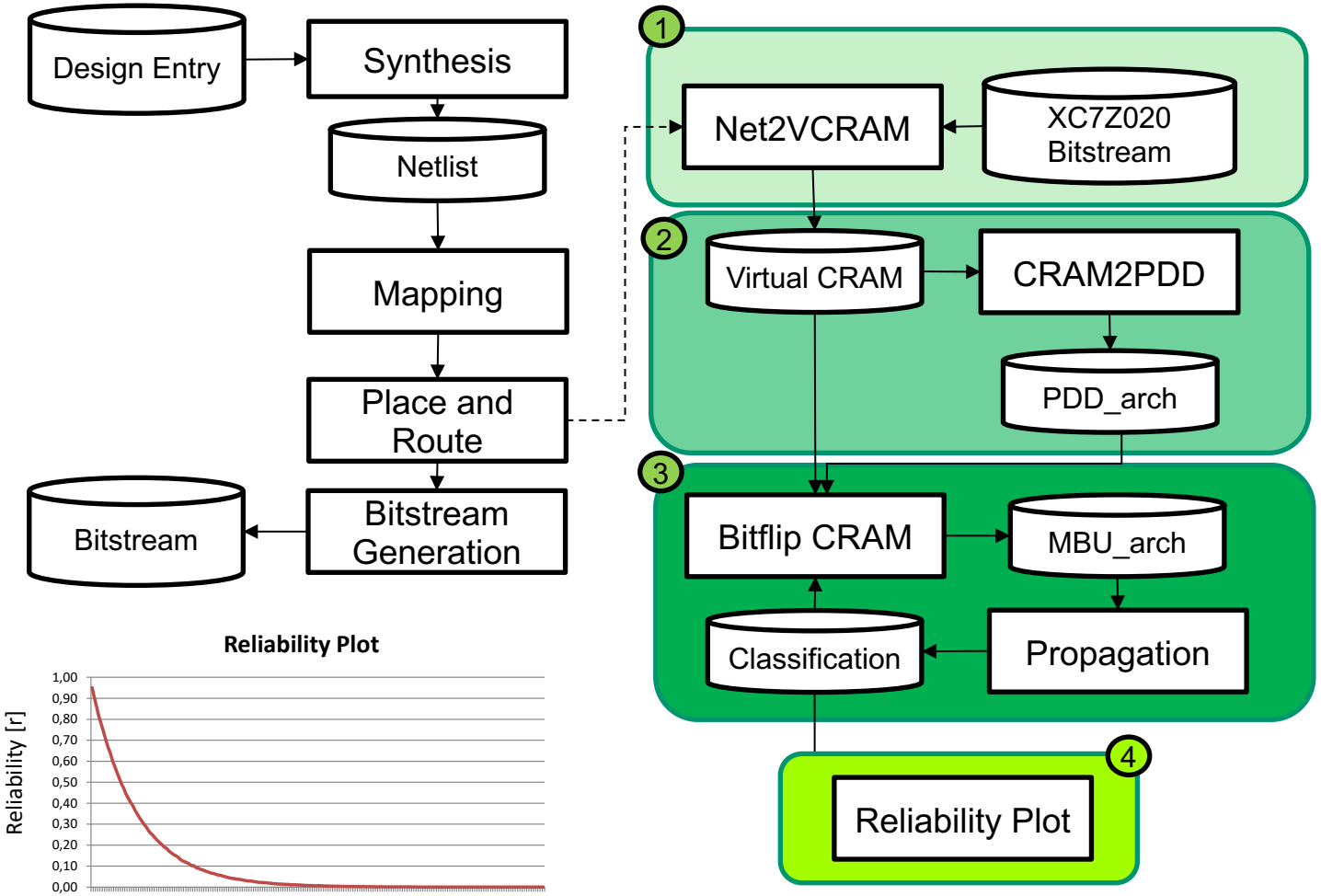


FPGA Architectural Model



Reliability Prediction Tool

AMD Xilinx Implementation Flow



1. Configuration coding
2. Architectural map
3. SEU insertion, propagation and classification
4. Cumulative effect and reliability results

Reliability Prediction Tool

- **Monte Carlo analysis with a limit up to 100,000 iterations per SEU combination**
- **Bit Classification criterias**
  - ***Accumulated***: bitflips accumulated in the virtual configuration memory
  - ***Miss***: number of upsets that did not hit any programmed resources
  - ***Error***: bitflips causing an error propagated to the output
  - ***Filtered***: bitflips that, even if there are related to a used resource, they did not propagate the error until an output cell

Back end on Reliability Prediction Tool