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Accurate Abstraction and High Level Modeling and Validation of SEE in Electronic Systems

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Abstract:

In this talk, we will be discussing the practical use of formal based techniques, such as SAT, SMT and probabilistic model checker to analyze SEEs at logical and higher abstraction levels. Through examples, we will illustrate each approach and its benefits.

Short Bio:

Dr. Ait Mohamed received his Ph.D. (1996) in Computer Science from Université Henri Poincaré, Nancy 1. Before his arrival at Concordia in 2002, he worked as a Postdoctoral Fellow at Université de Montréal, a Research Scientist at Cistel, and a Senior Verification Engineer at Nortel Networks in Ottawa. Dr. Ait Mohamed main research areas include model checking, assertion-based verification, FPGA-based design and verification, radiation effect on electronic circuit for aerospace applications and medical applications. Formal based techniques to analyze the reliability and the performability of such systems are investigated and several peer reviewed papers and journals has been already published. Currently, he is a full professor with the Electrical and Computer Engineering department at Concordia University.

Organizers: