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Sensitivity characterization of SRAM-based FPGA against SEU and SET

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Abstract:

One solution for emulating transient faults such as SEU, MBU or SET resulting from particle accelerators or even from real particle radiation in space, consists in irradiating the circuit with electromagnetic radiation. The objective of this work is to characterize an FPGA circuit based on SRAM memory (Cyclone V SoC of the DE10-Nano board) against transient faults resulting from electromagnetic radiation. The fault injection tool used is the ChipSHOUTER. A complete testbed has been realized allowing the reliable reproduction of the fault injection campaigns. The analysis and interpretation of the results of fault injection campaigns on different DUT (Design Under Test) are detailed in this presentation. This work allowed us to better understand the sensitivity of this circuit, built on TSMC's 28 nm low-power (28LP) process technology, against transient faults.

Short Bio:

Fakhreddine Ghaffari (Member, IEEE) received the degree in electrical engineering and master's degree from the National School of Electrical Engineering (ENIS), Tunisia, in 2001 and 2002, respectively, and the Ph.D. degree in electronics and electrical engineering from the University of Sophia Antipolis, France, in 2006. He is currently an Associate Professor with CY Cergy paris University, France. His research interests include VLSI design and implementation of reliable digital architectures for wireless communication applications in ASIC/FPGA platform and the study of mitigating transient faults from algorithmic and implementation perspectives for high-throughput applications.

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