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CERN

Sensitivity characterization of SRAM-based FPGA against SEU and SET

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SUMMARY

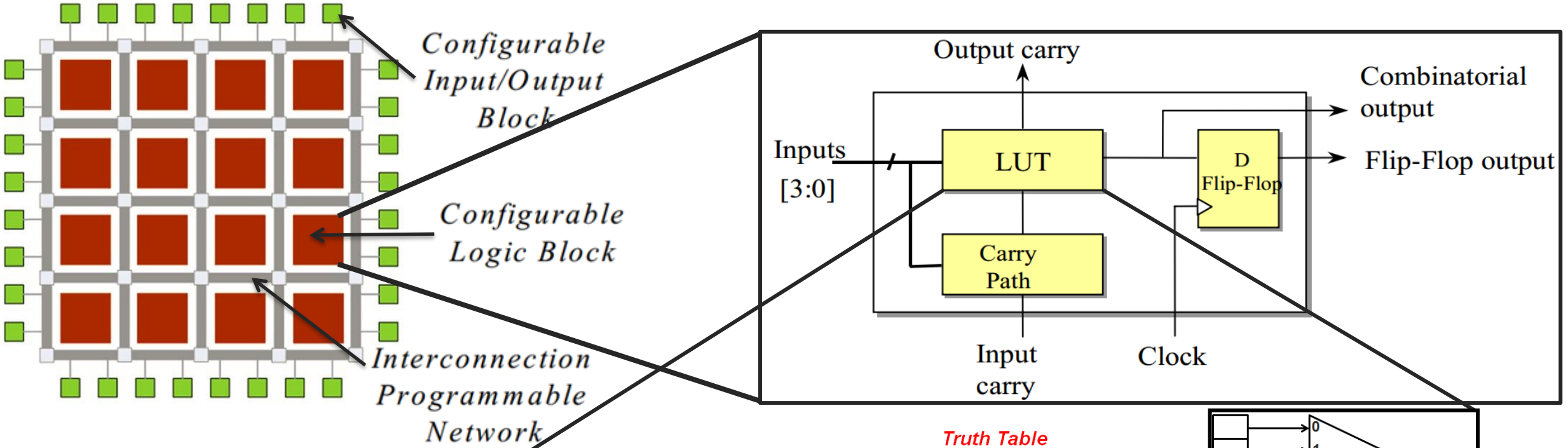
MOTIVATIONS

I. Motivations

II. State of the Art

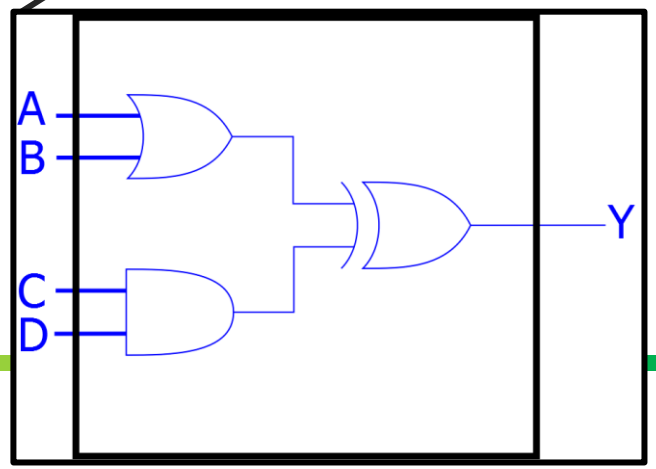
III. Contributions

IV. Conclusion and Perspectives



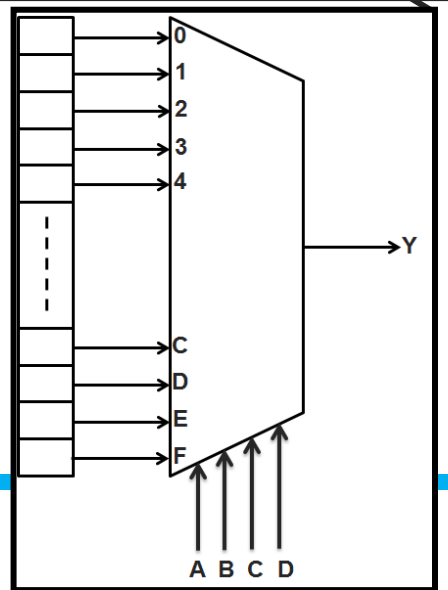
Newer FPGAs embed :

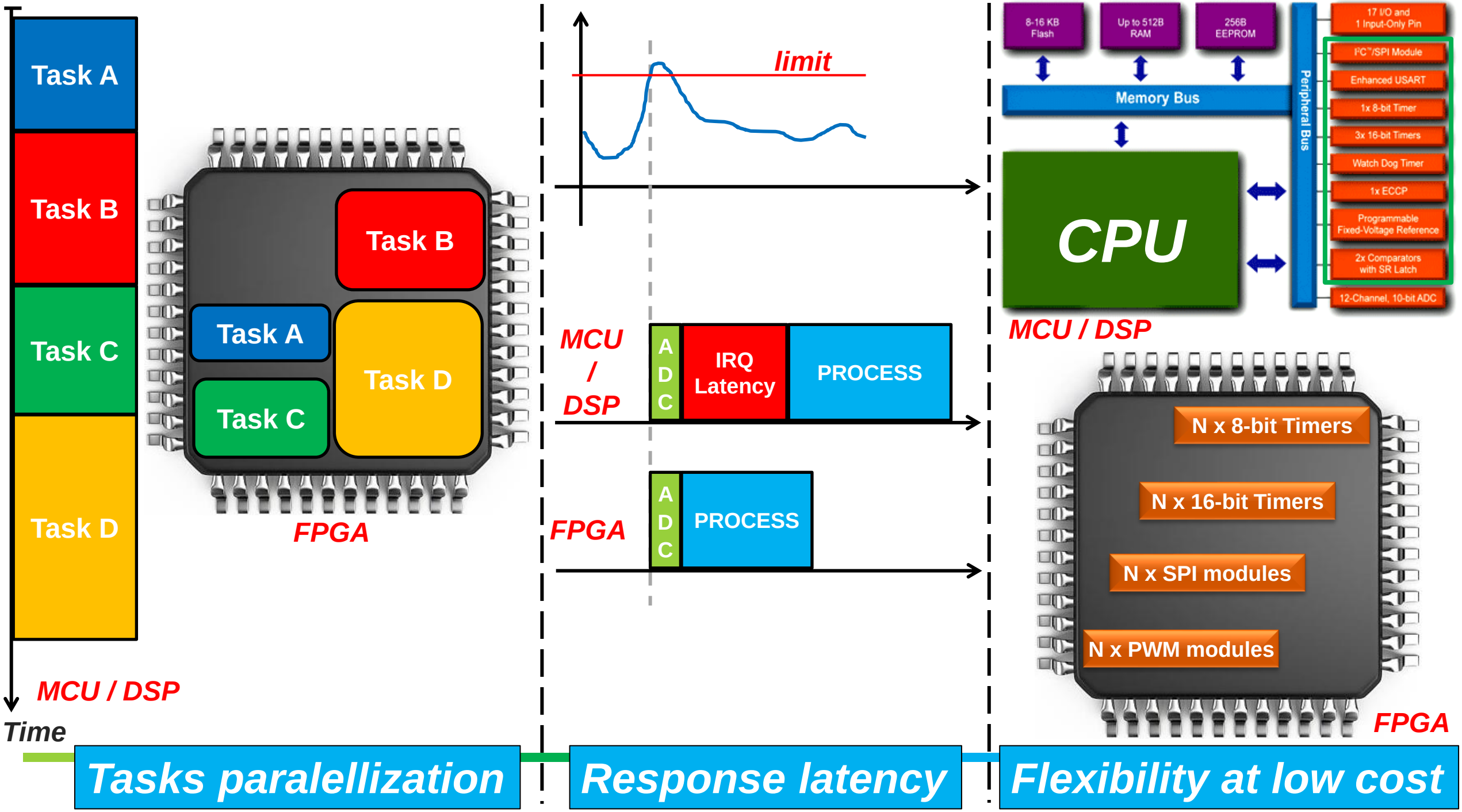
- ❑ Hard processor
- ❑ H-P DSP Blocks
- ❑ PLL,
- ❑ ADC,
- ❑ Flash memory,
- ❑ Transceivers,
- ❑ PCIe Hard IP, …



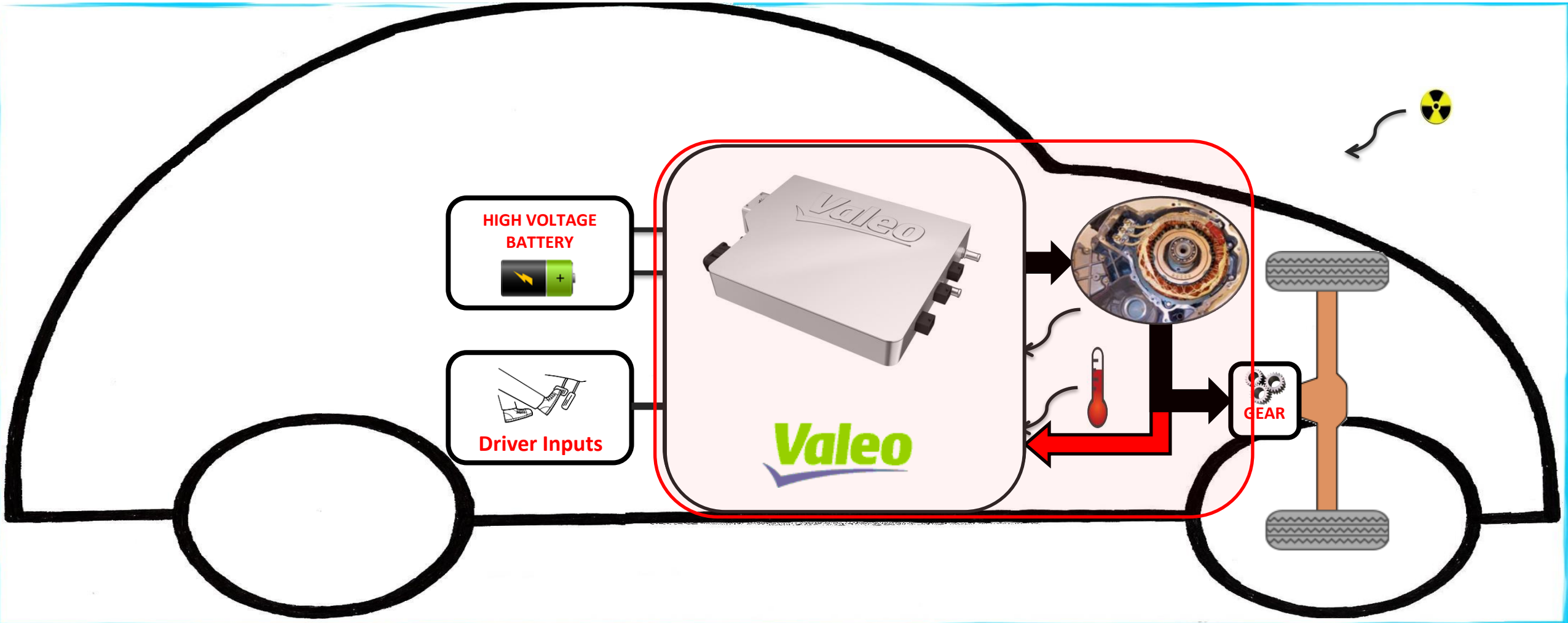
Truth Table

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	0	0	0	1
⋮	⋮	⋮	⋮	⋮
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0




Task A
Task B
Task C
Task D
MCU / DSP
Time
Task B
Task A
Task D
Task C
FPGA
limit
MCU / DSP
A D C
IRQ Latency
PROCESS
FPGA
A D C
PROCESS
8-16 KB Flash
Up to 512B RAM
256B EEPROM
17 I/O and 1 Input-Only Pin
I²C™/SPI Module
Enhanced USART
1x 8-bit Timer
3x 16-bit Timers
Watch Dog Timer
1x ECCP
Programmable Fixed-Voltage Reference
2x Comparators with SR Latch
12-Channel, 10-bit ADC
Peripheral Bus
Memory Bus
CPU
MCU / DSP
N x 8-bit Timers
N x 16-bit Timers
N x SPI modules
N x PWM modules
FPGA
Tasks paralellization
Response latency
Flexibility at low cost

MOTIVATION



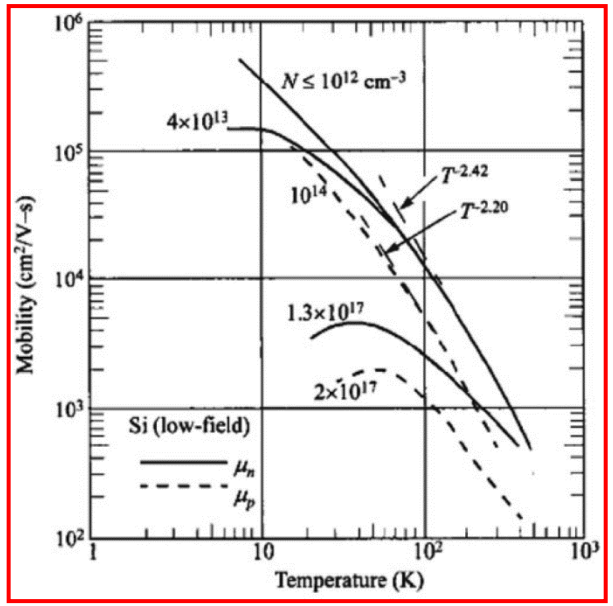
Safety-critical applications cannot allow such behavior !

Contrary to MCU and DSP, it is up to the FPGA designers to ensure the correct execution of the design to be implemented in the FPGA.

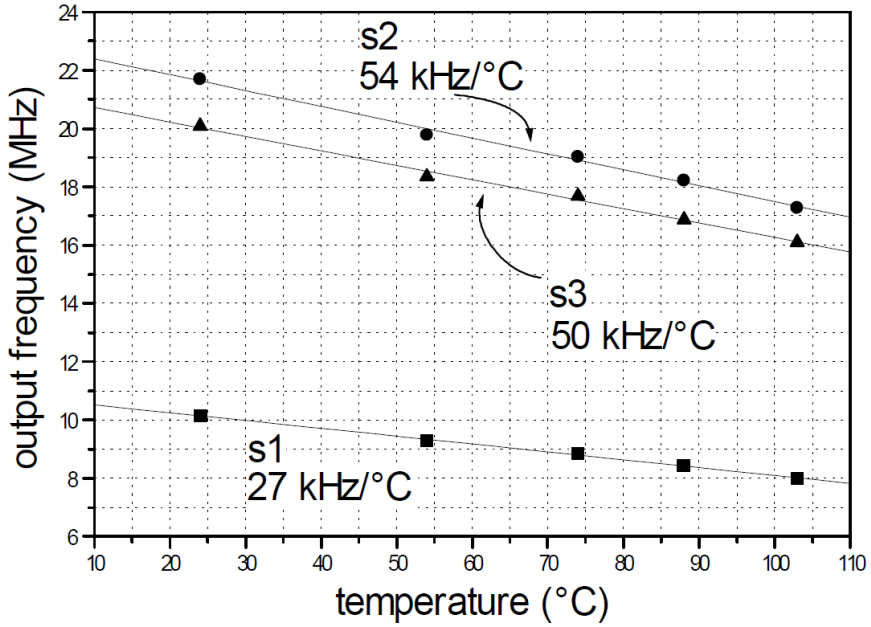
SUMMARY

TEMPERATURE EFFECTS

$$T_{plh} = \frac{C_L \left[\frac{2|V_{th,p}|}{V_{dd} - |V_{th,p}|} + ln\left(3 - 4\frac{V_{th,p}}{V_{dd}}\right) \right]}{\mu_p C_{ox} \frac{W_p}{L_p} (V_{dd} - |V_{th,p}|)}$$



$V_{th,p}$ is also proportional to T

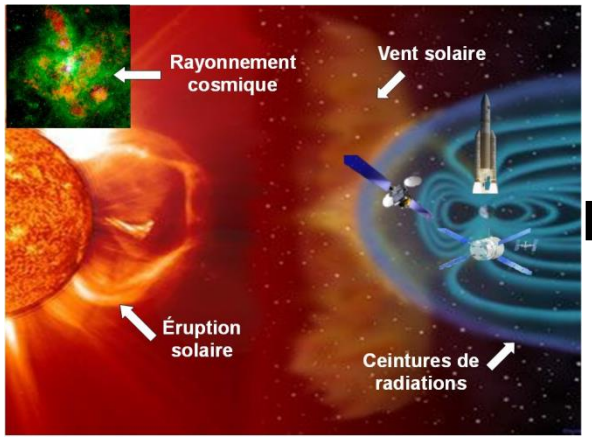


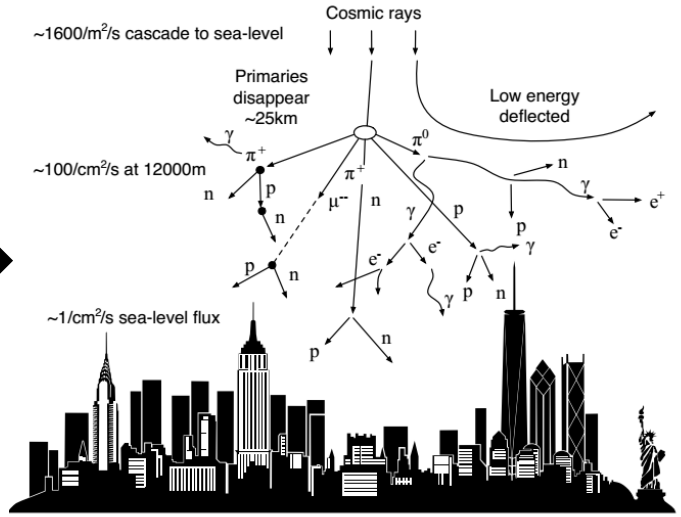
[Boe-1997] Boemo et al., Thermal monitoring on fpgas using ring-oscillators, "International Workshop on Field-Programmable Logic and Applications, 1997

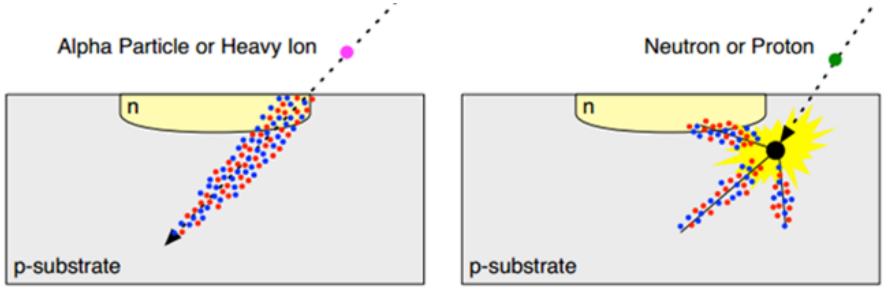
[Wol-2012] Wolpert et al., Managing Temperature Effects in Nanoscale Adaptive Systems, Springer, 2012
[Fil-2001] Filanovsky et al., Mutual compensation of mobility and threshold voltage temperature effects with applications in cmos circuits," IEEE Transactions on Circuits and Systems, 2001

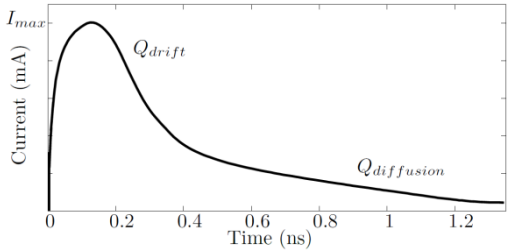
The temperature affects the propagation delay inside the FPGA.

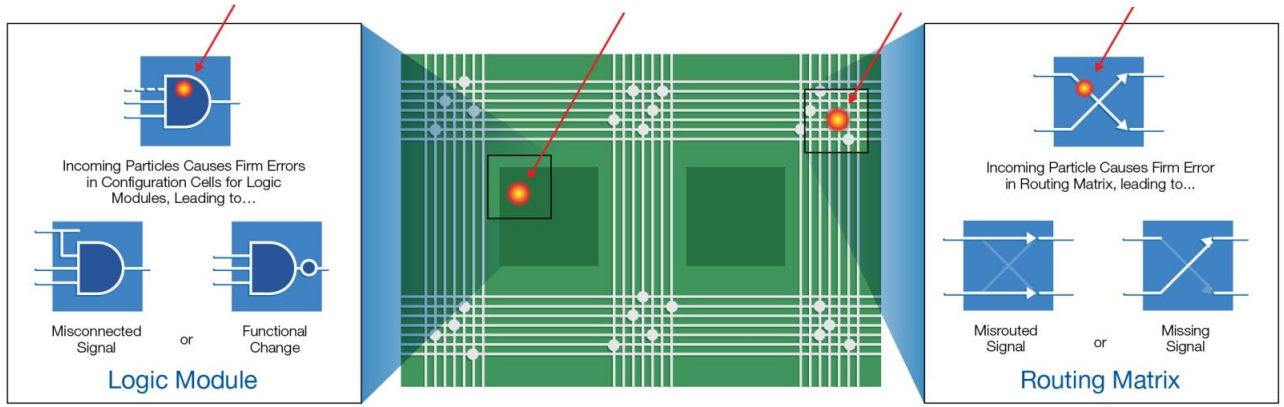
TEMPERATURE AND RADIATION EFFECTS

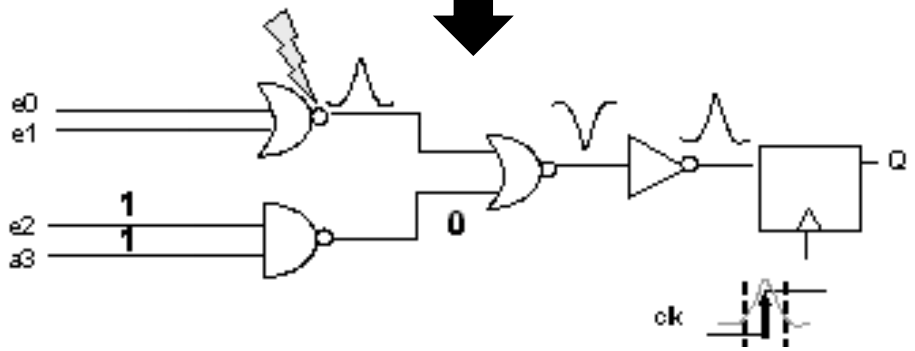








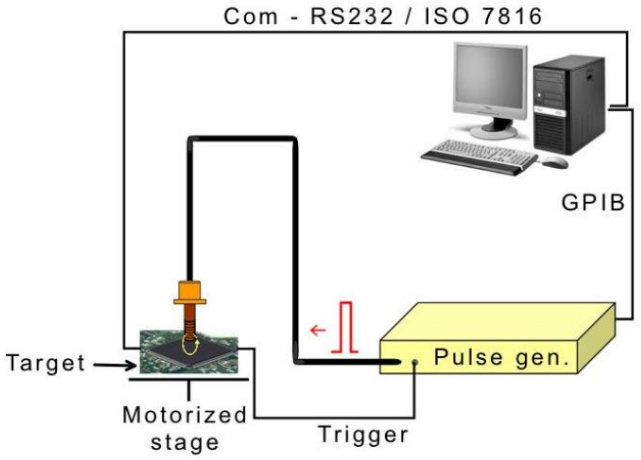


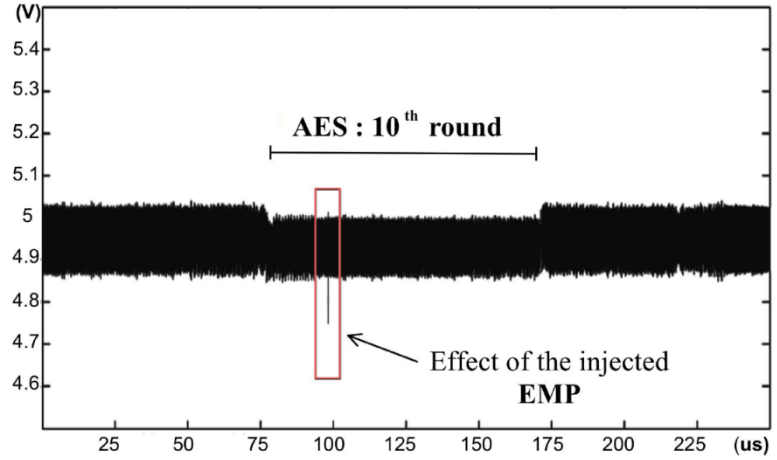


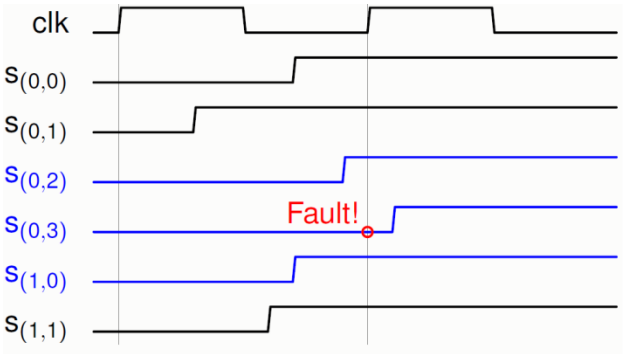
[Les-2005] Lesea et al.,The rosetta experiment: atmospheric soft error rate testing in differing technology fpgas," IEEE Transactions on Device and Materials Reliability, 2005
[Ohl-1998] Ohlsson et al., Neutron single event upsets in sram-based fpgas," in Radiation Effects Data Workshop, 1998

Radiation particles can cause Single Event Upset and Single Event Transient in the FPGA.

ELECTROMAGNETIC FIELD EFFECTS







[Deh-2012] Dehbaoui et al., Electromagnetic transient faults injection on a hardware and a software implementations of aes," in Fault Diagnosis and Tolerance in Cryptography (FDTC), 2012 Workshop on, Sept 2012

Electromagnetic field can induce timing errors in the FPGA design.

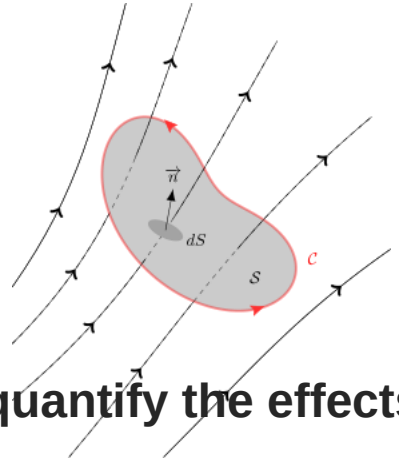
SUMMARY OF STATE OF THE ART

- Temperature ★★★ :
  - Effects : Variation of the propagation delay.
  - Consequences : Could lead to timing errors under certain conditions.
  - Techniques exist to mitigate timing errors in FPGAs (Timing Error Recovery, Time Borrowing, etc.).
- Radiation ★★★:
  - Effects : Single event Transient and Single Event Upset (Single Event Effects).
  - Consequences : Modification of the FPGA functionality, propagation of a pulse toward a storage element.
  - Techniques exist to mitigate SEE in FPGAs (TMR, EDAC, BER, Scrubbing, etc.)
- Electromagnetic field ★☆☆:
  - Effects : Modification of the voltage
  - Consequences : Could lead to timing errors under certain conditions.
- **The following limitations have been identified :**
  - **No link to quantify the effect of a given electromagnetic field on an FPGA.**
  - **No published work address the effect of unintentional electromagnetic field on FPGA.**
  - **Combined effects ?**

SUMMARY

Field Coupling

Magnetic Field :



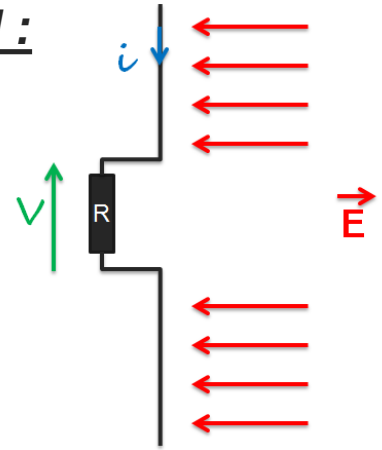
▪ ***Maxwell-Faraday :***

$$\oint_C \vec{E} \cdot \mathrm{d}\vec{\ell} = -\iint_S \frac{\partial \vec{B}}{\partial t} \cdot \vec{n}\,\mathrm{d}S$$

❑ How to quantify the effects of electromagnetic field on an FPGA ? ***$V_{emi} = \omega \mu H_n S$ (Faraday's Law of Induction)***

~~❑ Some basies regarding field coupling~~

Electric Field :

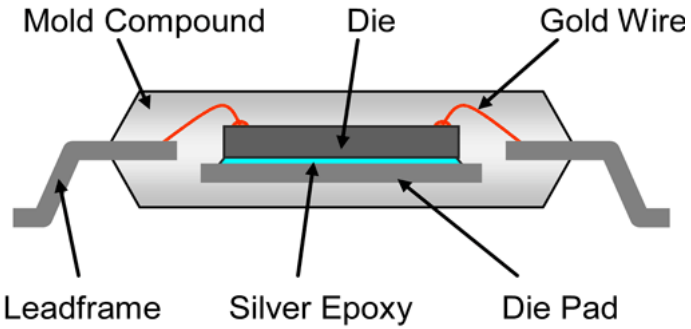


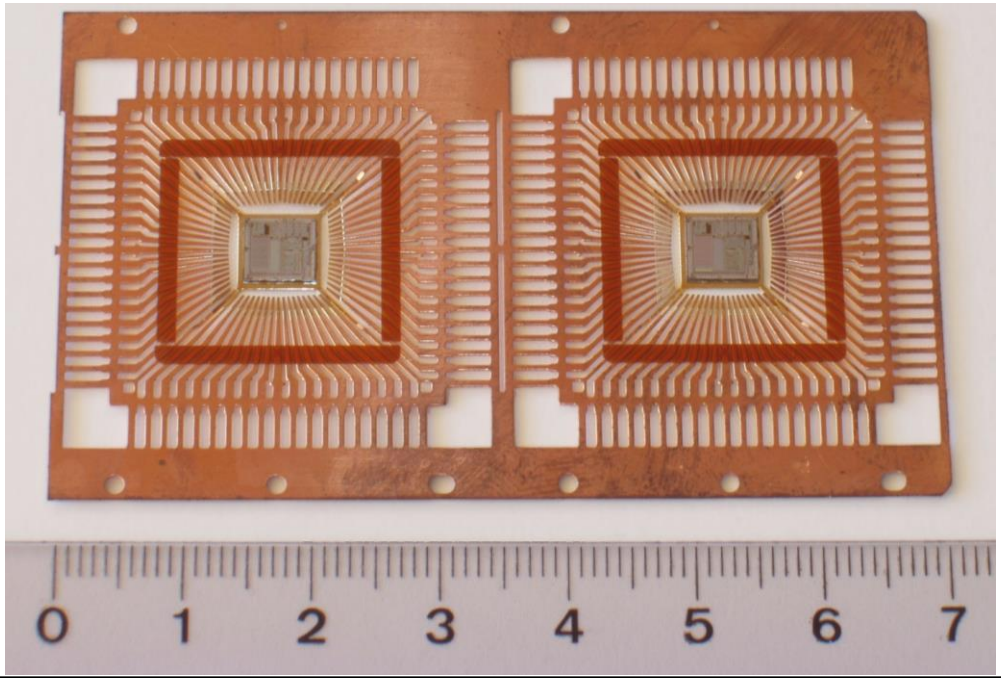
▪ ***Coupling is relative to the wavelength (λ = c / f)***

▪ ***Good coupling when conductor length = λ/4 (sometimes λ/10)***

Field coupling results in an induced voltage, function of the coupling parameters.

FIELD COUPLING AT IC LEVEL



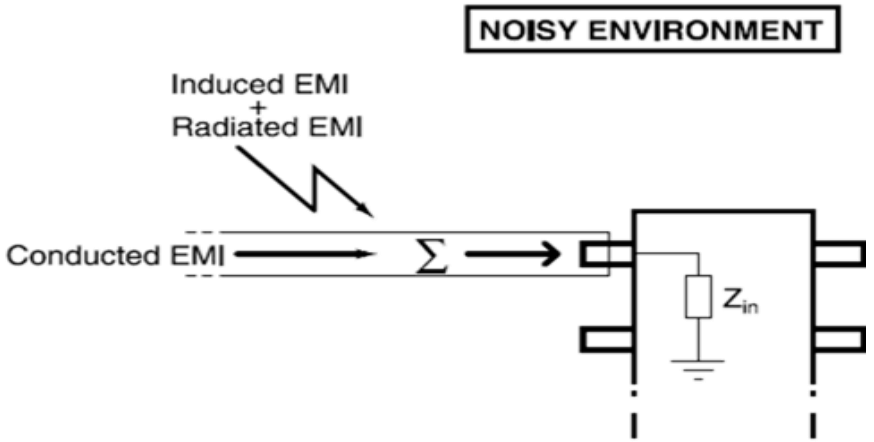


❑Motor frequency range up to ~ KHz.
❑Power Electronics up to hundreds of MHz.

At die scale, due to the micrometric size of the connections, magnetic field coupling is negligible.

Considering a 1 cm long leadframe + bonding :

- ***λ => 30 GHz***
- ***λ/4 => 7.5 GHz***
- ***λ/10 => 3 GHz***

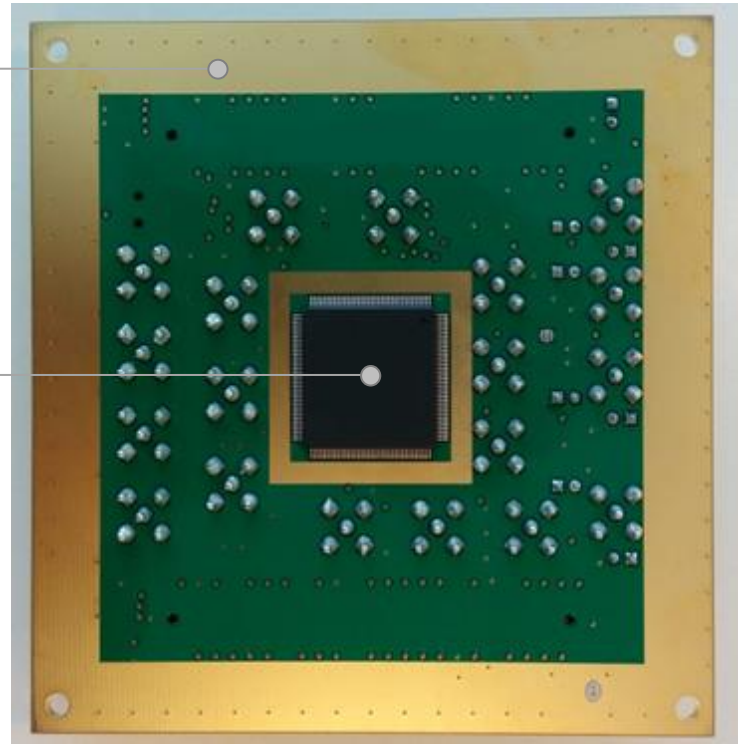


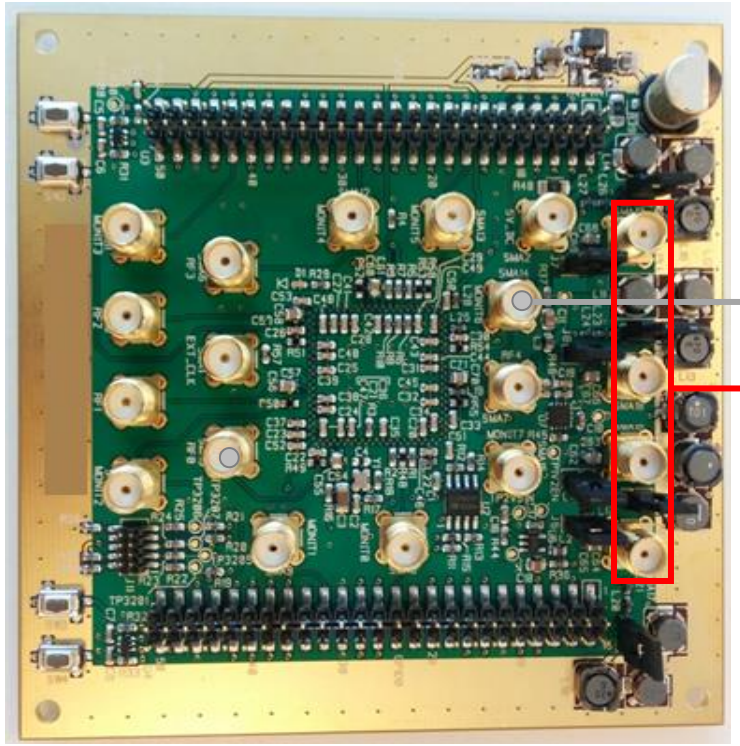
Electric field coupling is also negligible.

In our electromagnetic environment, we can consider that it will be difficult to directly disturb the IC itself.

PCB tracks will be the principal carriers of noise.

FPGA TEST BOARD



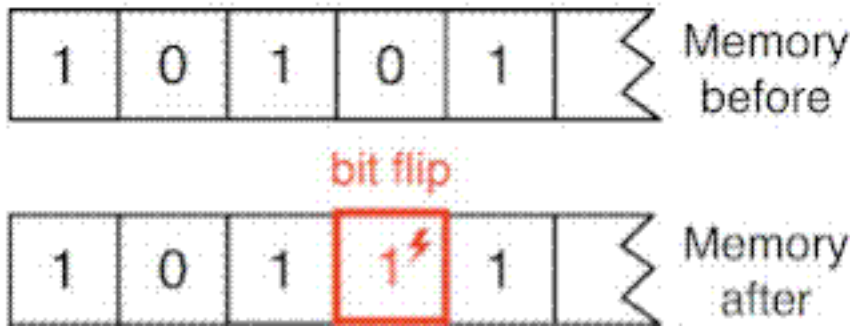


IEC 62132-1

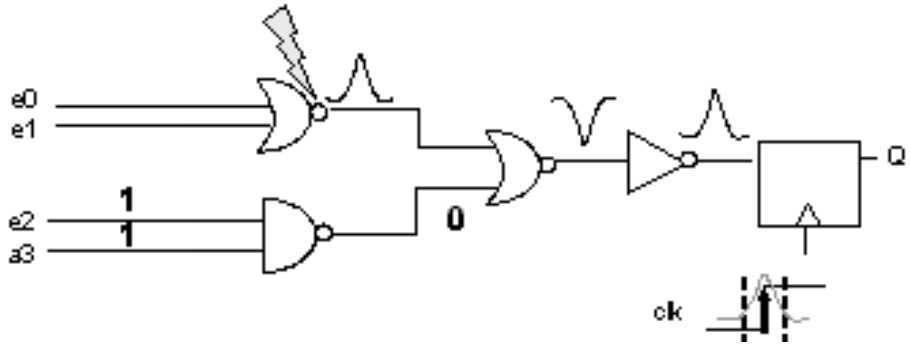
This board allows to :

- **Perform TEM cell test.**
- **Vary FPGA voltage test (direct access to FPGA power supply pads).**
- **Monitor the response of the FPGA when applying disturbances.**
- **Temperature tests.**

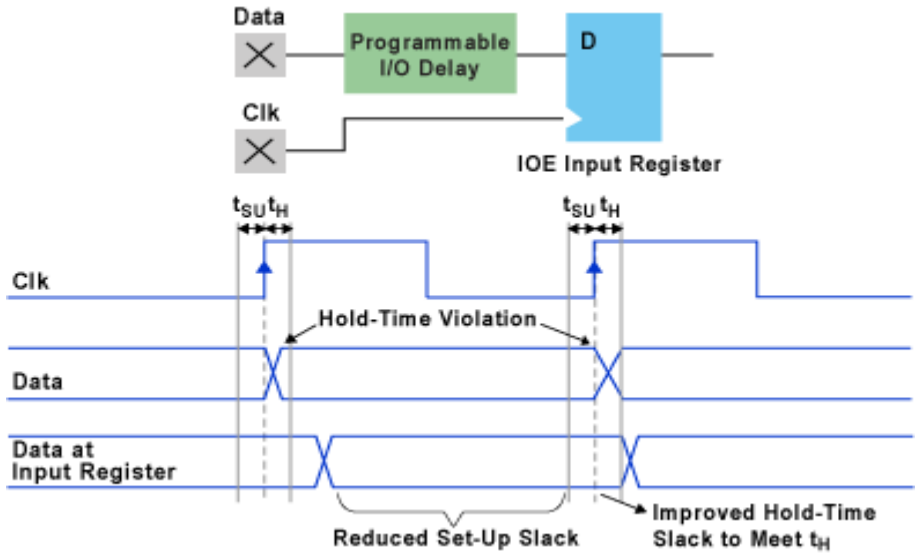
TYPE OF ERRORS



Upset

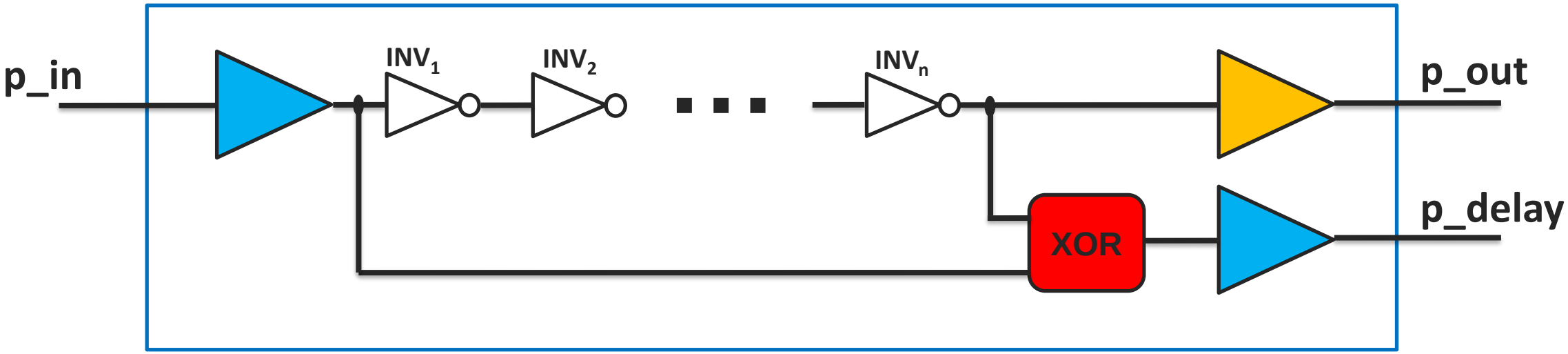


Transient



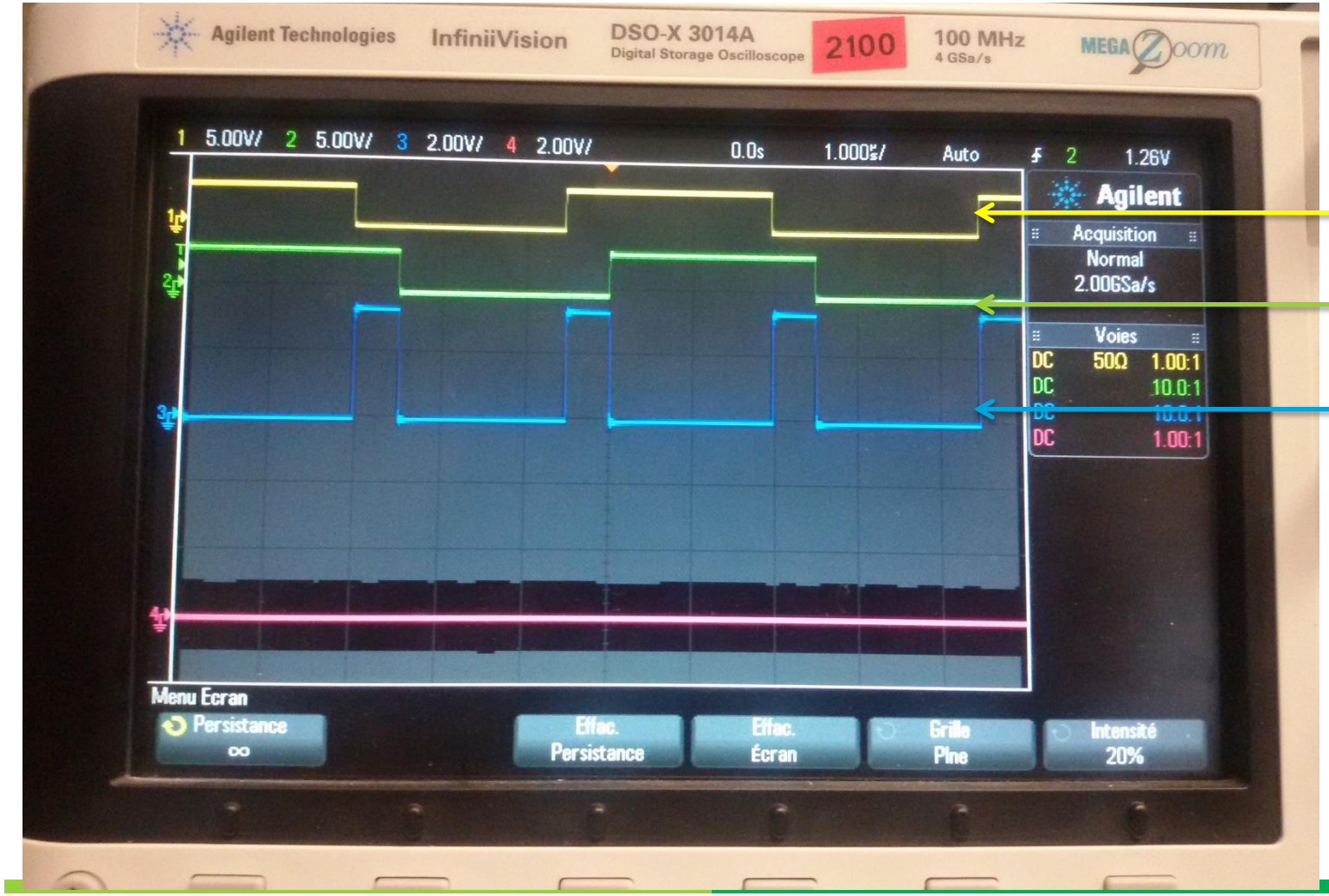
Timing

Propagation delay evaluation



1394-Inverter chain ⟶ Tdelay ~= 526 ns
1 inverter per LAB

Delay



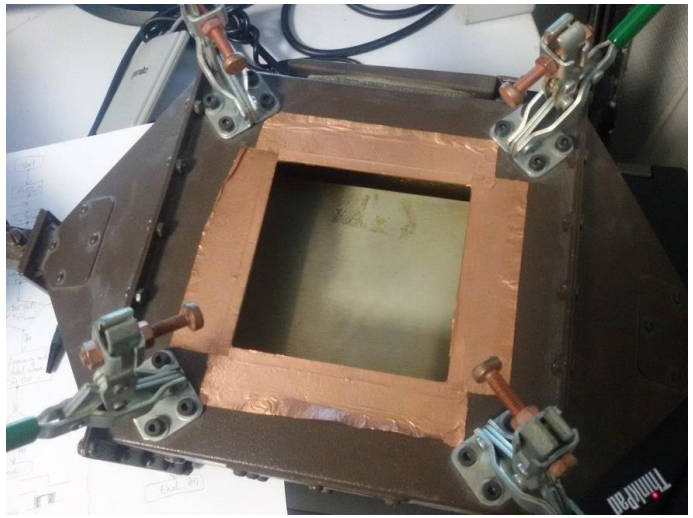
p_in

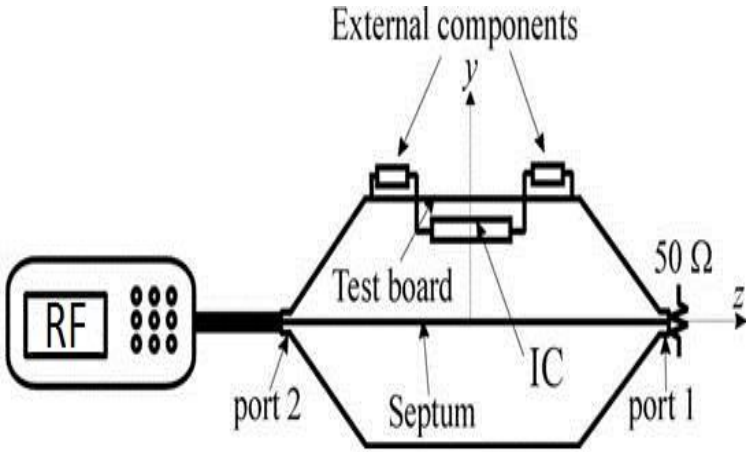
p_out

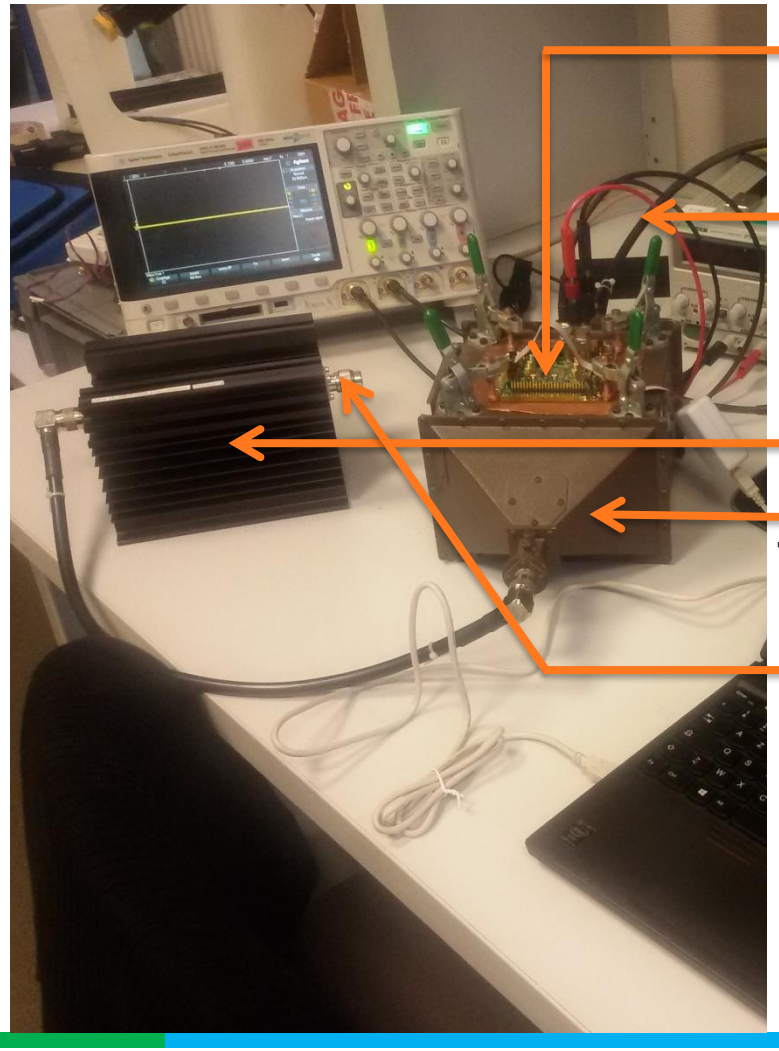
p_delay

RADIATED SUSCEPTIBILITY MEASUREMENT

IEC 62132-3 : TEM Cell







Results :

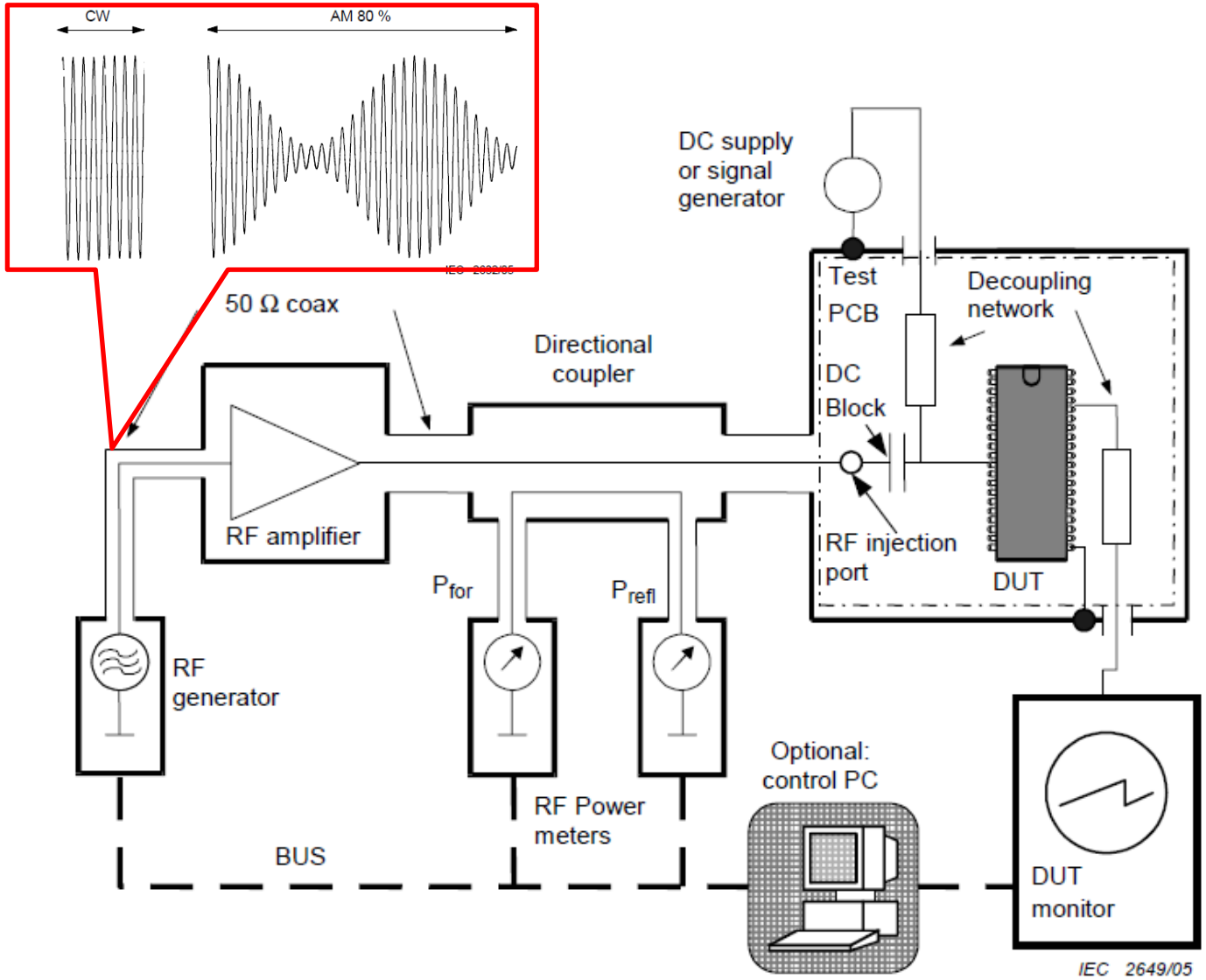
- Applied up to 370 V/m at IC level.

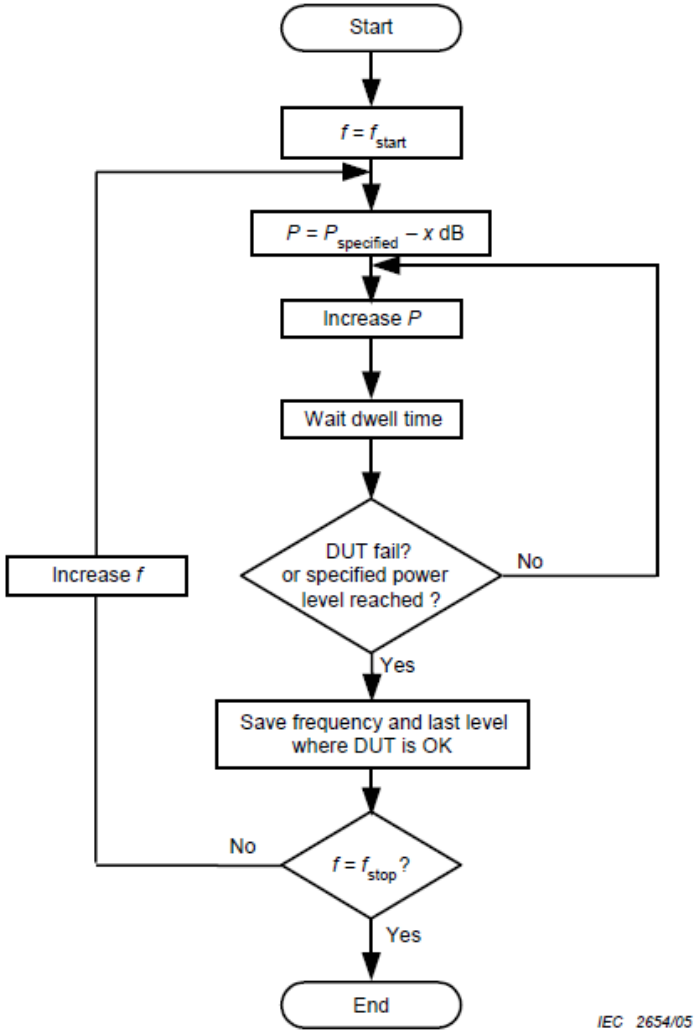
- Frequency range 10 KHz to 1 GHz.

- No error observed, confirming the previous assumption.

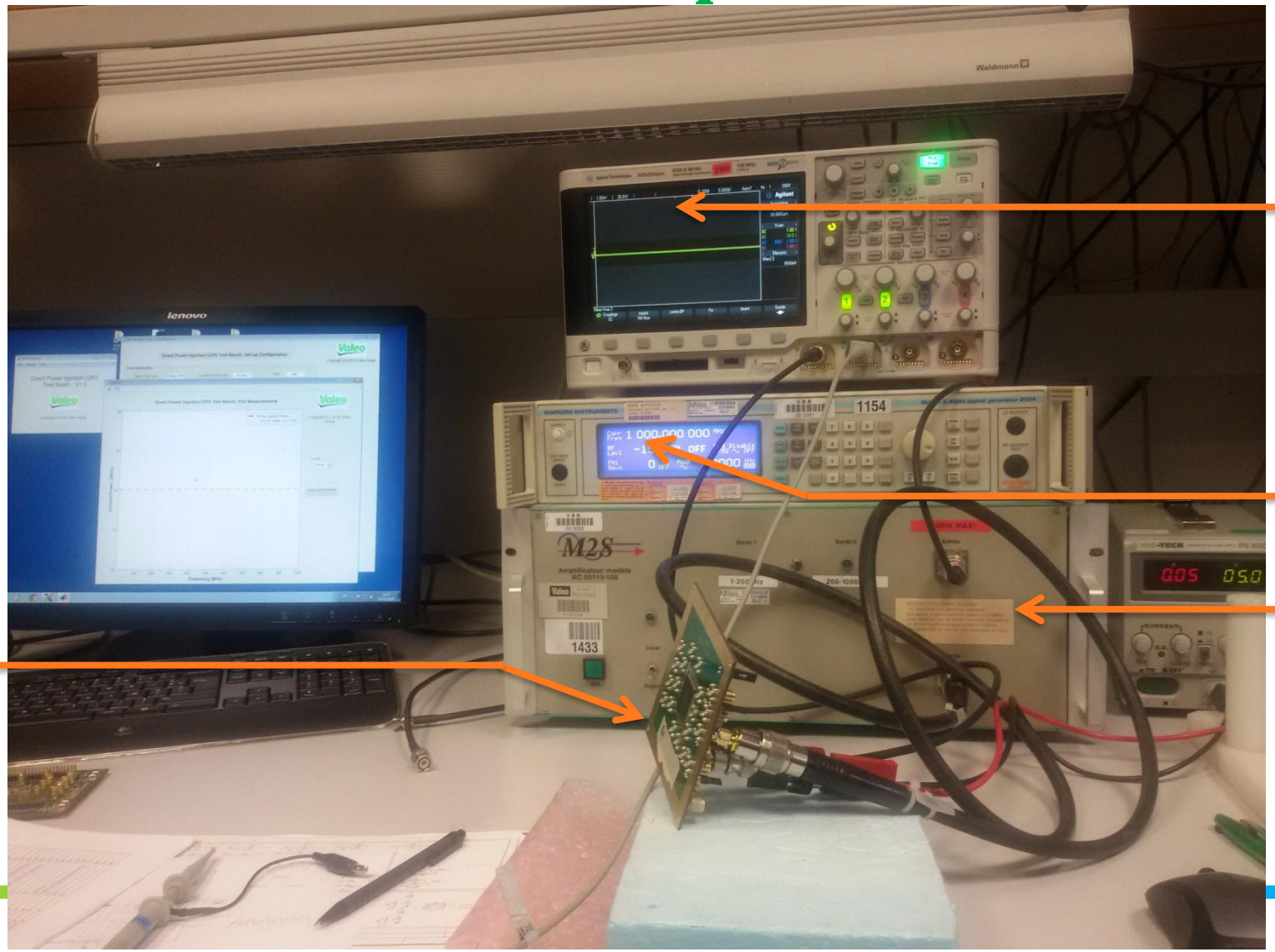
PCB tracks will be the principal carriers of noise.

DPI Theory

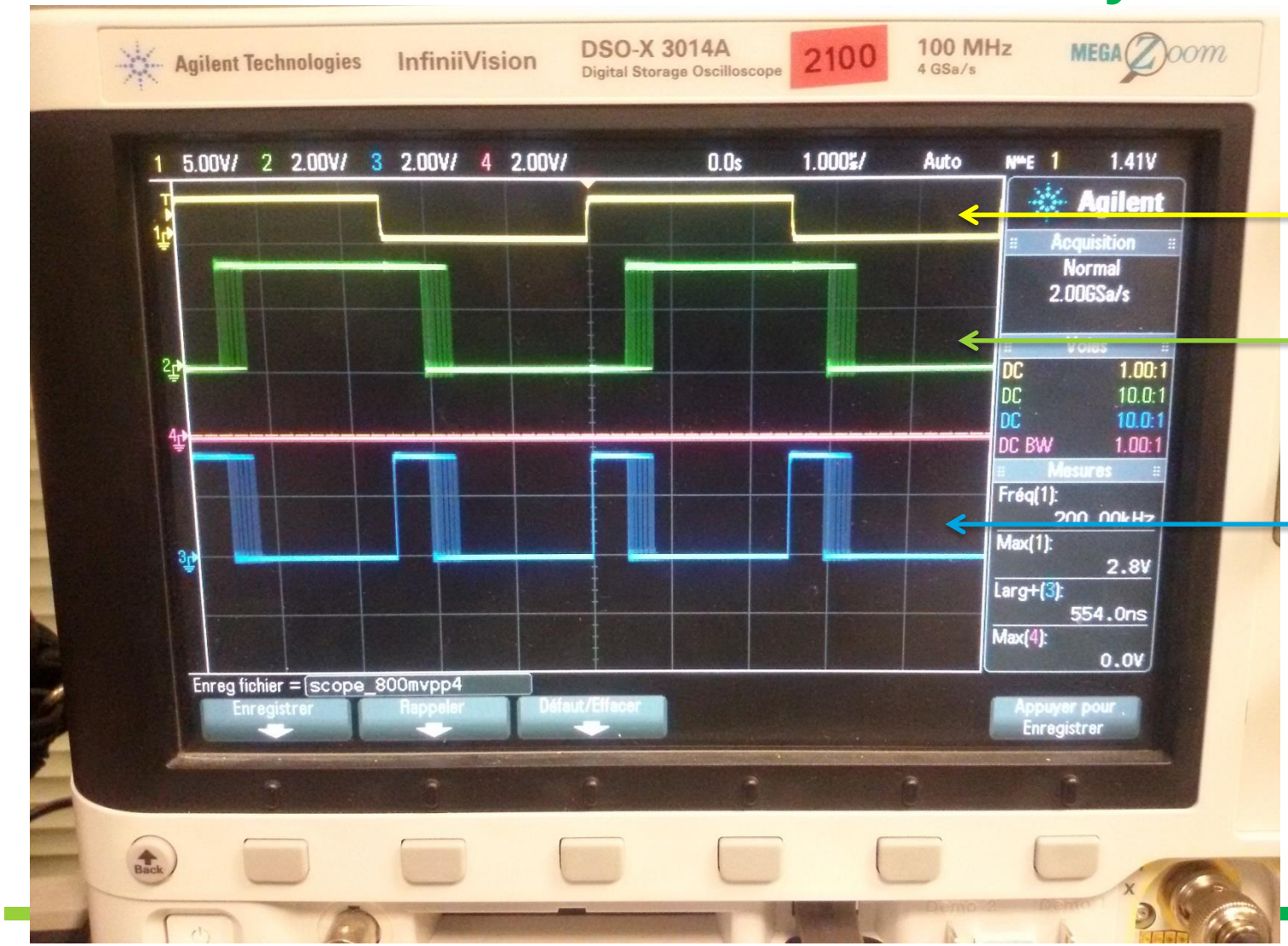

CW
AM 80 %
50 Ω coax
Directional coupler
DC supply or signal generator
Test PCB
Decoupling network
DC Block
RF amplifier
RF injection port
DUT
P_{for}
P_{refl}
RF generator
RF Power meters
Optional: control PC
BUS
DUT monitor
IEC 2649/05


Start
$f = f_{start}$
$P = P_{specified} - x$ dB
Increase P
Wait dwell time
DUT fail? or specified power level reached ?
No
Yes
Increase f
Save frequency and last level where DUT is OK
No
$f = f_{stop}$?
Yes
End
IEC 2654/05

DPI Setup



Delay

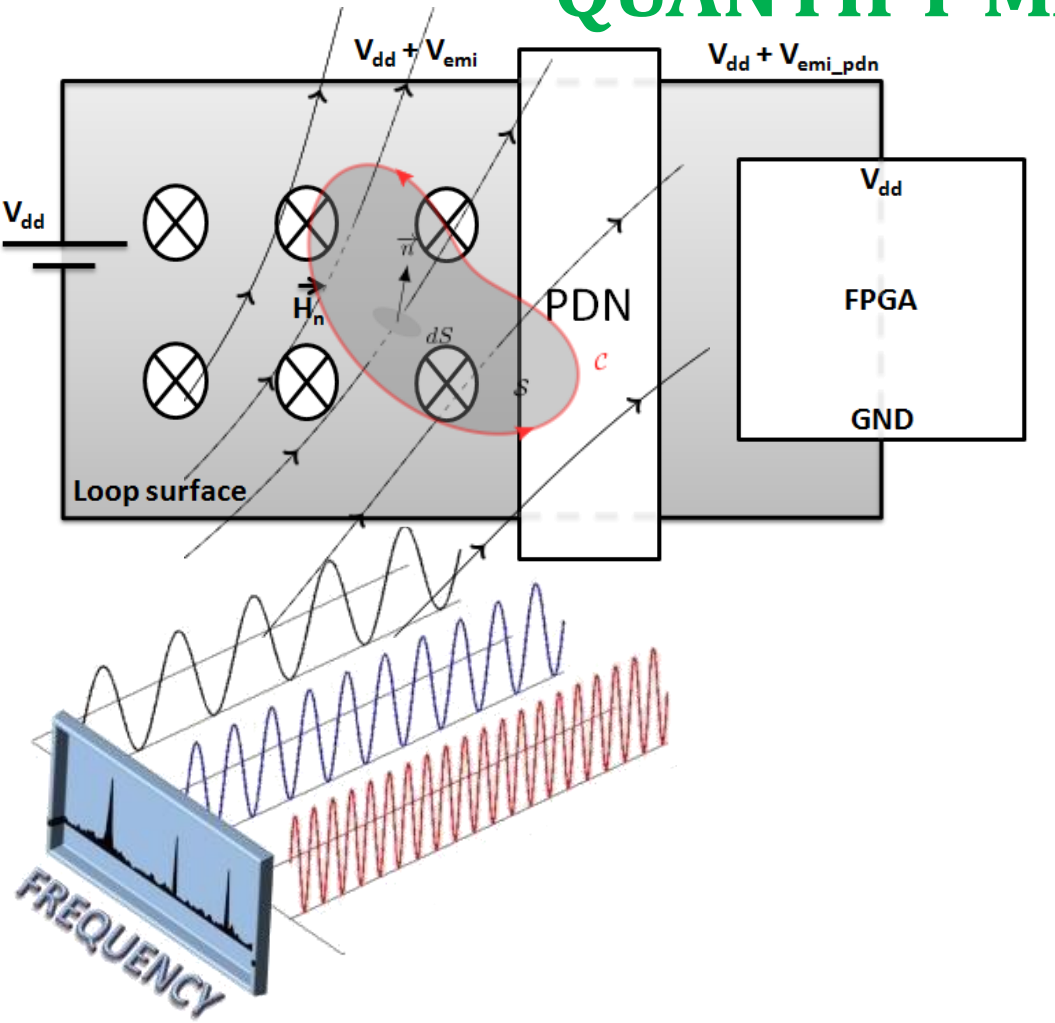


p_in

p_out

p_delay

QUANTIFY MAGNETIC FIELD EFFECTS



- ***Maxwell-Faraday :*** $\oint_C \vec{E} \cdot d\vec{\ell} = -\iint_S \frac{\partial \vec{B}}{\partial t} \cdot \vec{n}\, dS$

$$V_{EMI} = \omega \mu H_n S$$

$$V_{emi}(t) = 2.\pi.F.\mu_0.H_n.S\ sin(2\pi Ft)$$ **(Temporal evolution)**

$$V_{emi_N}(t) = \sum_{i=1}^{N} 2.\pi.F_i.\mu_0.H_n(F_i).S\ sin(2\pi F_i t)$$

- In the presence of a magnetic field, this magnetic field will couple onto the power supply plane and ***induced a parasitic voltage***.
- That parasitic voltage is proportional to the ***loop area*** formed by the power supply lines, the ***frequency*** of the magnetic field and the ***PDN transfer function*** (Power Distribution Network).

FPGA Under Test

Source Model (Geometry)

Source

Settings (Current, Frequency, etc.)

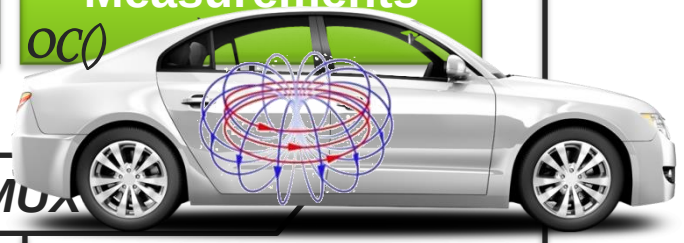
PCB Topology (Loop Surface, PDN)

FPGA Magnetic Sensitivity Tests

Electromagnetic Solver

Measurements

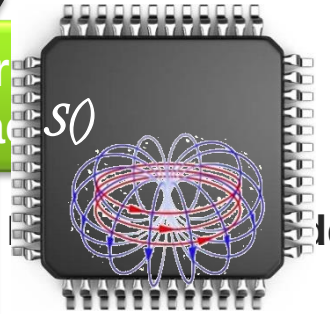
(Hx, Hy, Hz)



PHASE 2

FPGA magnetic Sensitivity (delay, jitter, etc.)

Parametr Extra



del

PHASE 1

FFT

Frequency Spectrum

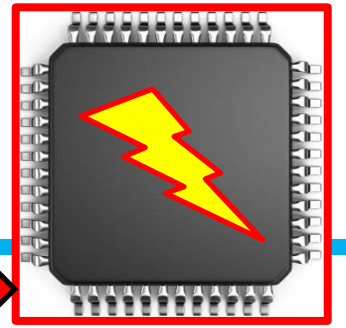
Magnetic Coupling

Induced Voltage

Effects Quantification on FPGA

PHASE 3

Effects on FPGA (delay, jitter, etc.)



FPGA Under Test

Source Model (Geometry)

Source

Settings (Current, Frequency, etc.)

PCB Topology (Loop Surface, PDN)

FPGA Magnetic Sensitivity Tests

Electromagnetic Solver

(Hx, Hy, Hz)

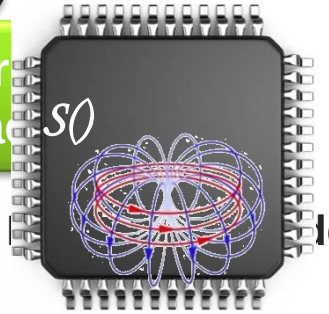
MUX

PHASE 2

FPGA magnetic Sensitivity (delay, jitter, etc.)

FFT

Parametr Extra



lel

Frequency Spectrum

Magnetic Coupling

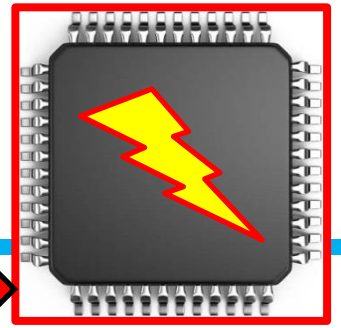
PHASE 1

Induced Voltage

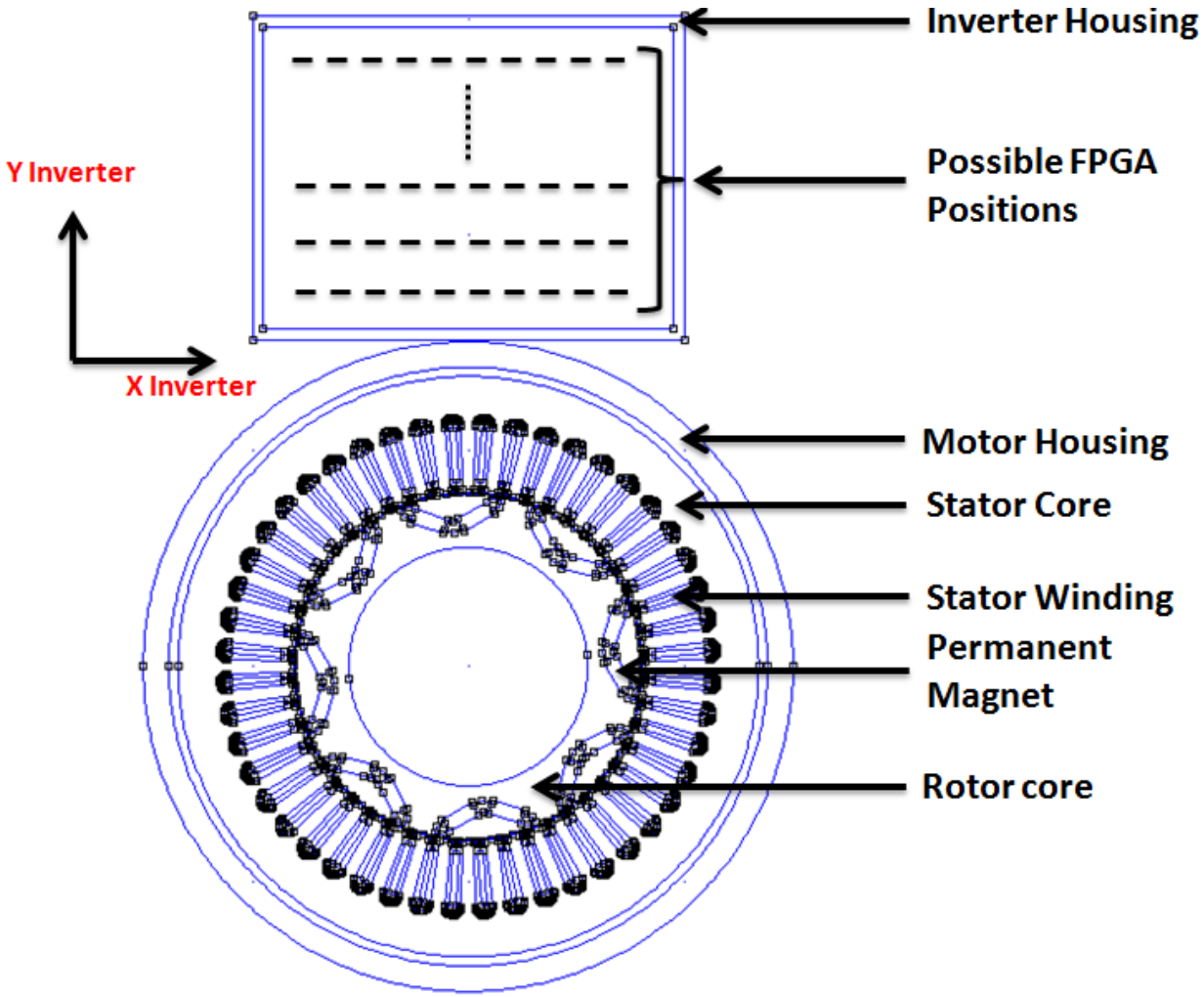
Effects Quantification on FPGA

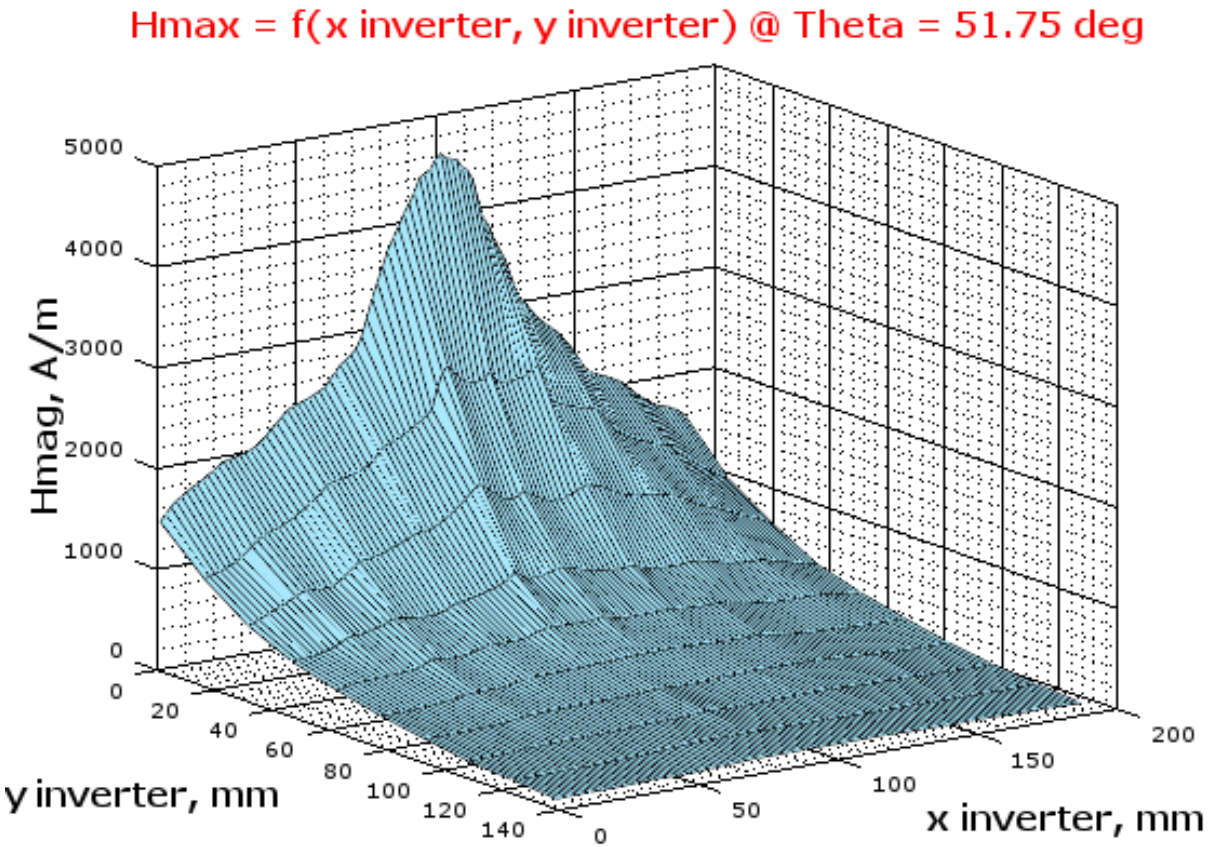
PHASE 3

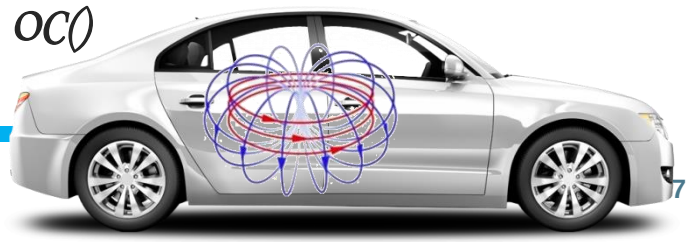
Effects on FPGA (delay, jitter, etc.)



SIMULATION RESULTS

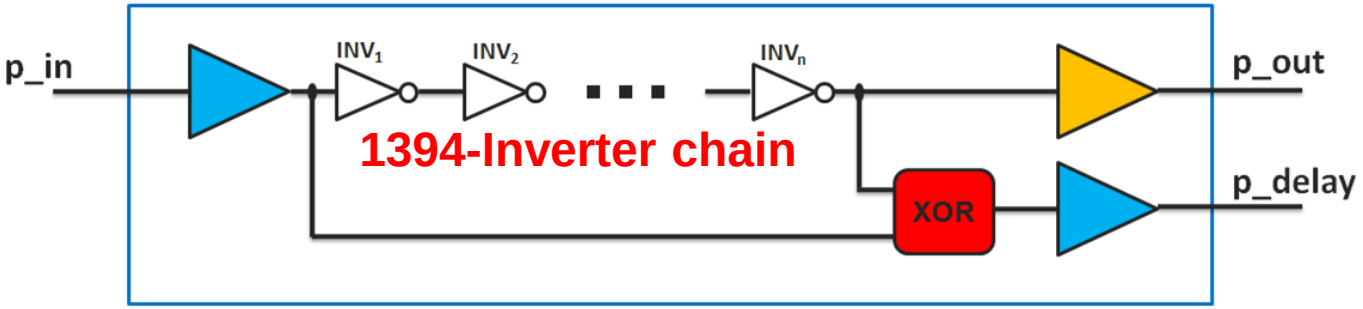


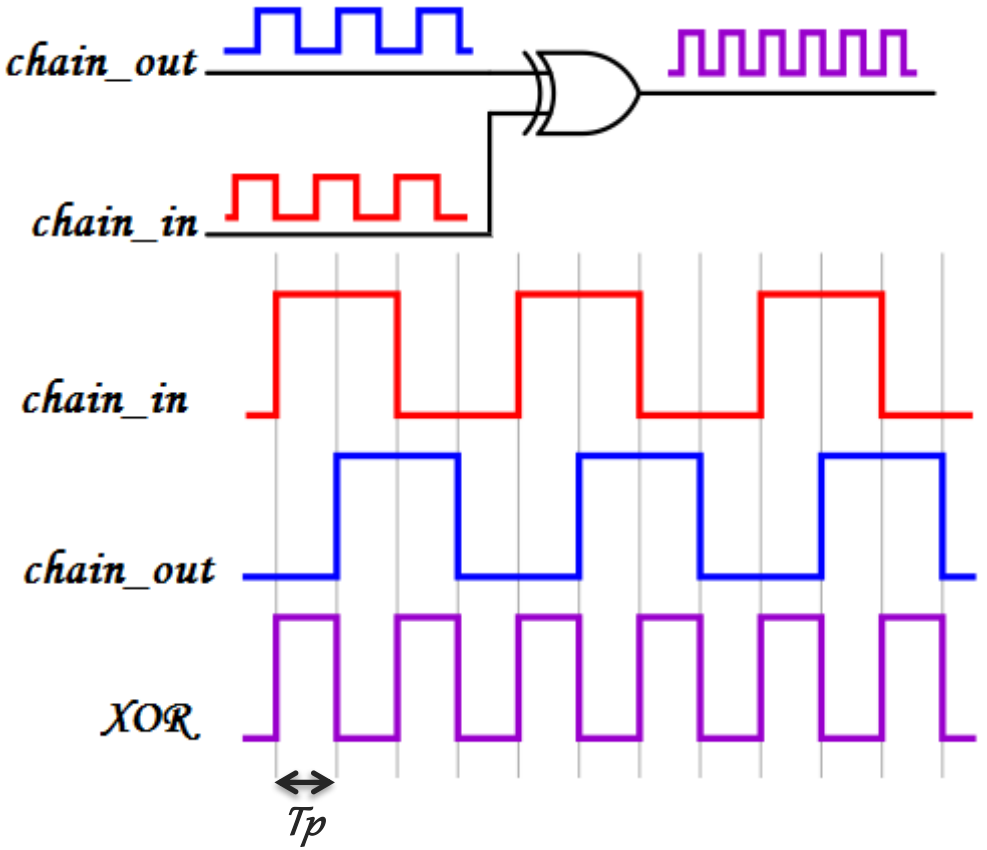




Magnetic Field at base speed (1194 rpm) with $I_S = I_{SMAX}$ ($I_D = 0$, $I_Q = I_{SMAX}$).

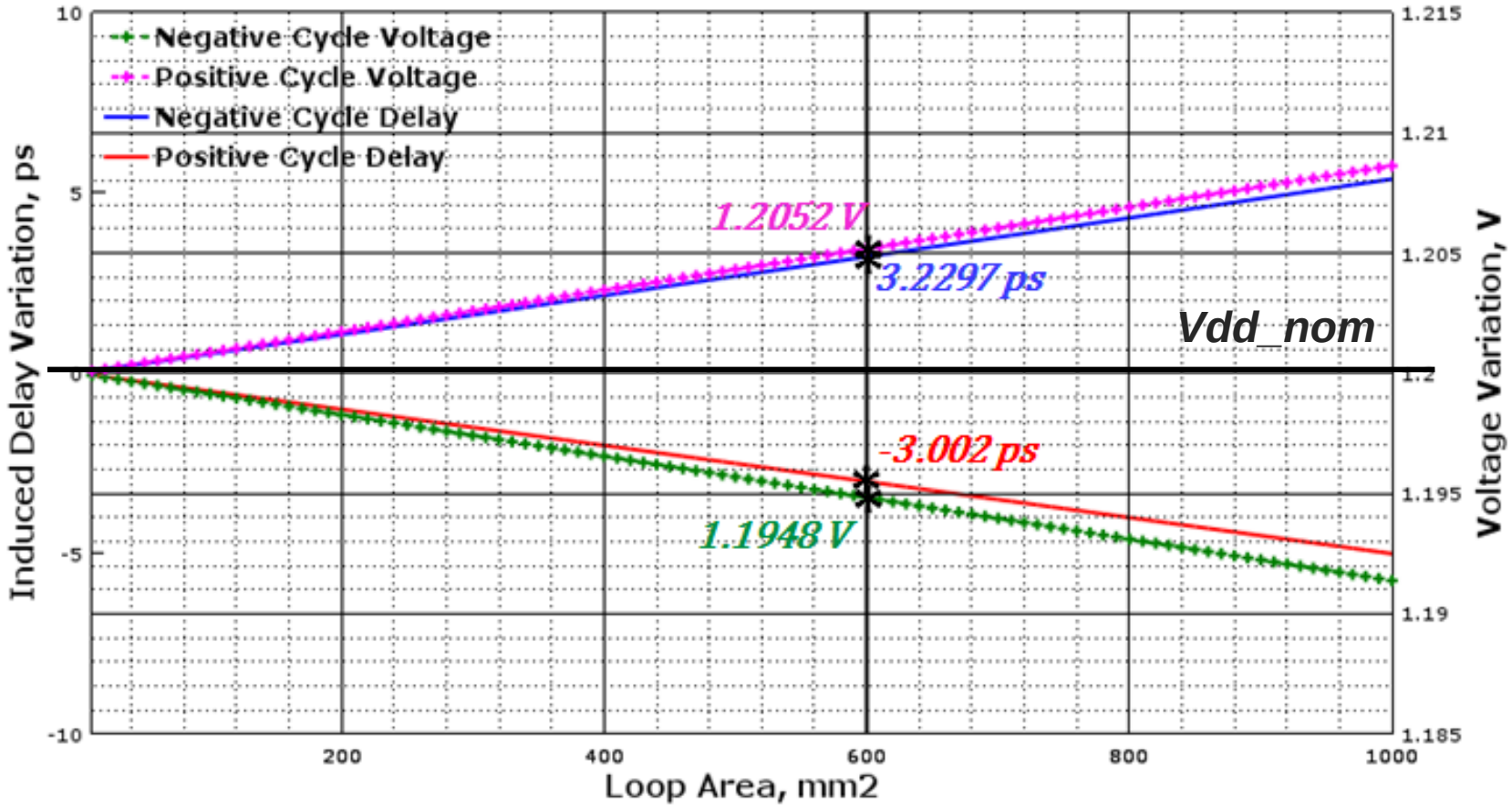
PROPAGATION DELAY EVALUATION





The propagation delay is the time a signal will take to go through a gate.

FPGA PARAMETRIC MODEL



- ***The patterned lines represent the voltage variation (right axis),***
- ***The solid lines represent the induced delay variation (left axis),***

@600 mm2 :

- **FPGA voltage variation from 1.1948 V to 1.2052 V. (~ 10,4 mV)**
- **Delay variation of -3.002 ps to 3.2297 ps at ambient temperature.**

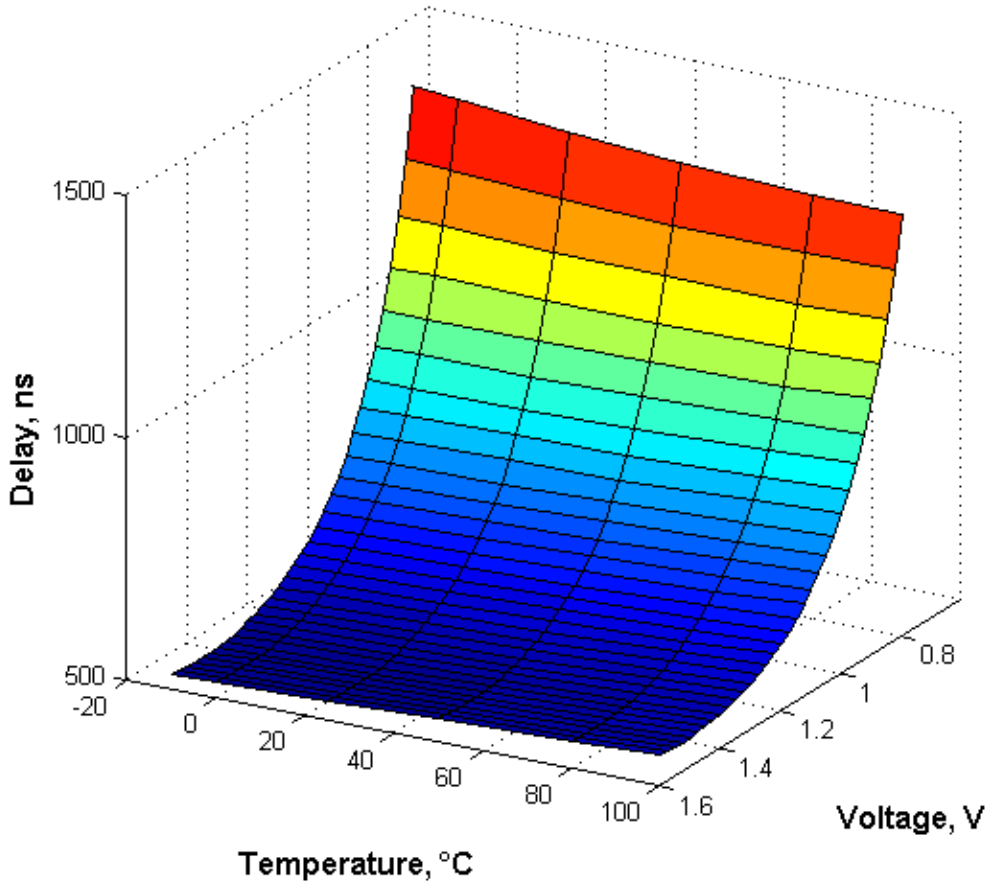
For one LUT only.

DELAY CHARACTERIZATION

$$T_{plh} = \frac{C_L \left[\frac{2|V_{th,p}|}{V_{dd} - |V_{th,p}|} + ln\left(3 - 4\frac{V_{th,p}}{V_{dd}}\right) \right]}{\mu_p C_{ox} \frac{W_p}{L_p} \left(V_{dd} - |V_{th,p}|\right)}$$

Temperature

Voltage

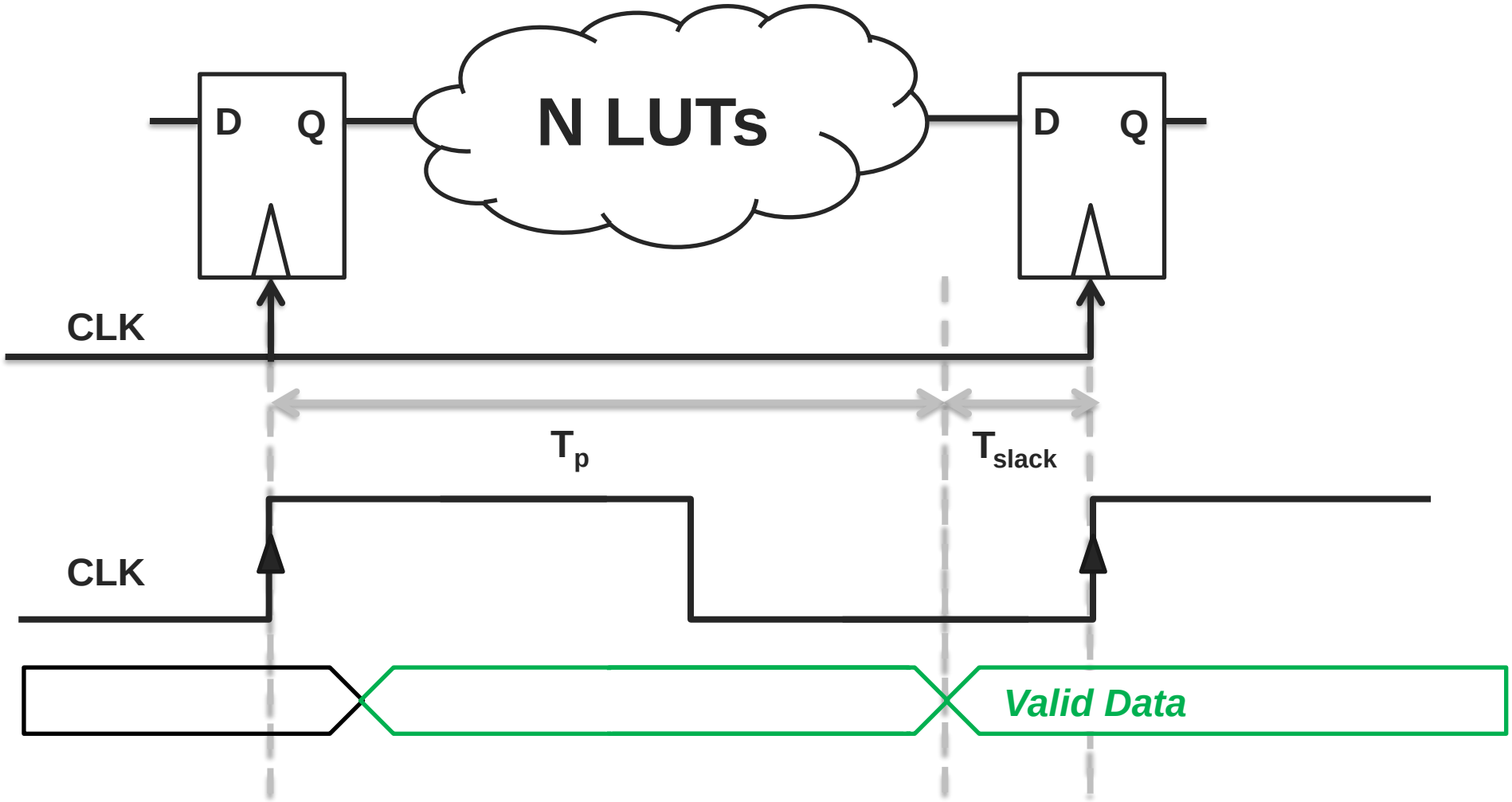


A delay is associated to a voltage and a temperature.

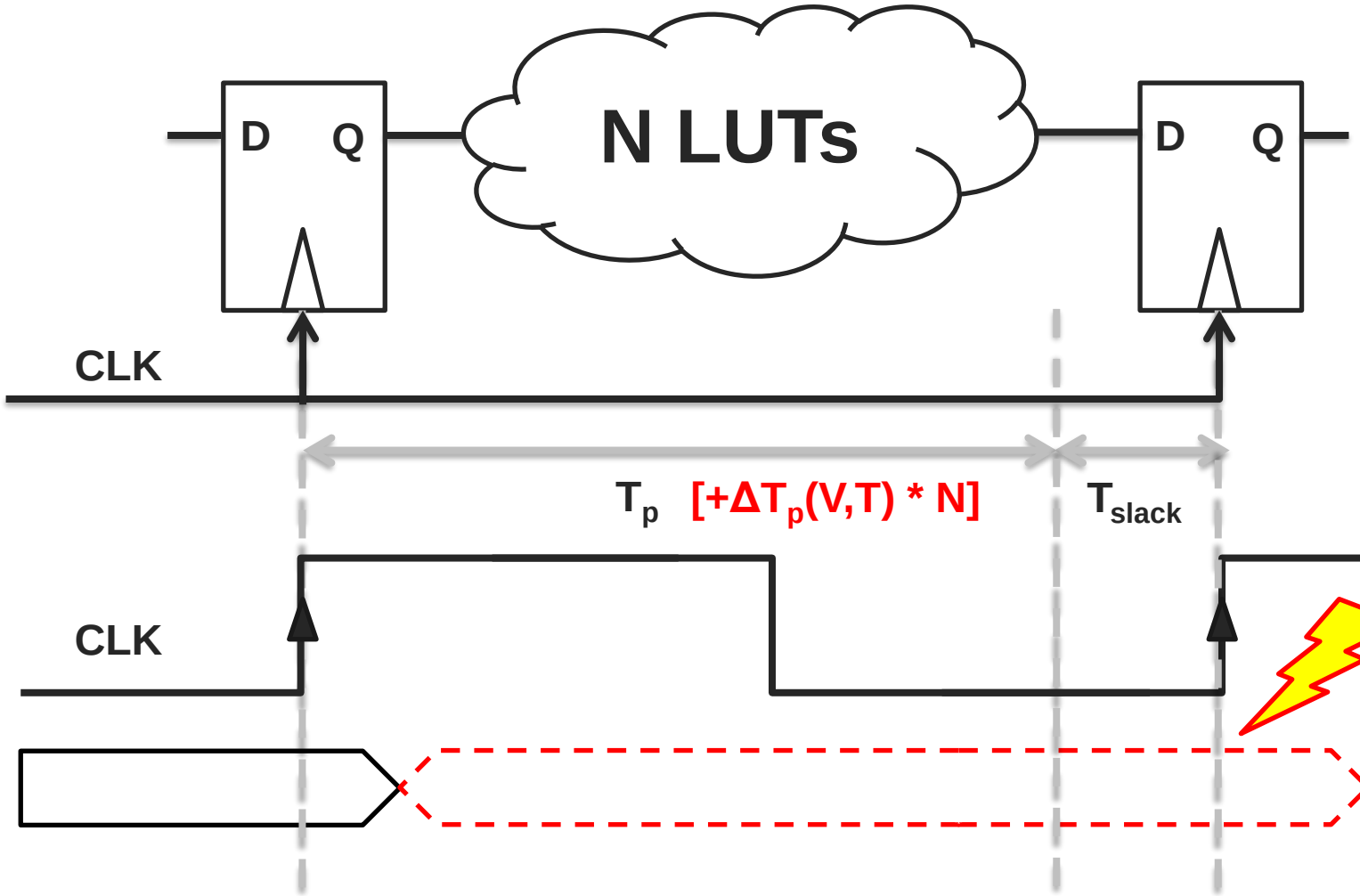
The effect of an electromagnetic field is also dependant on the temperature.

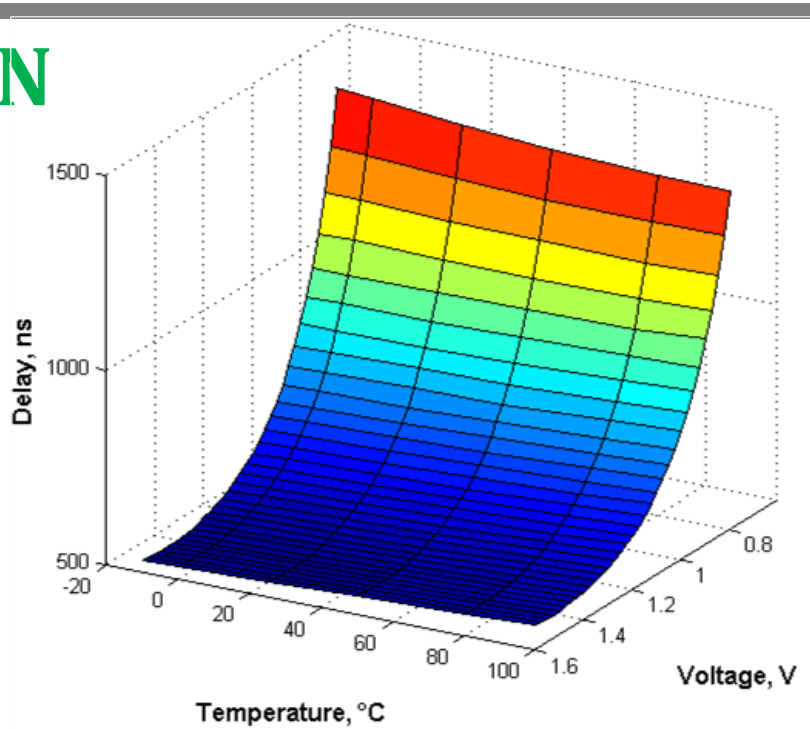
LUT block

EFFECT ON A DESIGN

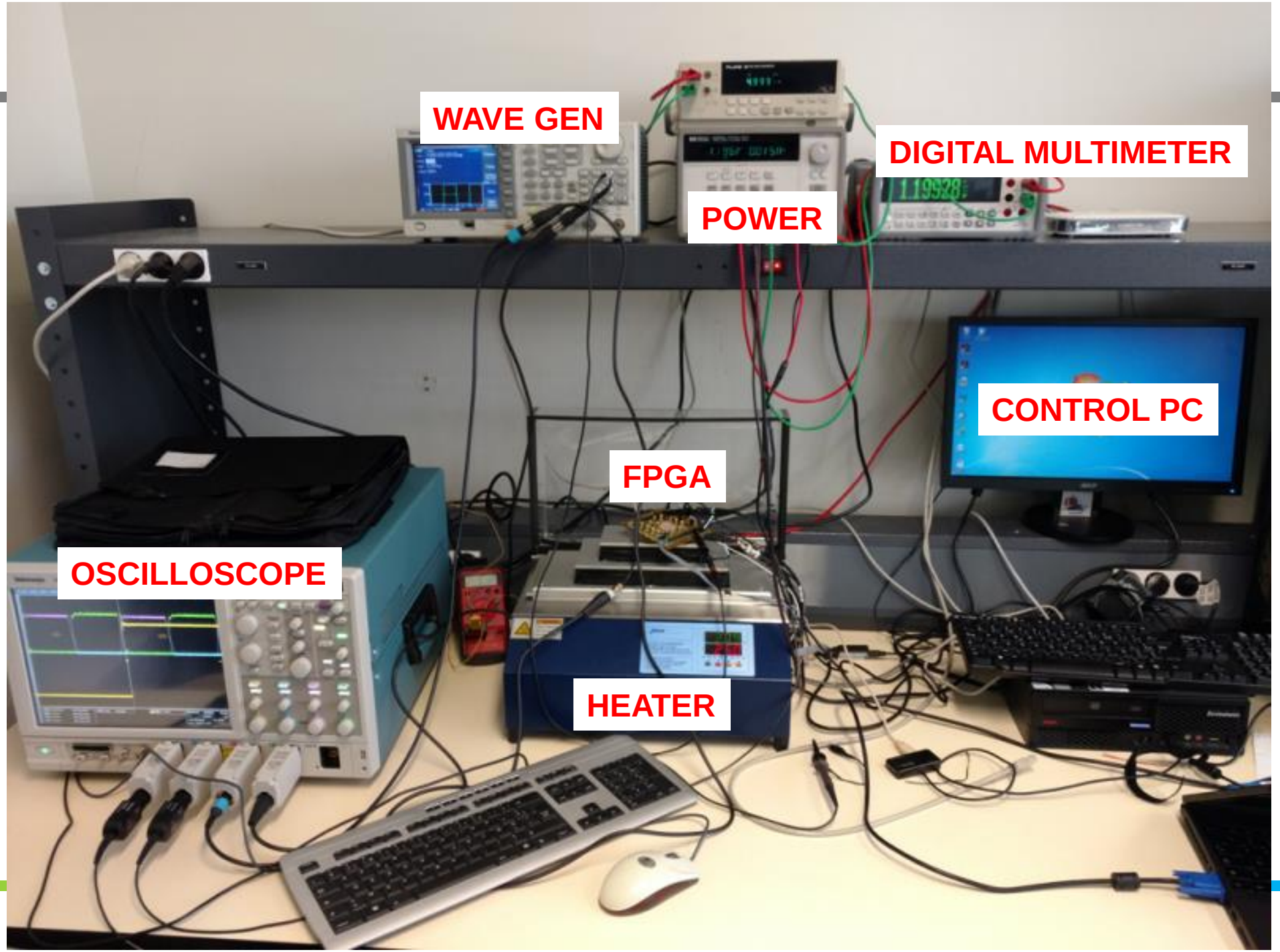


EFFECT ON A DESIGN

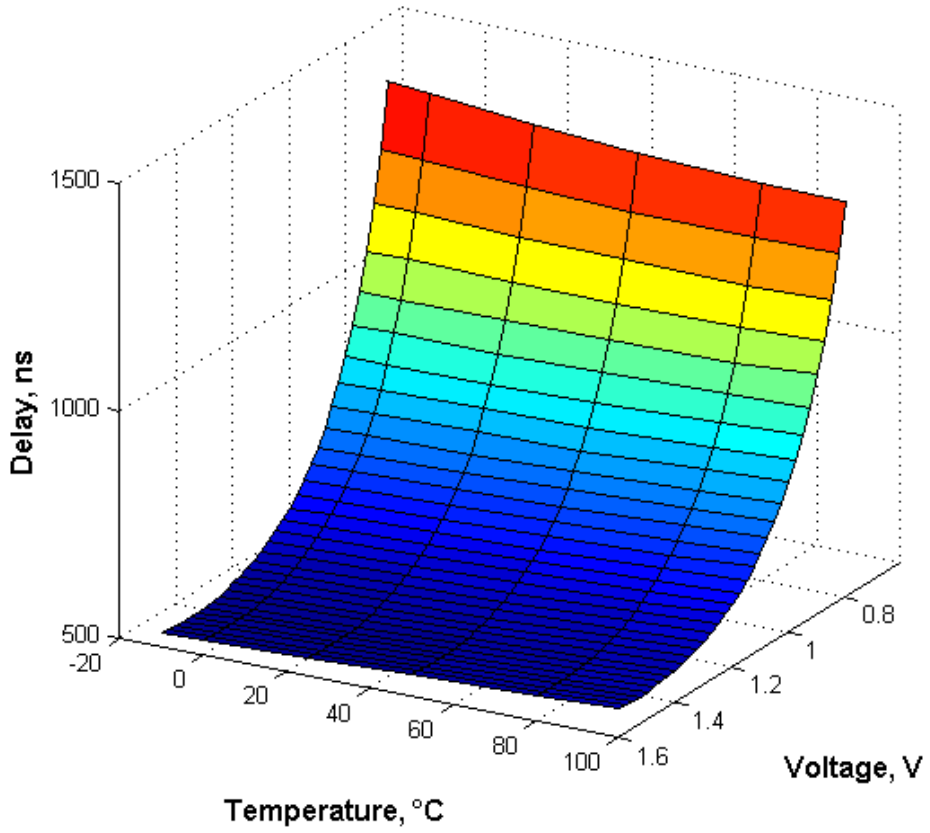




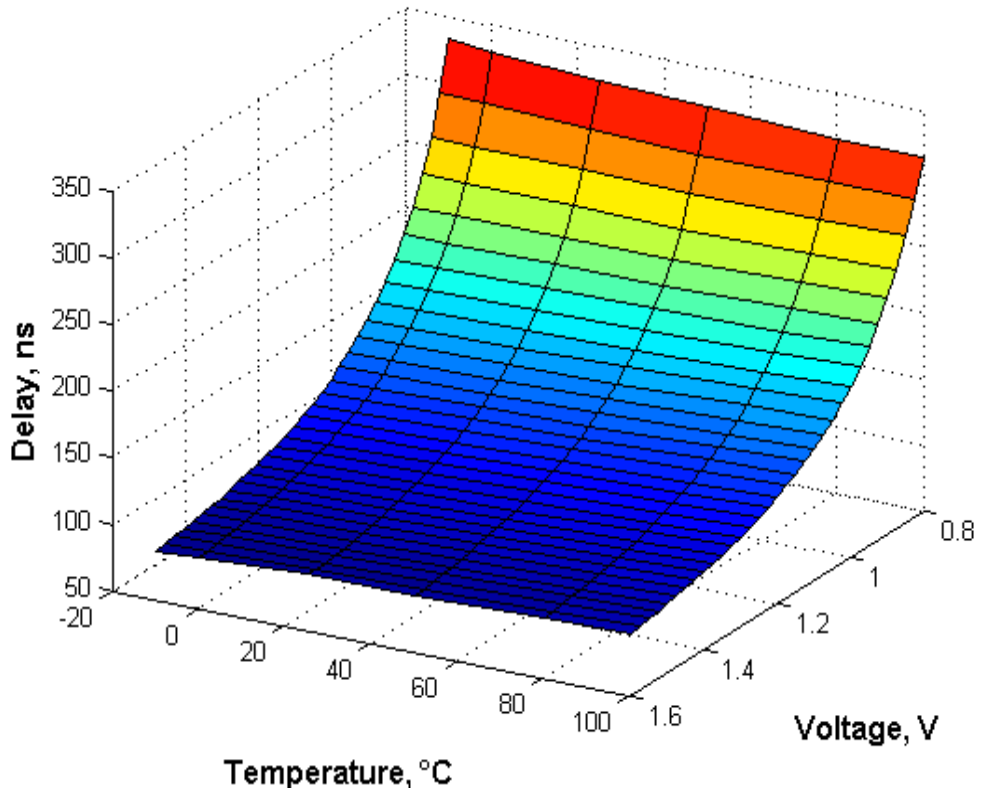
⚠ *The induced voltage, in conjunction with the ambient temperature, could cause runtime errors !*


WAVE GEN
DIGITAL MULTIMETER
POWER
CONTROL PC
FPGA
OSCILLOSCOPE
HEATER

DELAY CHARACTERIZATION

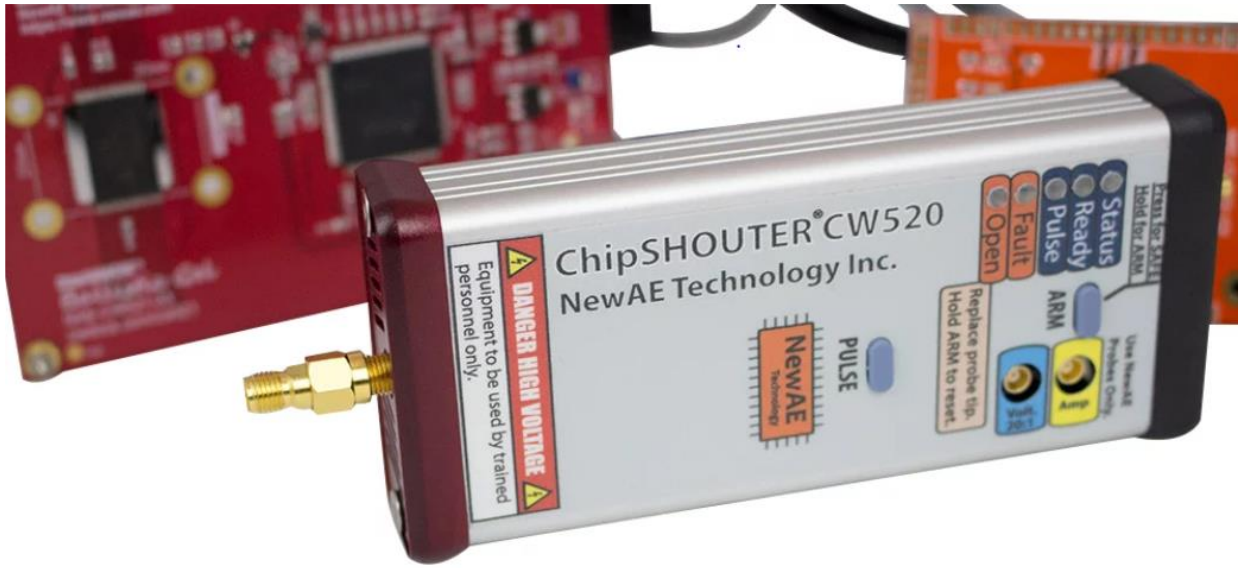


LUT block



Multiplier Block

Experimental Setup: Phase II



Parameters of the ChipShouter:

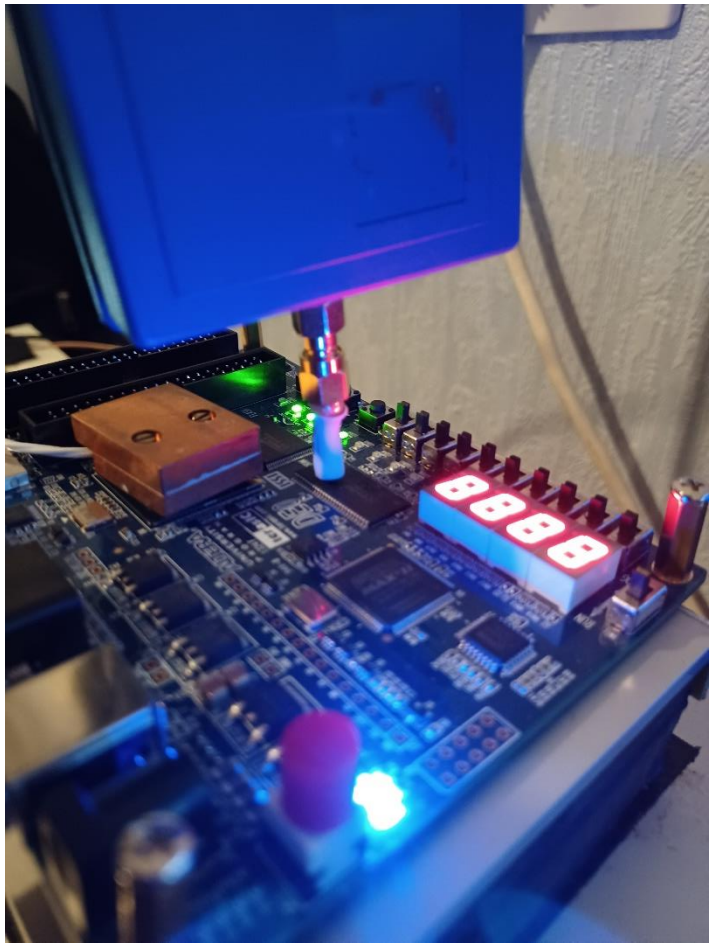
1) Pulse voltage (up to 500v)
2) Pulse width
3) Pulse repeat
4) Pulse deadtime
5) 4 probe tips of varying size and polarities

At IC level we can modify:

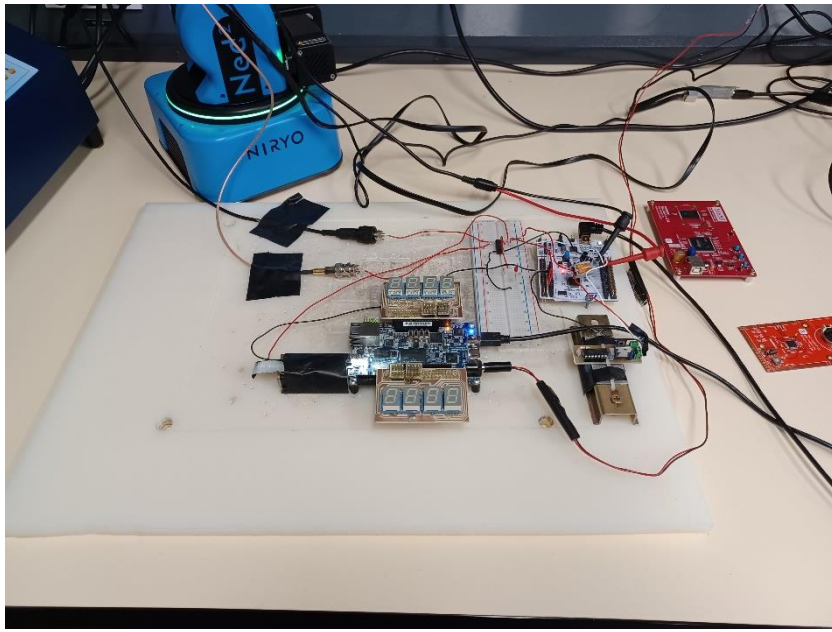
1) Power (voltage)
2) Temperature
3) DUT (Design Under Test)


```
# armed:g p
# pulse width                          80ns .............[pulse width (nS)]
# pulse width                          80ns(measured) ...[pulse width (nS)]
# pulse repeat                         10000 Repeat .....[pulse repeat (tim
es)]
# pulse deadtime                       500msec ..........[pulse deadtime (m
S)]
```

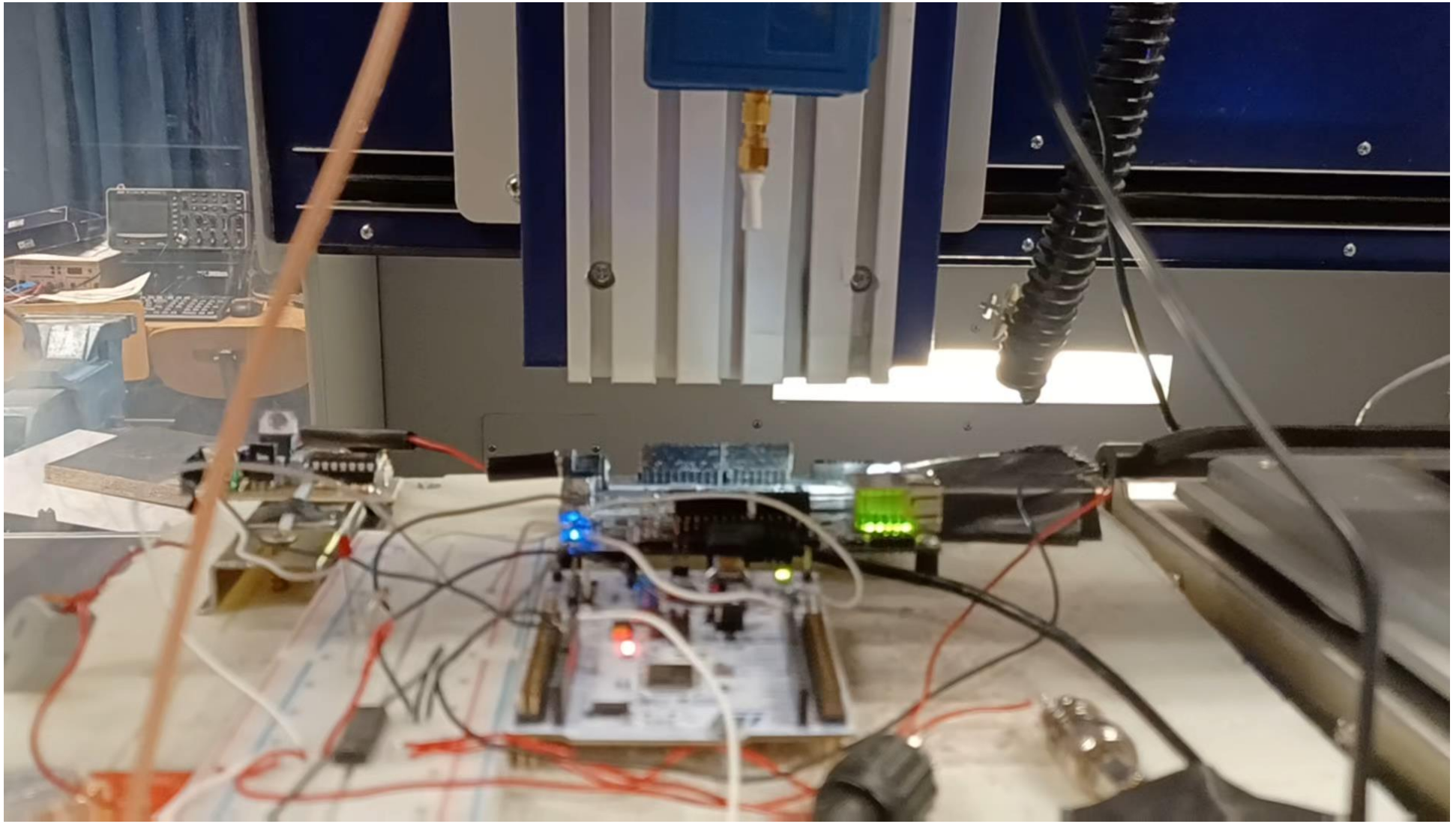
Experimental Setup



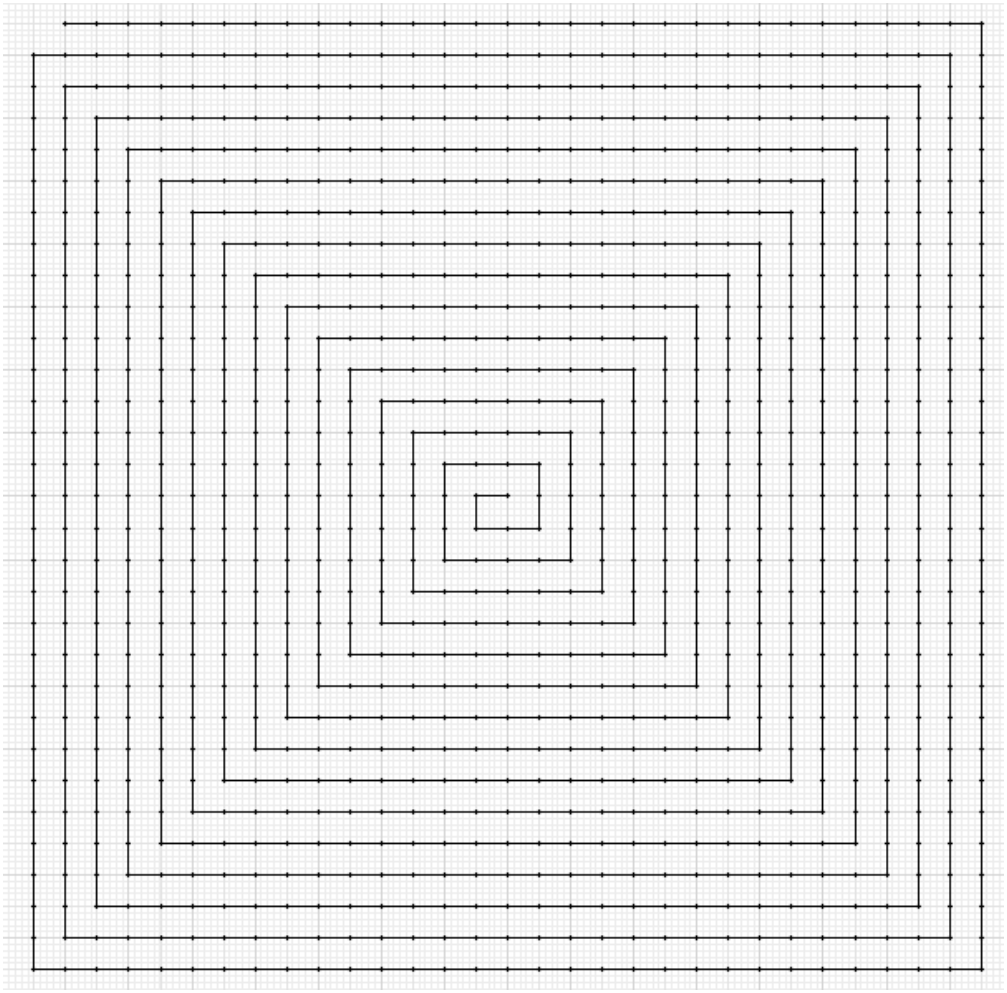
Perfect synchronisation in time and space
to be able to reproduce the same effect at each injection compaign

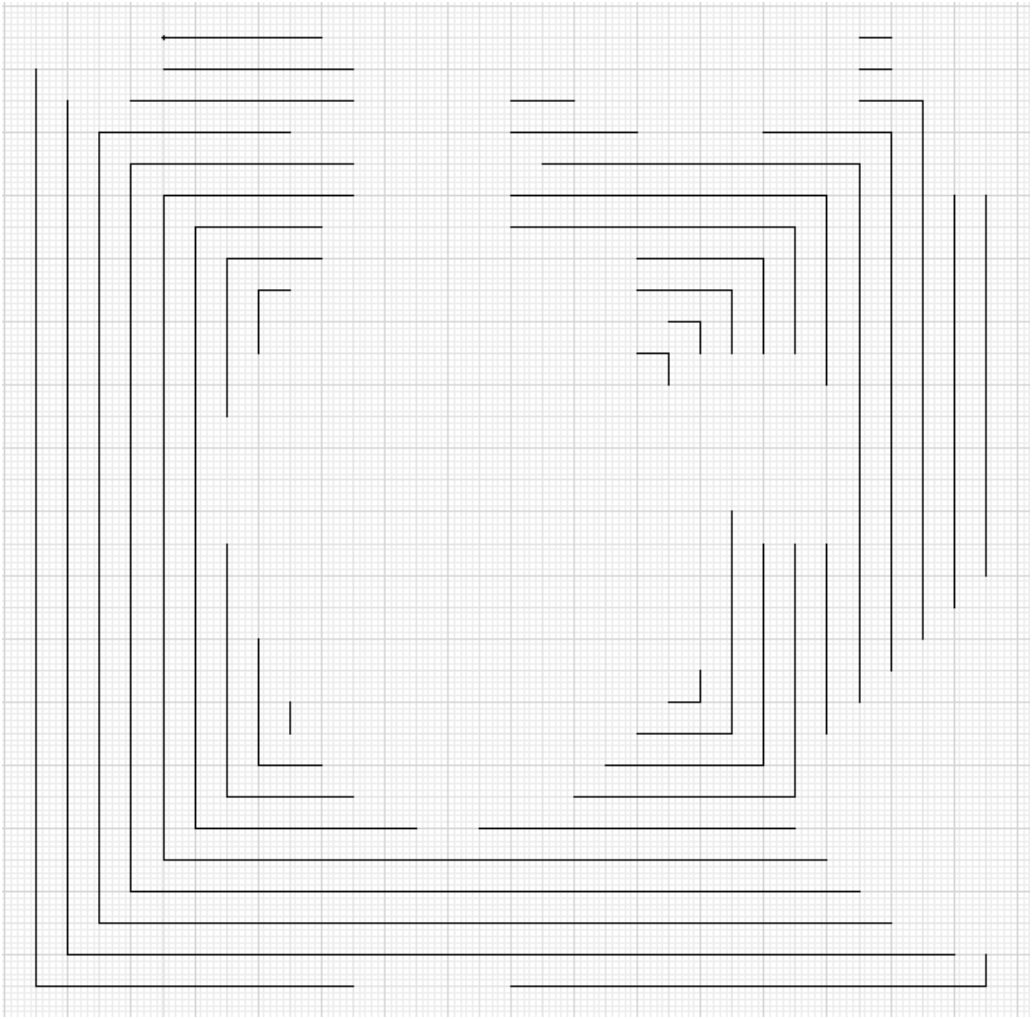


Experimental Setup



Preliminary results for the Configuration Memory (SRAM)

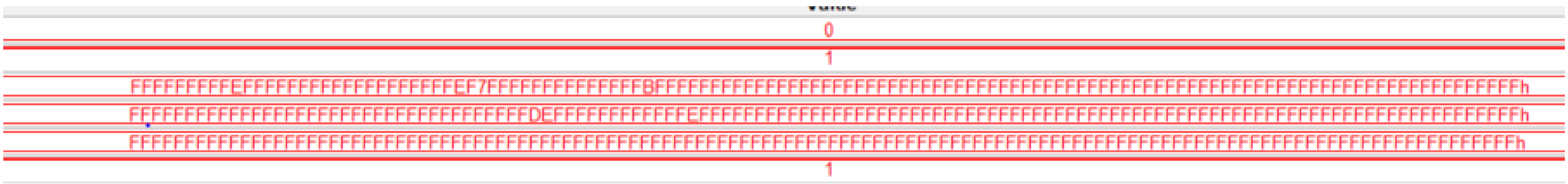




Before radiation by EMFI

After radiation by EMFI and removing sensitive points (inducing reconfiguration)

Preliminary results for the Configuration Memory (SRAM)



Example of errors on the buffers at the outputs of inverters chains

Preliminary results for the SDRAM

```
# Debut de LECTURE de la memoire SDRAM:
# FIN LECTURE.
debut d attente de 7s
fin de 7s
Cessez le feu

# Debut de LECTURE de la memoire SDRAM:
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095319] = 808
il y a 1 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095359] = 8000000
il y a 2 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095575] = 808
il y a 3 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095615] = 8080000
il y a 4 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096087] = 200
il y a 5 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096127] = 2000000
il y a 6 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096343] = 808
il y a 7 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096383] = A080000
il y a 8 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096599] = 808
il y a 9 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096639] = 8080000
il y a 10 error au total dans la SDRAM
# FIN LECTURE.
debut d attente de 7s
fin de 7s
Cessez le feu

# Debut de LECTURE de la memoire SDRAM:
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095319] = 808
il y a 1 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095359] = 8000000
il y a 2 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095575] = 808
il y a 3 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095615] = 8080000
il y a 4 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096087] = 200
il y a 5 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096127] = 2000000
il y a 6 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096343] = 808
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ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096383] = A080000
il y a 8 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096599] = 808
il y a 9 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096639] = 8080000
il y a 10 error au total dans la SDRAM
# FIN LECTURE.
debut d attente de 7s
fin de 7s
Cessez le feu
```

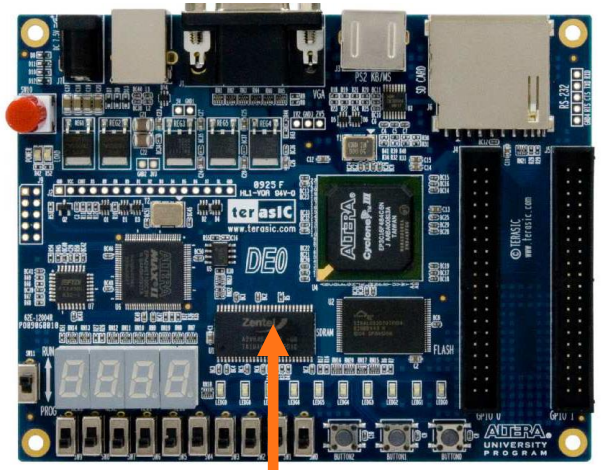

8 MB SDRAM

Different pattern of data:
0xFFFF FFFF
0x0000 0000
0xF0F0 F0F0
0xFF00 FF00
0xFFFF 0000
Etc…

```
# Debut de LECTURE de la memoire SDRAM:
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095319] = 808
il y a 1 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095359] = 8080000
il y a 2 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095575] = 808
il y a 3 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095615] = 8080000
il y a 4 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096087] = 200
il y a 5 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096127] = 2000000
il y a 6 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096343] = A08
il y a 7 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096383] = A080000
il y a 8 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096599] = 808
il y a 9 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096639] = 8080000
il y a 10 error au total dans la SDRAM
# FIN LECTURE.
debut d attente de 7s
fin de 7s
Cessez le feu

# Debut de LECTURE de la memoire SDRAM:
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095319] = 808
il y a 1 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095359] = 8080000
il y a 2 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095575] = 808
il y a 3 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2095615] = 8080000
il y a 4 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096087] = 200
il y a 5 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096127] = 2000000
il y a 6 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096343] = A08
il y a 7 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096383] = A080000
il y a 8 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096599] = 808
il y a 9 error au total dans la SDRAM
ERRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRRROR at SDRAM[2096639] = 8080000
il y a 10 error au total dans la SDRAM
# FIN LECTURE.
debut d attente de 7s
```

Problem of reproducibility of results !!!

SUMMARY

I. Motivations

II. State of the Art

III. Contributions

IV. Conclusion and Perspectives

CONCLUSION

❑ *The aim of this work is to ensure the reliability of FPGAs when used in the drive-system of an electric car.*

❑ *In this work, we improved the state of the art by studied how an electromagnetic field affect an FPGA and a methodology has been proposed to quantify the effects.*

❑ *EMFI is a good solution for rapid validation of proposed mitigation techniques*

PERSPECTIVES

❑ ***Flash-based FPGAs can also benefit from the developed methodologies as they are sensitive to voltage and temperature variation.***

❑ ***Combined effects of electromagnetic field, temperature and radiation hasn't been analyzed, but the methodologies have been developed to offer the possibility to be extended to these effects as presented.***

Thank you!