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Error rate prediction for programmable circuits: methodology, tools and studied cases

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Abstract:

Perturbations provoked by Single Event Upsets (SEUs) increase with the reduction of transistor's features. In this talk will be presented a strategy allowing to estimate SEU error-rates based on a limited radiation ground testing and fault injection results. A flexible and versatile test platform, well suited to implement such a strategy will be described. Experimental results obtained for different processors illustrate the accuracy of error rate predictions.

Short Bio:

Dr. Raoul Velazco got the PhD and the Doctor es Sciences in Computer Sciences in 1982 and 1990 respectively, both from INPG (Institut National Polytechnique de Grenoble). With the CNRS (French Research Agency) since 1984, where he is now Director of Researches Emeritus, he was until 2019 the co-leader of the RIS (Robust Integrated circuits and Systems) research group at TIMA laboratory (Grenoble). His main research activities focus the study of radiation effects on microelectronic circuits, the design hardening techniques and the development and exploitation of experiments devoted to operate on board satellites.

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