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Mitigation of Soft Errors at Circuit Level

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Abstract:

The mitigation of soft errors (SE) should be considered in all design abstraction levels. This talk will discuss the efficiency of mitigation techniques to decrease the soft error susceptibility on the circuit/physical design levels. Several techniques are considered: transistor reordering, sleep transistors, decoupling cells, and use of Schmitt Triggers. The use of logic multi-level design improves over 45% on average the SET results for the cells evaluated. The LETth considering the work-function fluctuation (WFF) impact is smaller than the LETth at ideal conditions. When using decoupling cells, the soft error susceptibility decreases, in our test cases. The results show that a design using a sleep transistor or Schmitt Trigger is very promising for soft error mitigation.

Short Bio:

Ricardo Reis received an EE degree from Federal University of Rio Grande do Sul (UFRGS), Brazil. Ph.D. degree in Microelectronics from INPG, France. Doctor Honoris Causa by the University of Montpellier. Full professor at UFRGS. Main research includes physical design automation, MPSoC and fault tolerant systems. More than 700 publications. He received the 2015 IEEE CASS Meritorious Service Award. Founder of conferences like SBCCI and LASCAS, a CASS Flagship Conference. Member of CASS DLP Program (2014/2015). Member of IEEE CASS BoG and IEEE CEDA BoG. Member of the IEEE IoT Initiative Activity Board. Chair of IEEE CASS SiG on IoT. Ricardo received the IFIP Fellow Award 2021 and the ACM/ISPD Lifetime Achievement Award 2022.

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