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Mitigation of Soft Errors at Circuit Level

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The mitigation of soft errors (SE) should be considered in all design abstraction levels. This talk will discuss the efficiency of mitigation techniques to decrease the soft error susceptibility on the circuit/physical design levels. Several techniques are considered: transistor reordering, sleep transistors, decoupling cells, and use of Schmitt Triggers. The use of logic multi-level design improves over 45% on average the SET results for the cells evaluated. The LETth considering the work-function fluctuation (WFF) impact is smaller than the LETth at ideal conditions. When using decoupling cells, the soft error susceptibility decreases, in our test cases. The results show that a design using a sleep transistor or Schmitt Trigger is very promising for soft error mitigation.

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