CERN QTI project proposal

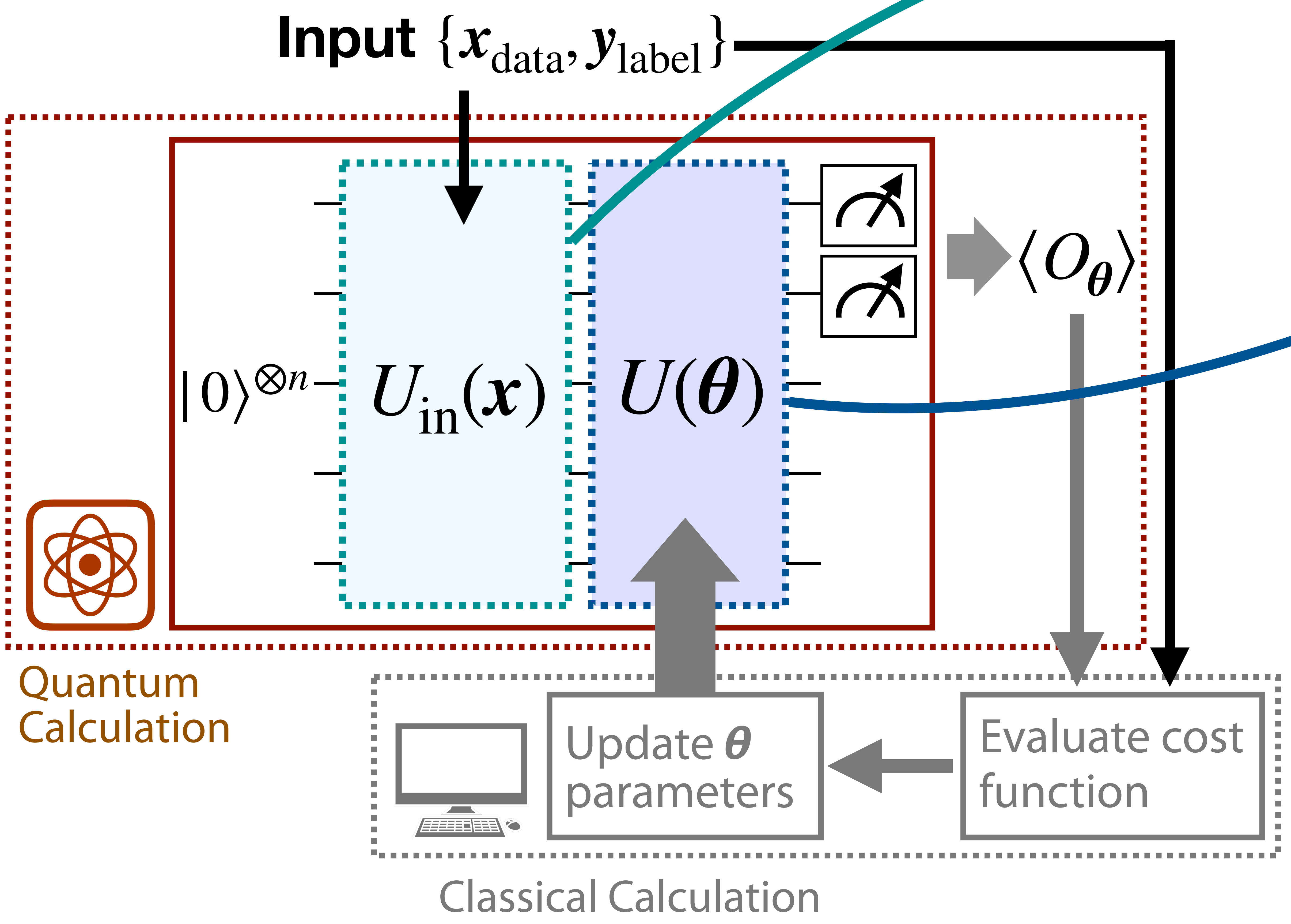
Co-designing near-term quantum architecture for HEP applications

ICEPP, University of Tokyo

Quantum Machine Learning

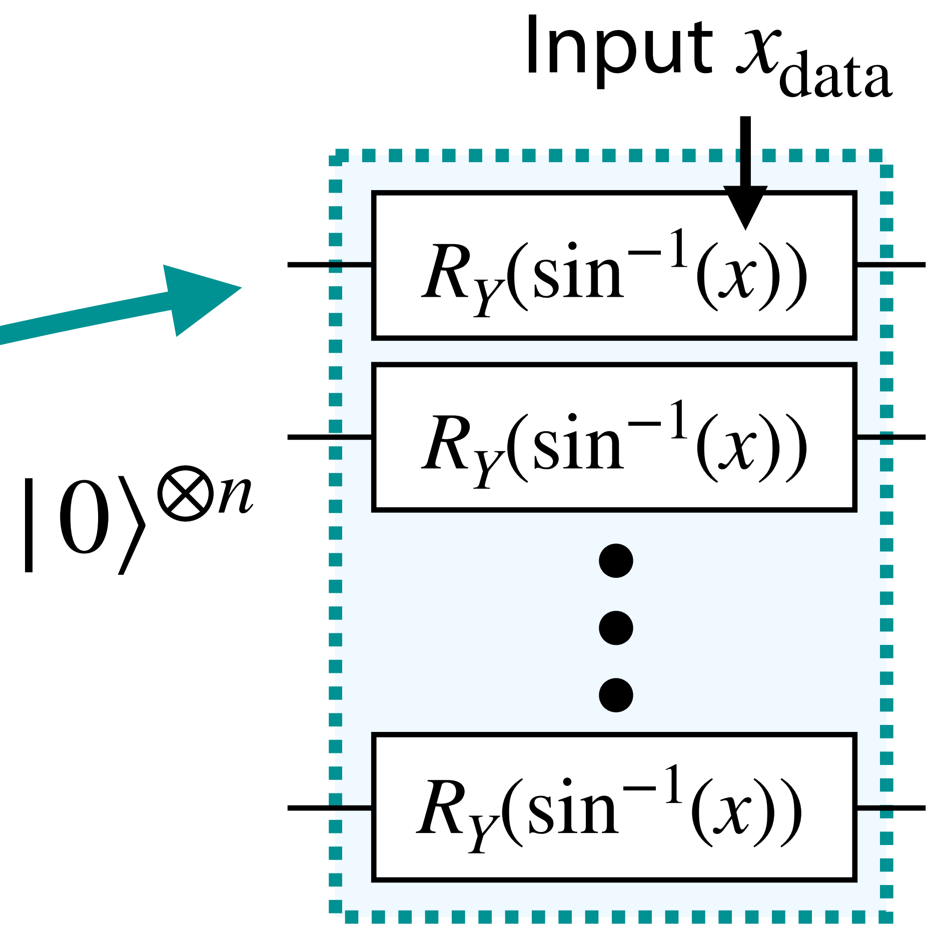
Quantum machine learning (QML) as a promising early application to HEP

Near-term architecture for QML based on variational quantum algorithm



Data encoding into Hilbert space

Data $x_i \rightarrow |\phi(x_i)\rangle = U_{\text{in}}(x_i)|0\rangle^{\otimes n}$

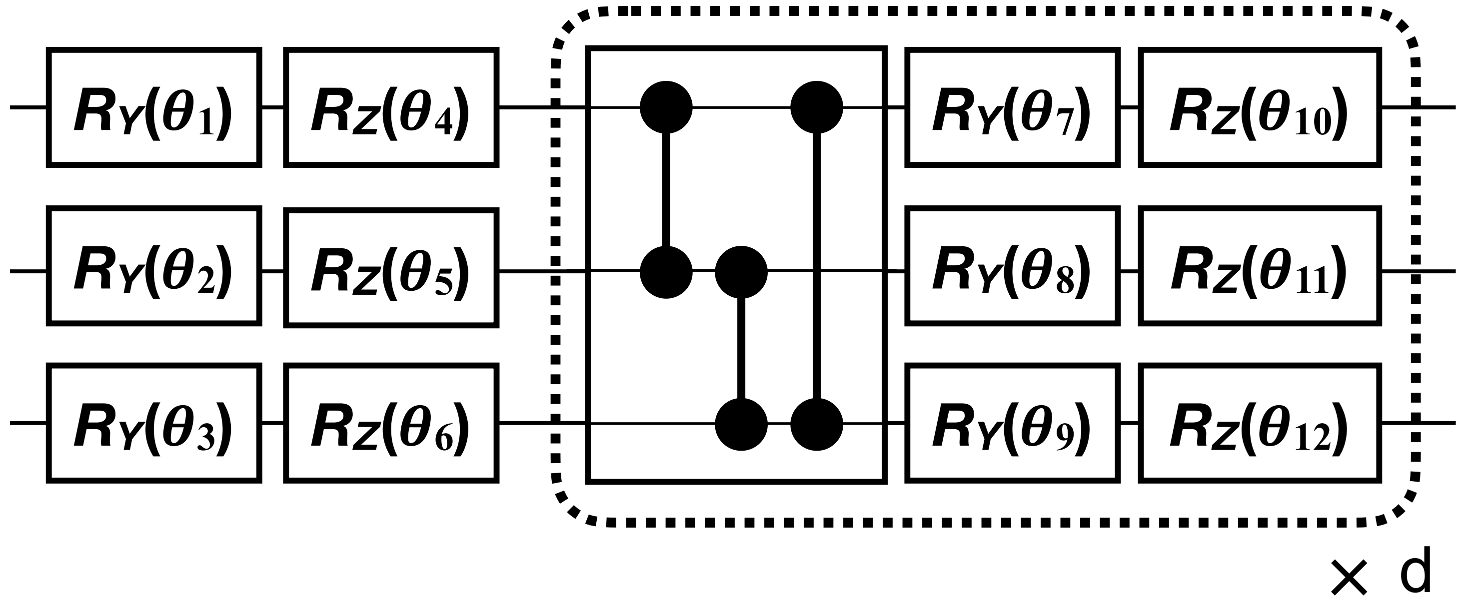


Example encoding with single-qubit rotation gates

➡ Representational complexity grows exponentially in *n*

Parameterized quantum circuit to learn the input state $|\phi(x_i)\rangle$

$$|\psi(x_i, \boldsymbol{\theta})\rangle = U(\boldsymbol{\theta})|\phi(x_i)\rangle$$



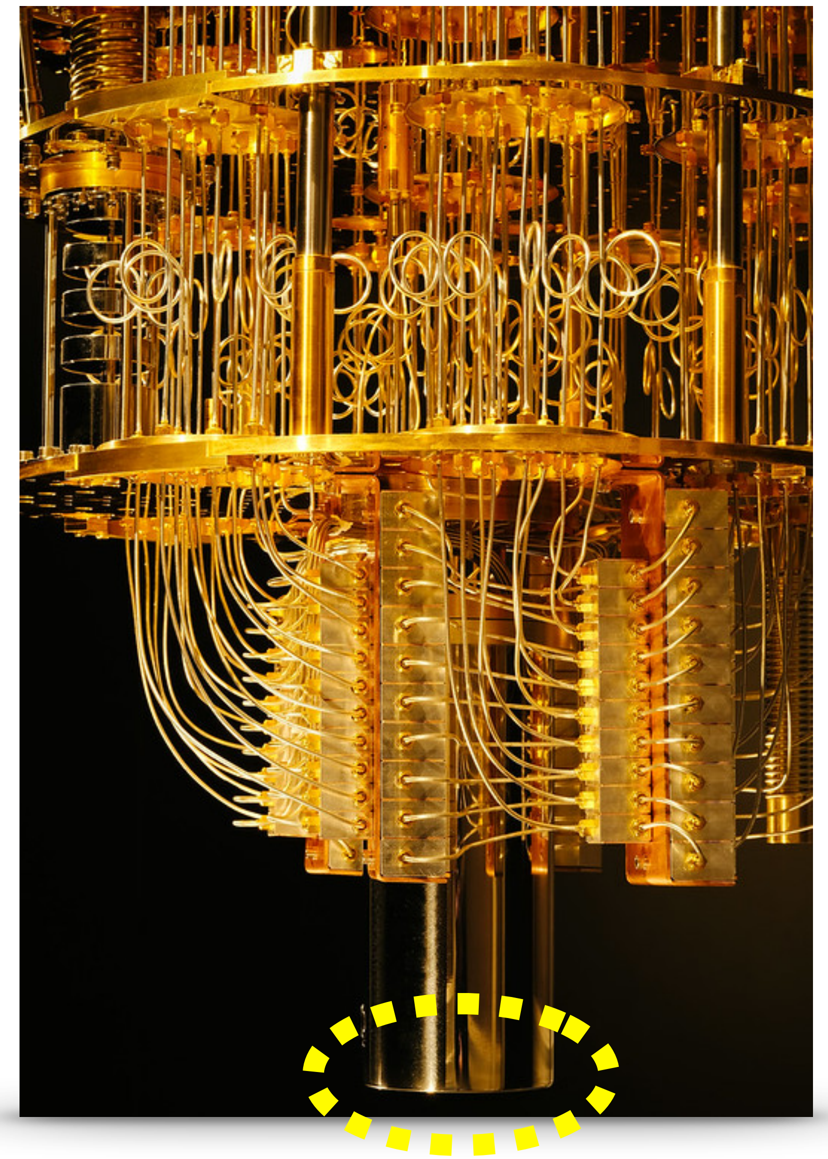
Example hardware-efficient SU(2) ansatz

➡ High expressibility with generalized ansatz that exploits large Hilbert space

Superconducting Qubit System

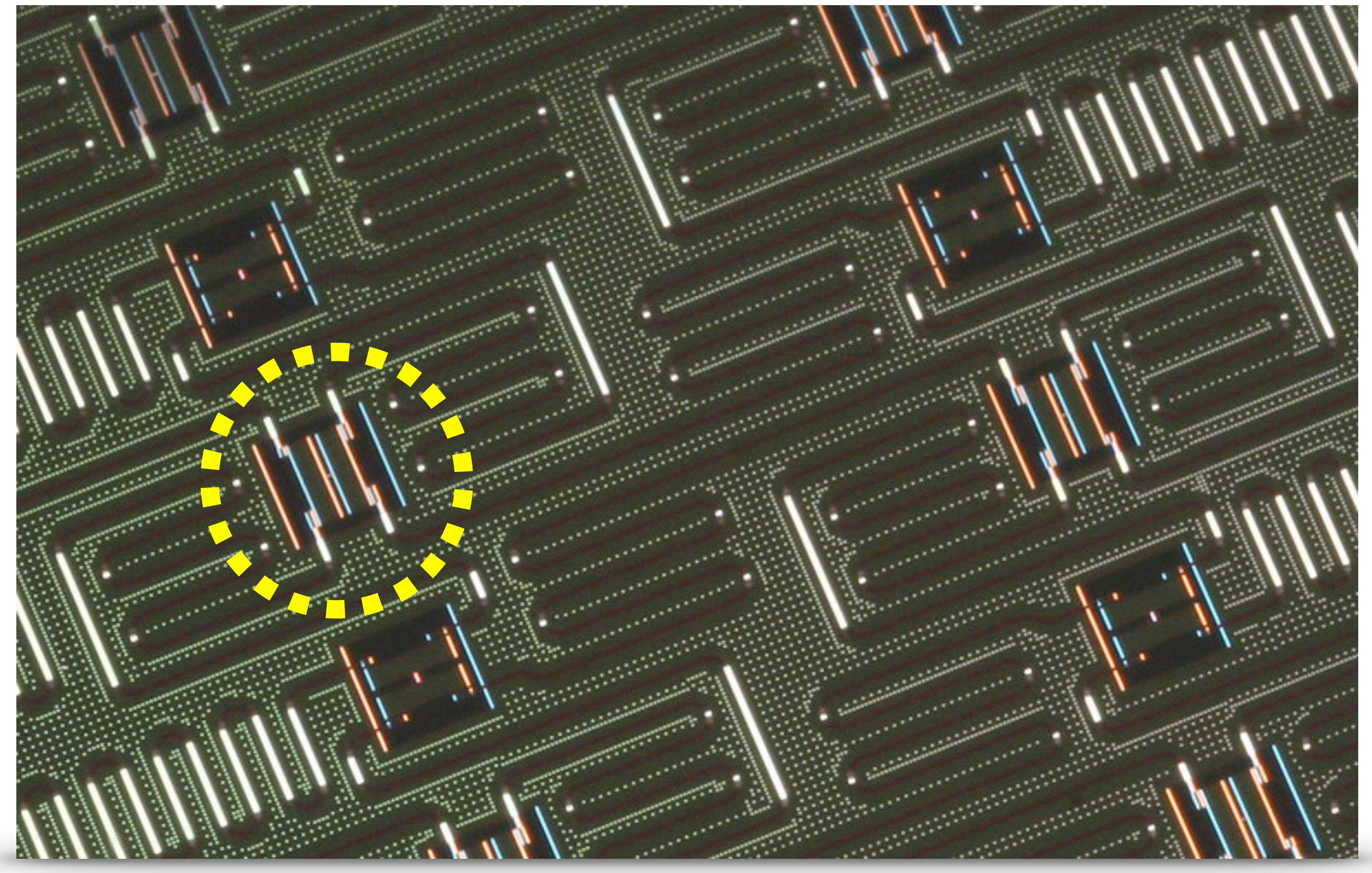
Highly hierarchical digital-analog hybrid system

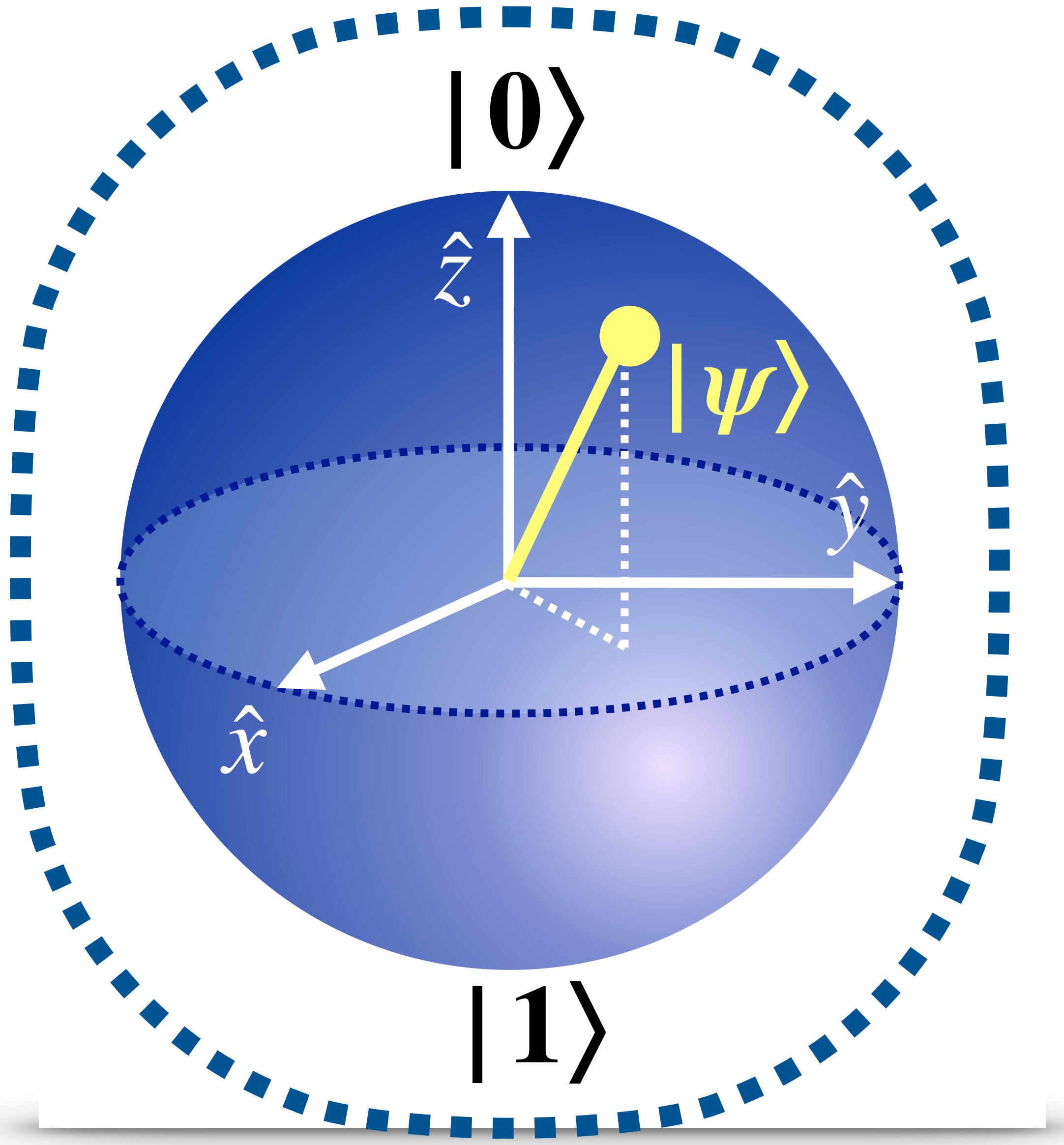
Circuit transpiration and optimization



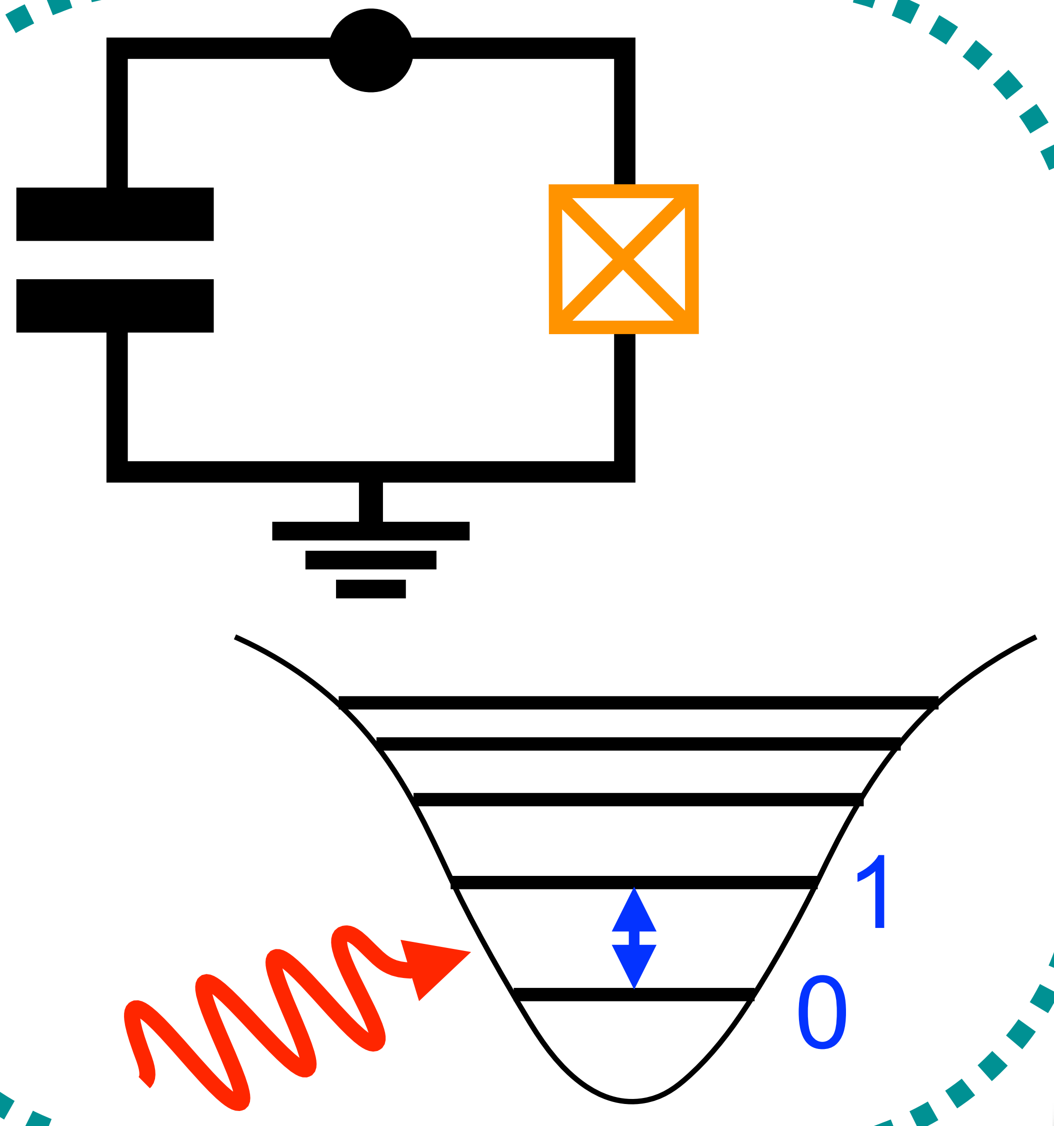
Both algorithm and implementation to hardware important for near-term device

Photo: IBM





Algorithm

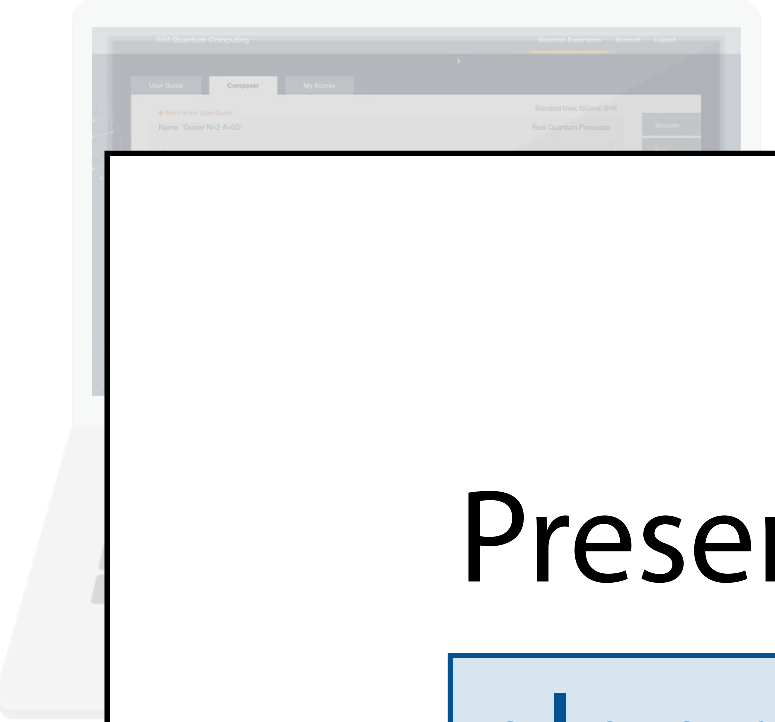


Qubit control and readout

Inspired from "Z. Minev, Superconducting Qubits, [Introduction to Circuit Quantum Electrodynamics](#)"

Superconducting Qubit System

Highly hierarchical digital-analog hybrid system



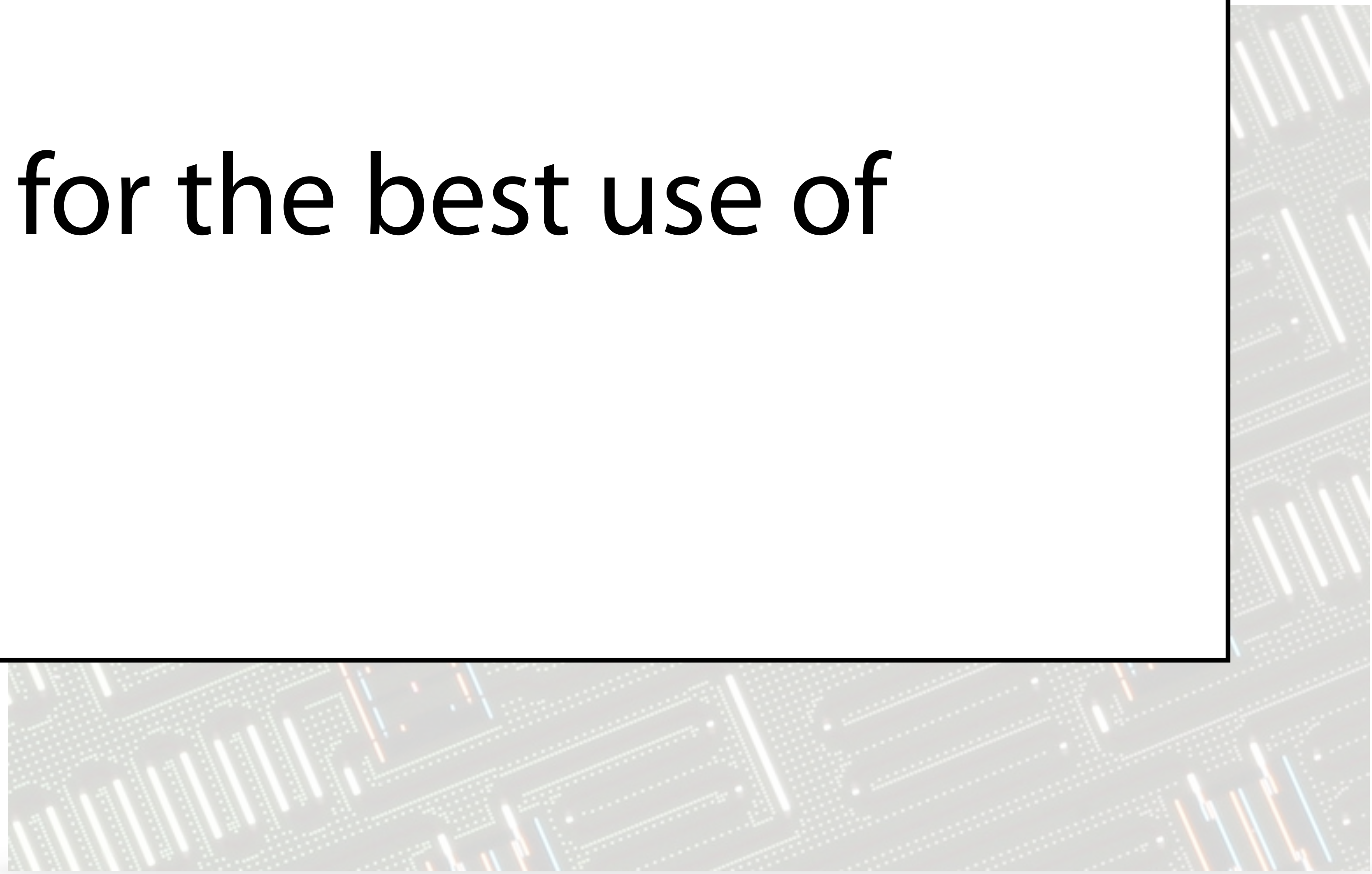
Present quantum computing architecture requires both

algorithm development and efficient implementation to hardware

for near-term quantum devices

Application-specific development would be crucial for the best use of near-term devices

IBM



Algorithm development

Qubit control and readout

Inspired from "Z. Minev, Superconducting Qubits, [Introduction to Circuit Quantum Electrodynamics]"

Proposal

Co-design near-term quantum architecture for HEP applications

Specific hardware architecture for scientific applications in long-term?

"HEP-motivated" data encoding and learning model

"HEP-desired" implementation for near-term device

Work on both aspects for a representative ML task in HEP
(e.g., classification, reconstruction, simulation)

Proposal

Specific hardware architecture for scientific applications in long-term?

Co-design near-term quantum architecture for HEP applications

“HEP-motivated” data encoding and learning model

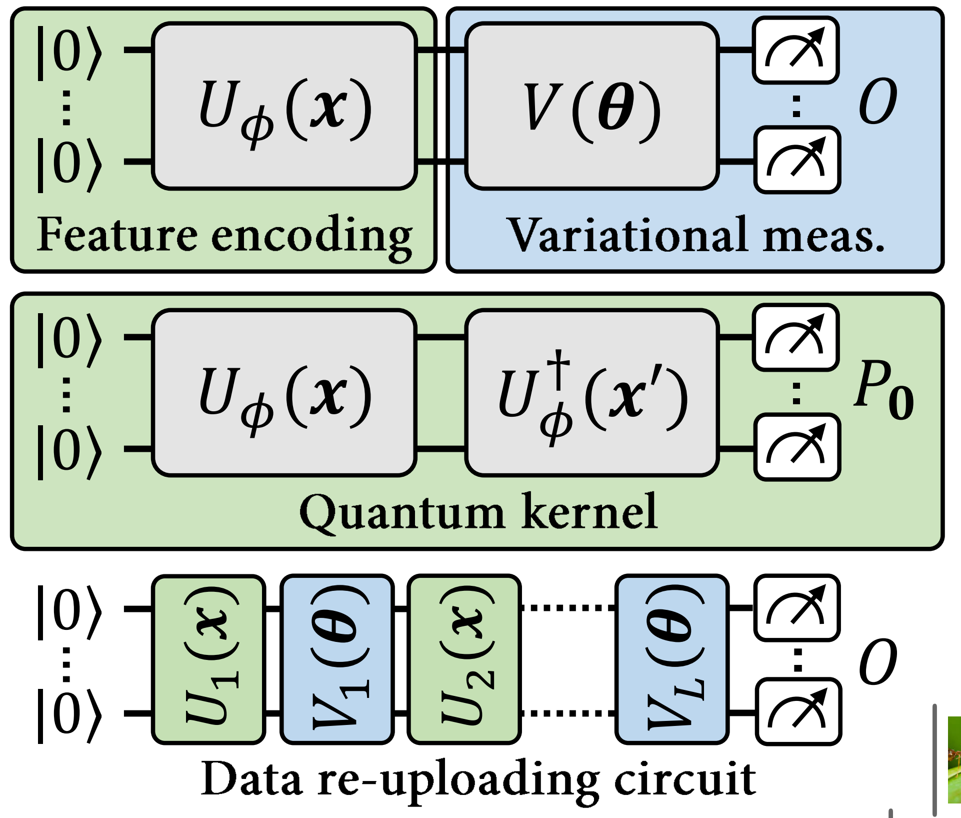
“HEP-desired” implementation for near-term device

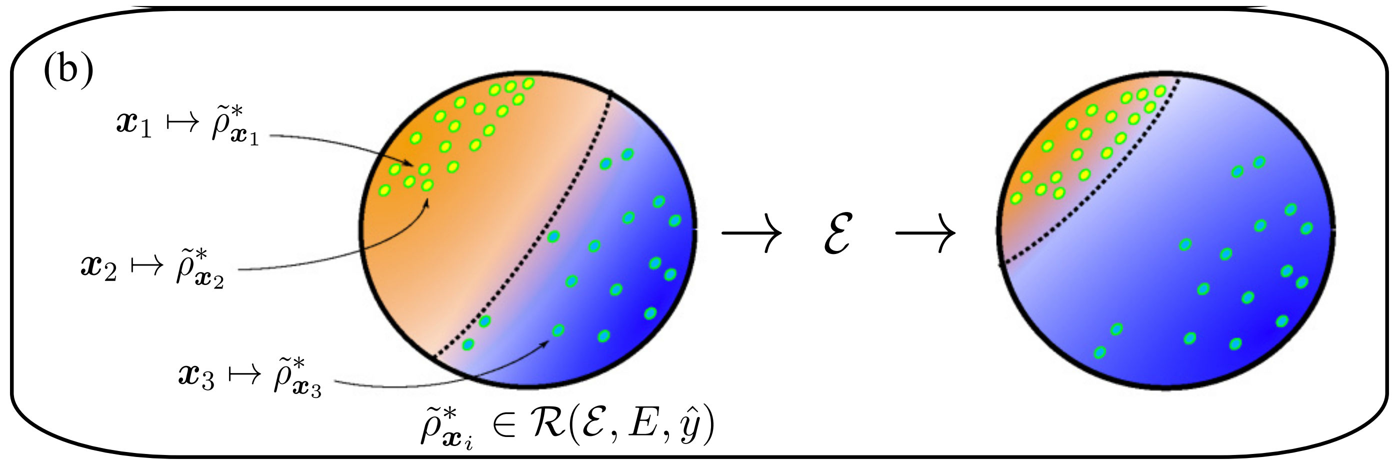
Develop **enhanced data encoding for HEP data** inputs:

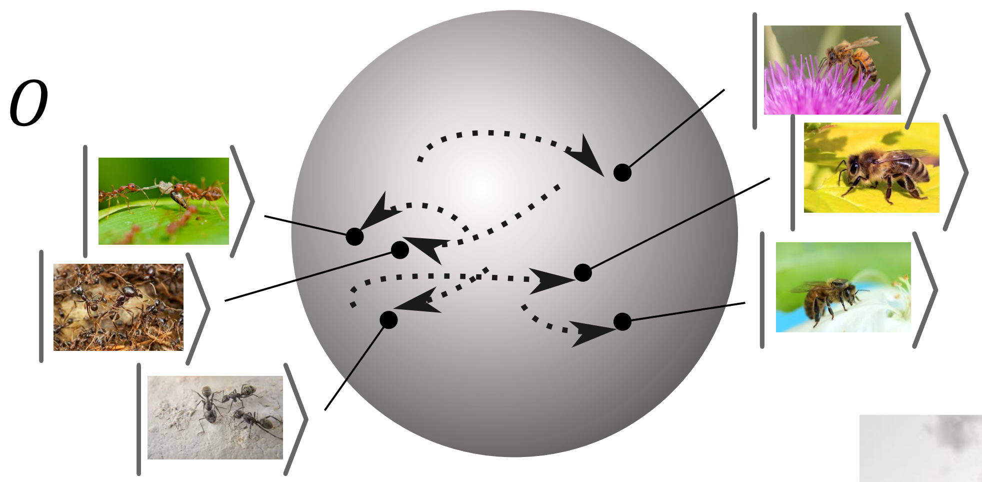
- Dense angle encoding with particle (4-vector) information
- Encoding robust against Pauli/amplitude damping noise
- Trainable embedding for better classification/noise resilience
- Data re-uploading with particle inputs

Improved **learning architecture for HEP**:

- Physics-motivated ansatz (e.g., symmetry preserving) for HEP
- Ansatz robust against Barren Plateau (e.g, quantum tangent kernel)
- Gradient descent calculation with noise resilience





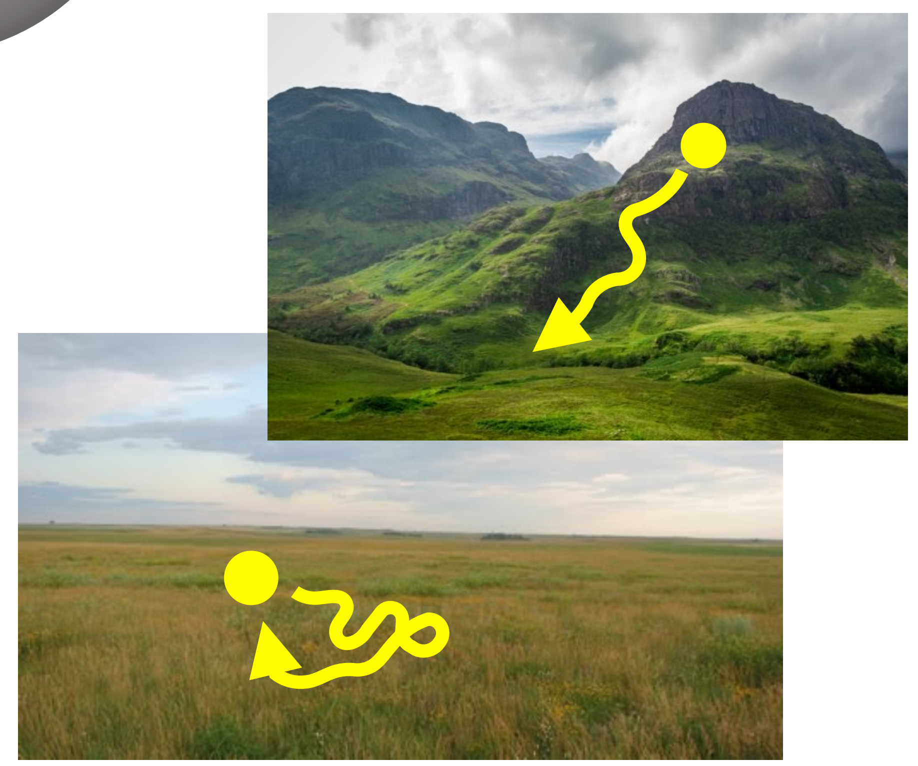


Definition 1 (Barren plateau)

Consider the VQA cost funcion $C(\boldsymbol{\theta}) = \langle\psi| U(\boldsymbol{\theta})^\dagger OU(\boldsymbol{\theta}) |\psi\rangle$, where $|\psi\rangle \in \mathbb{C}^{2^n}$ is a n-qubit quantum state, $U(\boldsymbol{\theta})$ is unitary and O is hermitian. This cost exhibits a barren plateau if

$$E_{\boldsymbol{\theta}\sim\text{uniform dist.}}\left[\frac{\partial C(\boldsymbol{\theta})}{\partial \theta_i}\right] = 0,\ V_{\boldsymbol{\theta}\sim\text{uniform dist.}}\left[\frac{\partial C(\boldsymbol{\theta})}{\partial \theta_i}\right] = O\left(b^{-n}\right)$$

holds for some $\theta_i \in \boldsymbol{\theta}$ and $b > 1$.



Proposal

Specific hardware architecture for scientific applications in long-term?

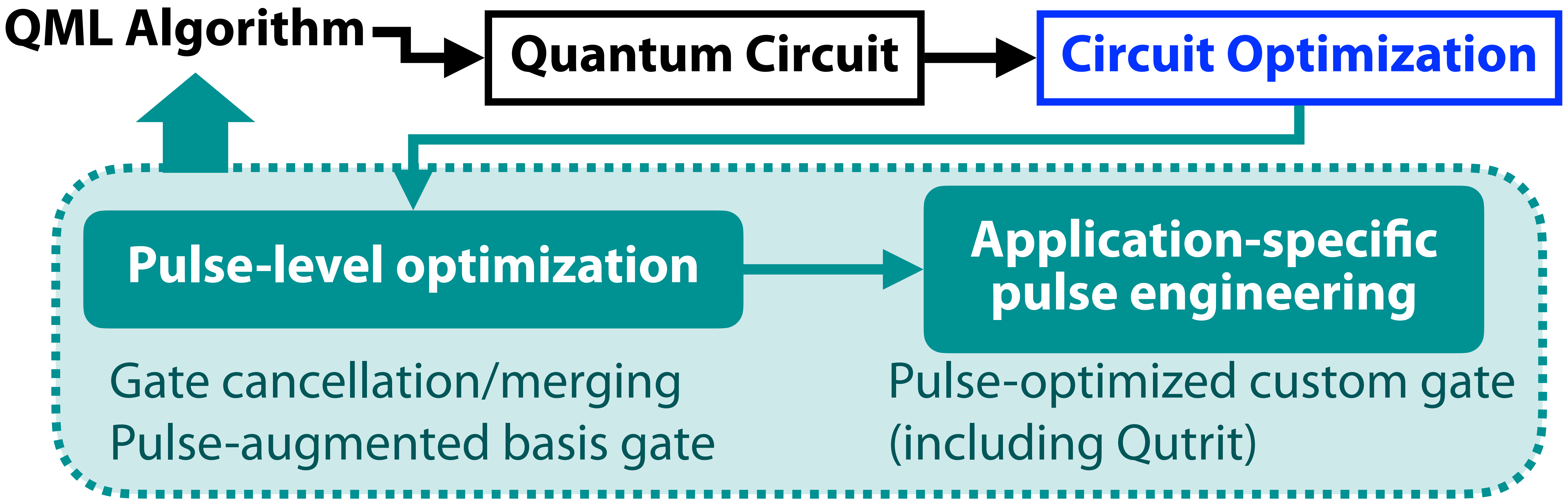
Co-design near-term quantum architecture for HEP applications

“HEP-motivated” data encoding and learning model

“HEP-desired” implementation for near-term device

Efficient hardware implementation for HEP algorithm:

- Gate synthesis/optimization for developed data encoding or ansatz
- Noise mitigation and error detection/correction
- Custom pulse control for parametrized gates
- Optimization of data & parameter loading sequence



Example circuit