RD50-MPW3 as example for “Depleted Monolithic Active Pixels Sensors”

Patrick Sieberer
## DMAPS Projects - Overview

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<th>Project</th>
<th>ALPIDE</th>
<th>MALTA</th>
<th>Monopix</th>
<th>RD50-MPW</th>
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<tr>
<td><strong>Target Experiment</strong></td>
<td>ALICE</td>
<td>ATLAS/RnD</td>
<td>RnD, Belle2</td>
<td>RnD</td>
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<tr>
<td><strong>Comment</strong></td>
<td>Very first DMAPS integrated into full detector system. Baseline for MALTA and Monopix</td>
<td>CERN-EP’s main development</td>
<td>Use case: OBELIX chip as future option for Belle2 tracker upgrade. <strong>Hephy heavily involved in design!</strong></td>
<td>This talk.</td>
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<tr>
<td><strong>Foundry</strong></td>
<td>TowerJazz</td>
<td>TowerJazz/LFoundry</td>
<td>TowerJazz/LFoundry</td>
<td>LFoundry</td>
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<tr>
<td><strong>Picture</strong></td>
<td><img src="#" alt="ALPIDE" /></td>
<td><img src="#" alt="MALTA" /></td>
<td><img src="#" alt="Monopix" /></td>
<td><img src="#" alt="RD50-MPW" /></td>
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<td><strong>Link</strong></td>
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*Non-comprehensive list!*
• CERN-RD50 collaboration
  – Radiation hard semiconductor devices for very high luminosity colliders
  – >400 people
  – 63 institutes
• CERN-RD50 CMOS Working Group
  – Program to study and develop monolithic CMOS sensors with
    • High granularity & high radiation tolerance
    • LFoundry 150nm HV-CMOS
  – Our program includes
    • TCAD simulations
    • ASIC design
    • DAQ development
    • Performance evaluation
  – Hephy Manpower
    • Thomas Bergauer
    • Christian Irmler
    • Helmut Steininger
    • Patrick Sieberer (PhD)
    • Bernhard Pilsl (Master student)
    • Klemens Flöckner (previous master student)
CMOS transistors for electronics inside a shielded well
Bulk of the wafer used as sensor
• 3 Depleted Monolithic Active Pixels Sensors (DMAPS) designed so far
  – submission dates in timeline, chip delivery ~5 months later
• All of them in LFoundry 150nm process
• High resistivity substrates (up to ~2kOhm*cm)
• Hephy started in RD50 in 2017
Digital performance in a telescope

- Digital logic in FPGA
- Synchronization with other detectors possible
- Data rate rather low (only one pixel can be activated)
- Tracking possible, but limited capabilities (single pixel)
- Lot of lessons learned for RD50-MPW3

Irradiated chips tested with Sr90
- Efficiency decreasing for higher fluence (radiation damage)

Testbeam MedAustron

- Simulation a) and testbeam measurements at 800MeV b) and 175MeV c) for a ‘switched reset pixel’
- Pulse width of signal independent of beam energy
- Testbeam results agree with simulation
- Analog pixel design taken from RD50-MPW2
  - Matrix design by Liverpool
- Complete new design of digital periphery
  - Covering ~15% of total area
  - Hephy did ~80% of the work
    - See next slide
  - Chip submitted in December 2021
  - Expected delivery ~April/May 2022
• State of the art commercial design tools
  – Cadence, Synopsis, Mentor/SiemensEDA
  – Affordable licenses from Europractise (EU funded project)

• Process Design Kit (PDK)
  – Provided by foundry
  – General process aspects (number of metal layers, design rules (spacing + thickness of metal wires), available implants, …)
  – IP-blocks: Pre-designed logic cells (Flipflops, logic gates, …), memory cells, … including timing libraries for timing verification
  – NDA (Non disclosure agreement) 😞 is mandatory to receive PDK
Functional Model
- Non synthesizable Verilog code
- Short code to develop main functionalities

RTL
- Synthesizable Verilog code

Synthesis
- Verilog matched to generic digital block
- Generic blocks mapped to physical blocks from PDK
- Logic optimization

Floorplan
- Write floorplan
- Write powerplan

Powerplan

Placement
- Placement of logic cells

Clock Tree
- Write timing constraints
- Clock tree synthesis (Placement + Routing of clock buffers)

Routing
- Detailed routing of logic cells
- Write out GDSII

Verification
- LVS/LEC (Logic vs Schematic, Logic equivalence check):
  Compare original netlist with final, layouted chip
- DRC (Design Rule check): Verify certain physical rules from foundry
  (metal density per plain, minimum distance, ….)
**RTL to GDSII Design Flow**

**Functional Model**
- Non synthesizable Verilog code
- Short code to develop main functionalities

**RTL**
- Synthesizable Verilog code

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- Incoming data stream (to FPGA)
- High speed data path
- Low speed data path (Monitoring)

**Caribou** used as DAQ
- AIDA2020 TLU connected to CaR-board for triggering
- 2-level chipboard to readout 2 chips with one setup
- 2 data paths (next slide)
Summary

- RD50-MPW2 very successful chip
  - Analog performance increased a lot compared to RD50-MPW1
- RD50-MPW3 submitted for fabrication in December 2021
  - Analog pixels electronics from RD50-MPW2
  - New digital periphery
- DAQ Design (Hardware, Firmware and Software) of RD50-MPW3 ongoing
  - No show stoppers seen so far
  - Ultimate goal is to build a small telescope demonstrator

Outlook/ToDo

- Triggering/Synchronization with other detectors
  - Preparation for testbeams at CERN + MedAustron
- Firmware development (ongoing)
- Software verification framework
  - Generates dummy data, which is fed into digital logic of the chip, processed using the RTL code, analyzed in software framework
- Simulations of whole detector system
  - TCAD used for E-Field
  - Allpix2 used for Monte Carlo studies
RD50-MPW2
- TCT and eTCT on passive test structures and active matrix
- Timing performance dependence on decreasing laser power as expected:
  - ToT decreases
  - ToA increases
- Rough calibration ToT $\rightarrow$ electrons available
- For details, see B. Hiti at 38th RD50 workshop (presented by S. Powell)

- Irradiation campaign up to $2\times10^{15}\text{N}_{\text{eq}}/\text{cm}^2$
- Sr90 tests: Decrease in pixel efficiency seen
- “L” shape at edges observed
  - Might come from biasing scheme
  - Not fully understood

Measurements with Sr90 source (only done for lower irradiated chips)
• Testbeams at medical facilities
  – Ruder Boskovic Institute (HR)
    • See talk from R. Palomo at 39th RD50 workshop
  – Rutherford Cancer Center (UK)
    • See talk from S. Powell at 38th RD50 workshop
  – MedAustron (AT)
• Analog performance
  – Pulse width at various beam energies
• Digital performance in a telescope
  – Digital logic in FPGA
  – Synchronization with other detectors possible
  – Data rate rather low (only one pixel can be activated; analog only chip!)
  – Tracking possible, but limited capabilities (single pixel)
  – *Lot of lessons learned for RD50-MPW3*

• Simulation a) and testbeam measurements at 800MeV b) and 175MeV c) for a ‘switched reset pixel’
• Pulse width of signal independent of beam energy
• Testbeam results agree with simulation
• RD50-MPW1 suffered from high leakage current and low breakdown voltages
• TCAD studies done => RD50-MPW2 as analog-only chip
  – Performs really well ($I_{\text{leak}}$, $V_{BD}$)
  – Detailed tests including timing studies with lasers and testbeams (analog + digital performance)

See talk by M. Franks at 36th RD50 workshop
• LFoundry 150nm process
• Different Wafer resistivities and fluences available
• Passive test-structures 1)
• Active matrix of DMAPS pixel, including analogue readout 2)
• SEU tolerant memory array 3)
• Bandgap reference voltage 4)
• Test structures with SPADs 5)
• Details on 3) and 4): See talk from R. Marco Hernandez at 36th RD50 workshop
• Details on 1): See talk from M. Franks at 36th RD50 workshop or from R. Marco Hernandez at VERTEX 2020
Switched Reset Pixel

Continuous Reset Pixel
DESIGN OF RD50-MPW3
• Analog pixel design taken from RD50-MPW2
  – 64 x 64 pixels
  – Pixel size 62µm x 62µm
  – Active area: 3.968mm x 3.986mm
    • Total Size: 5.1mm x 6.6mm
• Digitization in each pixel
  – FEI3-style
  – Increase of pixel size necessary
    60µm x 60µm (RD50-MPW2) to
    62µm x 62µm (RD50-MPW3)
• Complete new design of digital periphery
  – Covering ~15% of total area
  – Focus of this talk

First draft of documentation available
• Pixels read out in double columns (DCOLs) with shared digital busses to reduce routing congestions

• Each pixels receives a global (chip-internal) timestamp and returns
  – 8bit leading edge
  – 8bit trailing edge
  – 8bit pixel address

• 8 flip-flops plus logic for configuration implemented in each pixel
  – All pixel from DCOL connected to a shift-register
  – Read-back is possible
  – Not shown in figure below

• Overview of the functionalities of the matrix can be seen in Development of High Voltage-CMOS sensors within the CERN-RD50 collaboration (E. Vilella, VERTEX2021, submitted to NIM-A)

In-pixel readout logic (FEI3 - style)
DIGITAL READOUT IMPLEMENTATION
• One End-Of-Column (EOC) per DCOL
  – Configuration of pixels
  – Pixel data readout + 32 words deep buffer
• Transmission Unit (TX Unit) for data transmission
  – 128 words deep buffer (FIFO)
  – Framing
  – Encoding (Aurora 8bit-10bit)
  – Serialization (Serial stream at 640MHz)
• Control Unit (CU) for reading out EOC buffers
  – Controls data propagation from EOCs to TX Unit
• Global Timestamp (TS) Generator
  – 8bit, running at 40MHz
  – Gray-encoded to minimize activity on bus
• Clock and Reset Generator
  – Dividing a fast (640MHz) clock into a 40MHz clock
  – Clock multiplexer for optional external 40MHz
  – Synchronizing the 2 external reset signals with clock
• I2C to wishbone module
  – Converts external I2C signals to internal wishbone control signals
Usually implemented in separate clock domain (16MHz)

**Clock Domain Crossing (CDC)**

- Usually, internal clocks are generated using a PLL
  - Not available, complex to design
- Internal 40MHz used
  - Generated by a divider from external 640MHz
- Special enable signal (EN, shown below) generated with 640MHz clock
  - 2 different cases, but always exactly 1 rising edge of 40MHz clock within high level of enable
  - Special attention to constraints and clock tree needed

**Internal Buffers**

- 2 stage FIFO chain
  - 32 words deep in each DCOL
  - 128 words deep in TX Unit
  - Less high speed buffers in FPGA required

**Monitoring**

- 10 monitoring outputs for internal signals

**External Control**

- Parts of internal logic can be controlled with external signals for debugging

Timing of enable signal (EN)
Matrix Readout and Control – End Of Column (EOC)

1 DCOL of Matrix

LE, TE, Pixel - Address (8 bit each)

SER IN

SER OUT

MUX 128 to 1

8 bits per register

Conf_reg_Pix0
Conf_reg_Pix1
Conf_reg_Pix2
Conf_reg_Pix3
Conf_reg_Pix4
Conf_reg_Pix5
Conf_reg_Pix6
Conf_reg_Pix7
Conf_reg_Pix8
...
Conf_reg_Pix15
Conf_reg_EOC

FIFO (24 bit * 32)

Token Handler

DATA OUT REG (32 bit)

EOC address

next token

previous token

Output Pad

TS

Wishbone-Bus

Wishbone - Bus

Patrick Sieberer
4.03.2022
Novelties of RD50-MPW3

Pattern registers

MUX

DATA
32bit from TX-FIFO

SOF/EOF/DEBUG
32bit each

IDLE
32bit

1 bit
k_char

SEL register

Comb. encoding

encoder output register

8bit-10bit Encoder

Serializer
(640MHz)

shift register

DATA-OUT (1bit)

Finite State Machine (FSM)

IDLE
32bit

DATA
32bit from TX-FIFO

Patricia Sieberer

4.03.2022
CONCEPTS RD50-MPW3 DAQ
# Data Flow and Software

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<th>Fast data path</th>
<th>Slow data path</th>
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<tr>
<td><strong>Purpose</strong></td>
<td>Data taking</td>
<td>Monitoring, Spy Data (small percentage of data)</td>
</tr>
<tr>
<td><strong>Data flow</strong></td>
<td>SFP port + UDP (Jumbo frames) for fast, firmware-controlled readout</td>
<td>AXI Bus + Ethernet network for monitoring and slow control</td>
</tr>
<tr>
<td><strong>Data storage</strong></td>
<td>Integrated into EUDAQ (EUDAQ raw data files)</td>
<td>EUDAQ + custom data storage possible, Handling of slow control commands</td>
</tr>
<tr>
<td><strong>Usage</strong></td>
<td>• data transmission + storage only</td>
<td>• Slow control commands</td>
</tr>
<tr>
<td></td>
<td>• easy integration to tracking framework <strong>Corryvreckan</strong></td>
<td>• Monitoring</td>
</tr>
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<td></td>
<td>• Testbeam</td>
<td>• Standalone tests at laboratory</td>
</tr>
<tr>
<td><strong>Current development efforts (examples)</strong></td>
<td>Loopback speed-test at 640MHz implemented</td>
<td>Draft of online monitor:</td>
</tr>
<tr>
<td></td>
<td>• Dummy data generated in FPGA</td>
<td><img src="image" alt="Draft of online monitor" /></td>
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<tr>
<td></td>
<td>• Data sent to CaRboard, loop-back over FMC connector</td>
<td></td>
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<tr>
<td></td>
<td>• Data read by FPGA + sent over UDP to PC (850Mbit/s data rate achieved)</td>
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TRIGGERING RD50-MPW3
AIDA-TLU with 2 possible DUT interfaces:

- **EUDET Mode**: Needed for Hephy-telescope and many other older telescope
  - Whenever no (fast or “synchronizable”) internal TS is available in the telescope

- **AIDA Mode**: Needed for RD50-MPW3 and newer telescope (probably at CERN)
  - Whenever internal TS-synchronizing is possible
  - Much faster than EUDET
• TLU has two internal, fast FIFOs
  – Trigger Number (TN), 15 bit
  – Fast timestamp (TS-T = TimeStamp-TLU), up to 160MHz, ~16 bit (coarse and fine(?)

• For the EUDET mode, the TN written on the DUT interface after every trigger
  – Trigger input from scintillators needed

• For AIDA mode, TS-C and TS-T are synchronized at the beginning of each run with a special signal on the DUT interface
  – TLU and RD50-MPW3 now have the same TS!

• **EUDAQ Producer available, which reads the two FIFOs of the TLU to match TN with a TS-T (and thus also TS-C)**
  – Event matching must be done offline
  – Data readout over the IPBus, up to **50MHz trigger rate** possible (otherwise, FIFO-overflow)
    • This determines our max. particle rate we can handle (!)