WAFFER-TO-WAFFER BONDING FOR ULTRA-THIN HYBRID PIXEL DETECTORS

F. HÜGGING, UNIVERSITY OF BONN
I.-M. GREGOR, DESY & BONN
T. FRITZSCH, FRAUNHOFER IZM BERLIN
Want to reduce mass, i.e. thickness of pixel detectors as much as possible while keeping the benefits of the hybrid approach:

- Separate development and optimization of sensors and FE electronics allowing for best performance of FE electronic and sensor.
- Fine pitch interconnection between FE and sensor pixel with a pitch down to ~20µm.
- Thinning of FE and sensor parts to the minimum.
- Can benefit from active CMOS sensor development by integrating some electronic already into the sensor

Target is the development of ultra-thin hybrid pixel detectors based on:

- 50 – 100 µm thick pixel sensor on 200 (300) mm CMOS wafers
- ~20 µm thick pixel FE chip thickness on 200 (300) mm CMOS
ULTRA THIN HYBRIDS: ENABLING TECHNOLOGIES

- **Wafer-to-Wafer bonding between R/O and sensor wafer:**
  - Main objective of this project to choose and develop the process for fine pitch W2W bonding with sensor and FE electronic wafers of 200 and 300 mm size.

- **Thinning and backside processing** of bonded wafer-wafer assembly:
  - Thinning on wafer level is easy, but might need backside process of the sensor backside, i.e. backside implantation and metallization
  - Opening and connection to the R/O chip pads (I/O and power) from the backside after thinning:
    - similar to the TSV pixel module project already demonstrated during AIDA-2020.

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![Diagram of wafer bonding process](image-url)
ULTRA THIN HYBRID PIXEL DETECTORS: SETUP

- Bonding layer with metal-metal and/or capacitively coupled contacts
- Thinned R/O wafer with backside via last interconnection (TSVs)
- R/O backside redistribution layer (RDL) with contact pads
- Thin sensor (passive or DMAPS like) with contact pads and backside processing
PROOF OF CONCEPT PROJECT FOR AIDAINNOVA

- Develop dedicated CMOS Sensor wafer compatible with a pixel FE chip wafer:
  - Starting point: passive CMOS sensor development on 200 mm wafer with 110/150 nm process node from LFoundry
  - Decided to use TimePix3 chip wafers (GF 130 nm on 200 mm wafers)
  - Keep own FE development on the same wafer as the sensor as backup option: explore if both are possible on same by a “shared reticle” large enough to cover 2 times the TimePix chip
  - Developing and optimization of hybridization process including thinning and interconnection from chip’s backside has started at IZM.
  - Longer Term: Transfer process to more modern feature size pixel chips (65nm or 28 nm on 300 mm wafers) for smaller pixel pitches and faster electronics
CMOS SENSOR WAFER DESIGN

- Starting Point: Full-Size Passive CMOS Sensor SUBMISSION from 2019/20 and CMS Submission in 2022:
  - Up to full-size 4 x 4 cm² pixel sensor tiles by stitching
  - Different pixel flavors (50 x 50 µm², 25 x 100 µm²; AC or DC coupled, biasing with > 4 kOhm poly-resistor)
  - Float-zone or high ohmic Cz wafer material possible
  - LF0undry 150 nm 1.8V CMOS process with reduced mask sets
  - Thinning to 150 µm with handling wafer, backside implantation @ CMOS fab; Backside Al-Si metal, UBM, Flip-chip @ ATLAS ITk hybridization vendor
  - Very good performance before and after irradiation with hybrid pixel detectors.
- Pixel sensor design can be re-used and is well advanced
  - Use large reticle design (MLM2 or 4) with reduced mask sets
  - Currently in discussion with LF0ndry about technical and contractual details
  - Looking for funding (not within in AIDAinnova)
  - Once this is settled design can be finished with 1-2 month
SENSOR PERFORMANCE: SMALL PROTOTYPES

100µm thickness (~90µm active sensor) + RD53A

Charge spectrum (MIP)

Hit detection Efficiency (MIP)

Radiation (NIEL)

Requirement after irradiation 97% (in-time) efficiency

0 × 10^{15} n_{eq}/cm²

5 × 10^{15} n_{eq}/cm²

1 × 10^{16} n_{eq}/cm²
150µm thick full size (~140µm active sensor) + RD53A

Charge for MIP

Artificial higher MPV due to threshold cutting into spectrum

Radiation (NIEL)

Hit detection Efficiency (MIP)
Assembly by Wafer to Wafer Bonding – W2W

**Fully/Semi-Automated Wafer Bonder:**
- Wafer size 200 mm, 300 mm
- maximum force: 60 kN
- maximum temperature: 550 °C
- vacuum: $1 \times 10^{-5} \text{ mbar}$
- Wafer to wafer alignment accuracy <1µm

**Applicable Bonding processes:**
- Adhesive bonding
- Silicon direct bonding
- Anodic bonding
- Solder/eutectic bonding
- Thermo-compression bonding
- Metal-oxide hybrid bonding

**Requirements:**
- Wafer size matching: top and bottom wafer of the same size
- Design matching: reticle/chip step and repeat; design/wafer origin
- Particle free and planarized wafer surfaces
- (Special processes with pre-assembled wafer possible (parallel KGD assembly))
- Consistent with subsequent post-processes and dicing process
Introduction – Wafer Bonding

**Wafer to Wafer Bonding**

**Bonding without Intermediate Layer**
- Silicon Direct Bonding
- Anodic Bonding

**Bonding with Intermediate Layer**
- Glasfritt Bonding
- Solder / Eutectic Bonding
- Thermo-compression Bonding
- Hybrid Bonding
- Adhesive Bonding

**Permanent Bonding**
- Sensor Manufacturing
- MEMS / Sensor Packaging
  - Cap Wafer / Spacer Wafer Manufacturing
  - Wafer Level Capping

**Electrical Interconnects and Bonding layer:**
- Capacitive coupling IOs
- Electrically conductive IO interconnects
- TSV interconnects from wafer backside
- Process flow: vacuum processes, temperature steps, temporary bonding
Metal – Oxide Hybrid Bonding

**Cu/SiO2**

**Motivation for DBI®**:
- W2W, D2W, D2D
- Highest interconnect density: I/O pitch down to 1 µm
- High alignment accuracy
- No bumps, no intermetallics
- No gap – no underfilling
- High reliability

**Process**:
- SiO2 passivation + Cu pads
- Surface planarization (CMP)
- Surface activation (plasma, chemicals)
- Room temperature bond
- Annealing 150 – 300°C
- 3D chip stacking: memory chips, CMOS image sensors (CIS)

**Fraunhofer IZM-ASSID: 300mm W2W Bonding with <5µm alignment accuracy**

Fraunhofer test chip with 4 µm pad /18µm pitch, Metal density: 4.5%

<table>
<thead>
<tr>
<th>Surface Preparation (Results)</th>
<th>FhG IZM ASSID</th>
</tr>
</thead>
<tbody>
<tr>
<td>Roughness beside TSV (Oxide)  Ra</td>
<td>0,146 nm</td>
</tr>
<tr>
<td>Roughness on TSV (Cu) Ra</td>
<td>0,163 nm</td>
</tr>
<tr>
<td>Planarization</td>
<td>5 nm @ 100µm</td>
</tr>
</tbody>
</table>

Surface preparation in nanometer range → Atomic force microscopy

Processes patented, licence required for Invensas ZiBond® direct bonding, DBI® and DBI Ultra hybrid bonding technologies
Ultra Thin Hybrid Pixel Detectors

Process features that are explored and will be defined:

- Definition of wafer to wafer contacts: capacitively coupled, metal-metal, TLPB
- Bonding interface material:
  - metal polymer hybrid bonding
- Requirements for pad and bonding surface topography:
  - parameters of sensor and TMPX3 wafer must be measured
- TSV formation and backside contact: M1 contact (critical TMPX3/MPX3 M1-M2 issue)
- Backside RDL and contacts design, materials: wire bonding and/or soldering
CURRENT WORK: TPX3 WAFER EVALUATION & SENSOR WAFER DESIGN AND ARRANGEMENT

- TimePix3 wafer evaluation with MediPix/TimePix collaboration (Michael Campbell et al.):
  - chip size is ~ 14 x 15mm$^2$ on 200 mm wafers
  - measure absolute distances of chips/reticles wrt. the wafer borders for several wafer to ensure all wafers are the same
  - Low yield wafers for process setup and development are available
  - Prefer un-probed wafers for the W2W bonding process: no additional probe marks which disturbs the wafer topography even more
  - LFoundry 110/150nm maximum reticle size is 25 x 32mm$^2$
  - Could use MLM2 or place 2 different chips

Max Dies Per Wafer (without defect) #108
MILESTONES & DELIVERABLES FOR TASK 6.4

- Milestone MS6.4: Availability of parts and definition of the technologies for wafer to wafer hybridization
  - Due by M18, i.e. September 2022
  - Wafers delivered to IZM and report on the technologies chosen for the interconnection
    → Good progress here, milestone seems reachable, sensor wafers may come a bit later
- Deliverable D6.4: Test of the final ultra-thin hybrid assemblies from wafer to wafer bonding
  - Due by M44, i.e. November 2024
  - The characterisation will validate the module functionality after the extreme thinning, the interconnection yield and strength.
Wafer2Wafer Bonding project has started and first steps are on the way:

- Subcontracting IZM almost finished:
  - IZM outlined detailed programme with work package definitions and UBonnn will place order according to funding reserved for this in AIDAinnova.

- IZM started to develop and optimize their process flow for 200 wafers with TimePix3 and LFoundry CMOS Sensor wafers in mind.

- Established a collaboration with MediPix/TimePix developers to evaluate necessary details of the TimePix3 wafers.

- Design of CMOS sensor wafer is currently ongoing and well advanced since we can profit from previous designs.

- Need to settle contractual situation with LFoundry and clarify funding of the sensor wafer production.