KoALICE

# Design activities towards stitched sensor

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# Outline

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  - ITS3 timeline
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  - MOSS Monolithic Stitched Sensor
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- Next generation sensor design for LS3

# Introduction

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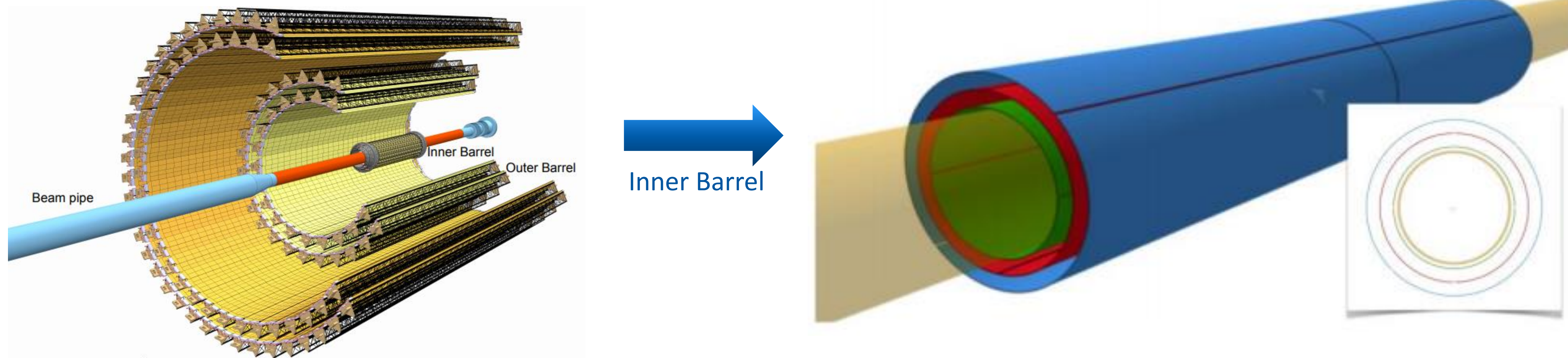


"Technical Design Report for the Upgrade of the ALICE Inner Tracking". ALICE Collaboration, B. Abelev et al. System. J. Phys. G 41, 087002 (2014).

https://indico.ph.liv.ac.uk/event/2/contributions/144/attachments/94/125/MBuckland_ALICE_HEPXmasMeeting.pdf

- ITS3 detector concept
  - The inner barrel in ITS2 is ultra-light but rather packed and irregular
  - circuit board (power&data) / mechanical support / water cooling
  
  → Integrating on chip / Rolling Si Wafer / power consumption below 20mW/cm$^2$

https://indico.cern.ch/event/932973/contributions/4073514/attachments/2141373/3608219/2020-11-12_FCC_ALICE_MAPS.pdf

# ITS3 detector concept

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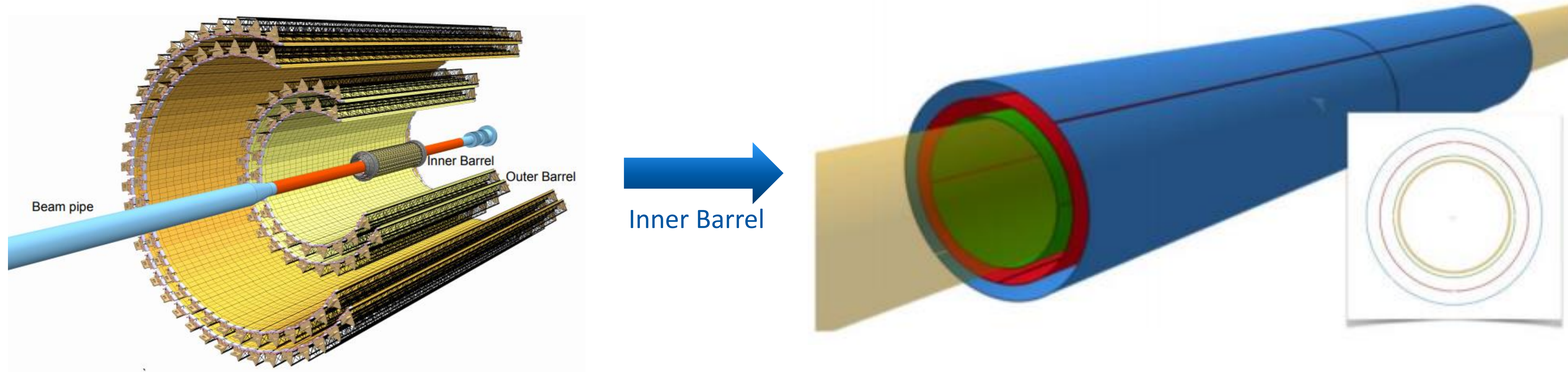
| Parameter | ALPIDE (existing) | Wafer-scale sensor (this proposal) |
|---|---|---|
| Technology node | 180 nm | 65 nm |
| Silicon thickness | 50 μm | 20-40 μm |
| Pixel size | 27 x 29 μm | O(10 x 10 μm) |
| Chip dimensions | 1.5 x 3.0 cm | scalable up to 28 x 10 cm |
| Front-end pulse duration | ~ 5 μs | ~ 200 ns |
| Time resolution | ~ 1 μs | < 100 ns (option: <10ns) |
| Max particle fluence | 100 MHz/cm$^2$ | 100 MHz/cm$^2$ |
| Max particle readout rate | 10 MHz/cm$^2$ | 100 MHz/cm$^2$ |
| Power Consumption | 40 mW/cm$^2$ | < 20 mW/cm$^2$ (pixel matrix) |
| Detection efficiency | > 99% | > 99% |
| Fake hit rate | < $10^{-7}$ event/pixel | < $10^{-7}$ event/pixel |
| NIEL radiation tolerance | ~3 x $10^{13}$ 1 MeV $n_{eq}/cm^2$ | $10^{14}$ 1 MeV $n_{eq}/cm^2$ |
| TID radiation tolerance | 3 MRad | 10 MRad |

https://indico.cern.ch/event/813597/contributions/3727803/attachments/1989307/3315951/2020-02-18_Trento2020_ITS3.pdf

- Chip size is traditionally limited by CMOS manufacturing (“reticle size”)
  - typical sizes of few cm$^2$
  - modules are tiled with chips connected to a flexible printed circuit board
- New option: stitching, i.e. aligned exposures of a reticle to produce larger circuits
  - actively used in industry
  - a 300 mm wafer can house a chip to equip a full half-layer

https://indico.cern.ch/event/813597/contributions/3727803/attachments/1989307/3315951/2020-02-18_Trento2020_ITS3.pdf

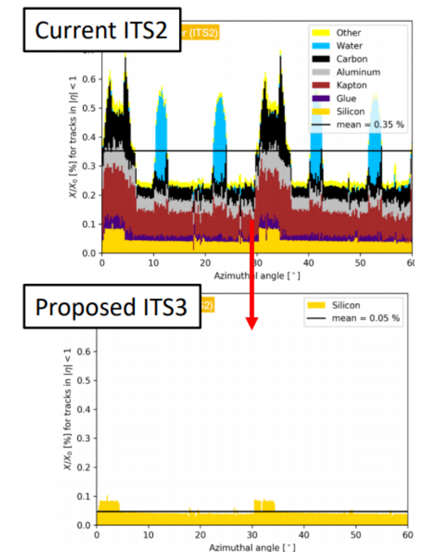
# ITS3 detector concept




“Technical Design Report for the Upgrade of the ALICE Inner Tracking”. ALICE Collaboration, B. Abelev et al. System. J. Phys. G 41, 087002 (2014).

https://indico.ph.liv.ac.uk/event/2/contributions/144/attachments/94/125/MBuckland_ALICE_HEPXmasMeeting.pdf

- Key ingredients:
  - 300 mm wafer-scale chips, fabricated using stitching
  - thinned down to 20-40 µm (0.02-0.04% X0), making them flexible
  - bent to the target radii
  - mechanically hold in place by carbon foam ribs
- Key benefits:
  - extremely low material budget: 0.02-0.04% X0 (beampipe: 500 µm Be: 0.14% X0)
  - homogeneous material distribution: essentially zero systematic error from material distribution




https://indico.cern.ch/event/974424/contributions/4158313/attachments/2185864/3693273/2021-02-08_DAQFEET-ITS3sensor.pdf

# ITS3 timeline

## main milestones

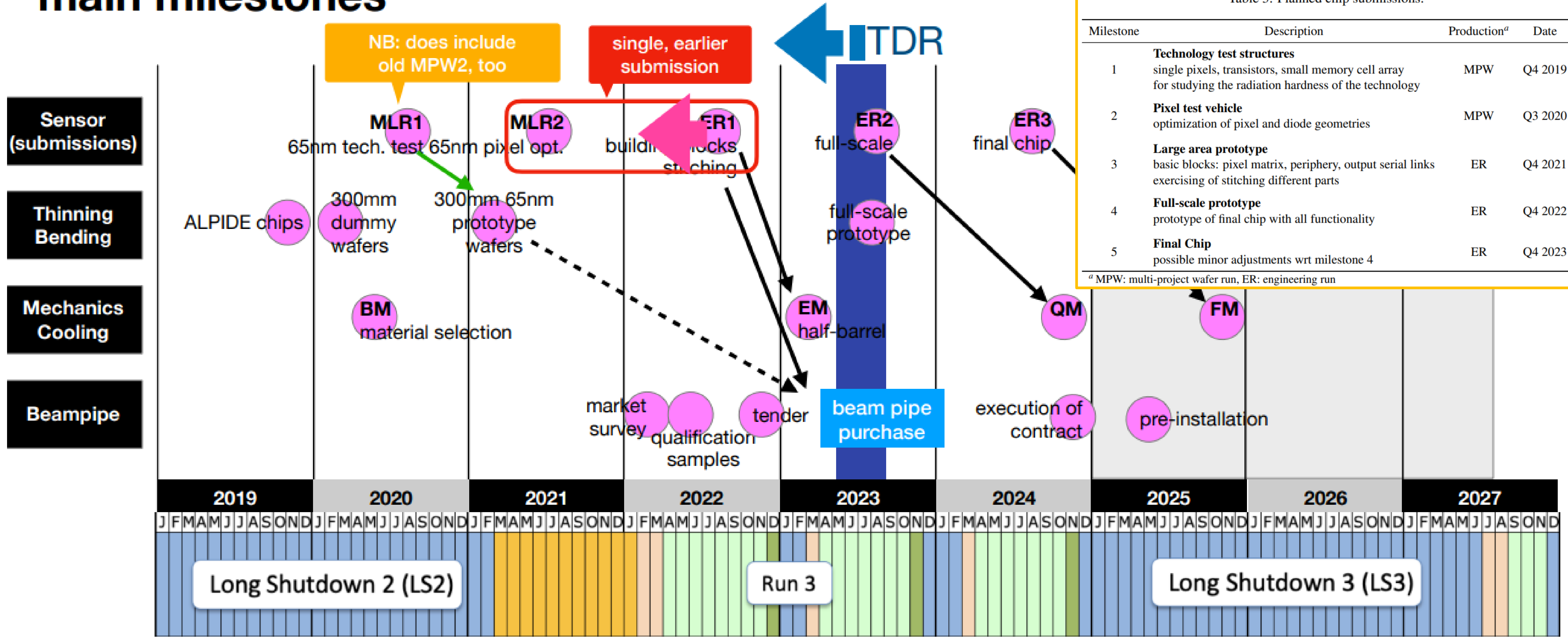



Table 3: Planned chip submissions.

| Milestone | Description | Production[a] | Date |
|---|---|---|---|
| 1 | **Technology test structures** single pixels, transistors, small memory cell array for studying the radiation hardness of the technology | MPW | Q4 2019 |
| 2 | **Pixel test vehicle** optimization of pixel and diode geometries | MPW | Q3 2020 |
| 3 | **Large area prototype** basic blocks: pixel matrix, periphery, output serial links exercising of stitching different parts | ER | Q4 2021 |
| 4 | **Full-scale prototype** prototype of final chip with all functionality | ER | Q4 2022 |
| 5 | **Final Chip** possible minor adjustments wrt milestone 4 | ER | Q4 2023 |

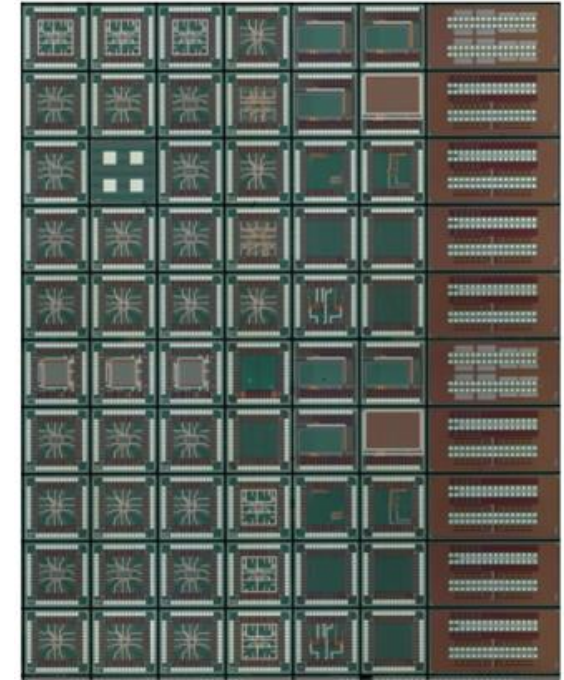
[a] MPW: multi-project wafer run, ER: engineering run

**Tight schedule, but we are on track!**

**MLR:** multiple layer per reticle, **ER:** engineering run,
**BM:** breadboard module, **EM:** engineering module, **QM:** qualification module, **FM:** final module

# MLR1 production

IPHC
Transistor test
10 µm OPAMP
SF AC
DPTS
Yonsei
25 µm SF
20 µm SF PW
20 µm AMP AC
NIKHEF
DESY
RAL
20 µm SF
PAD chip
20 µm SF
SF AC
10 µm AMP AC
Opamp AC
NIKHEF
15 µm SF
10 µm SF PW
20 µm AMP
AC
CPPM
10 µm SF
SF AC
10 µm AMP
AC



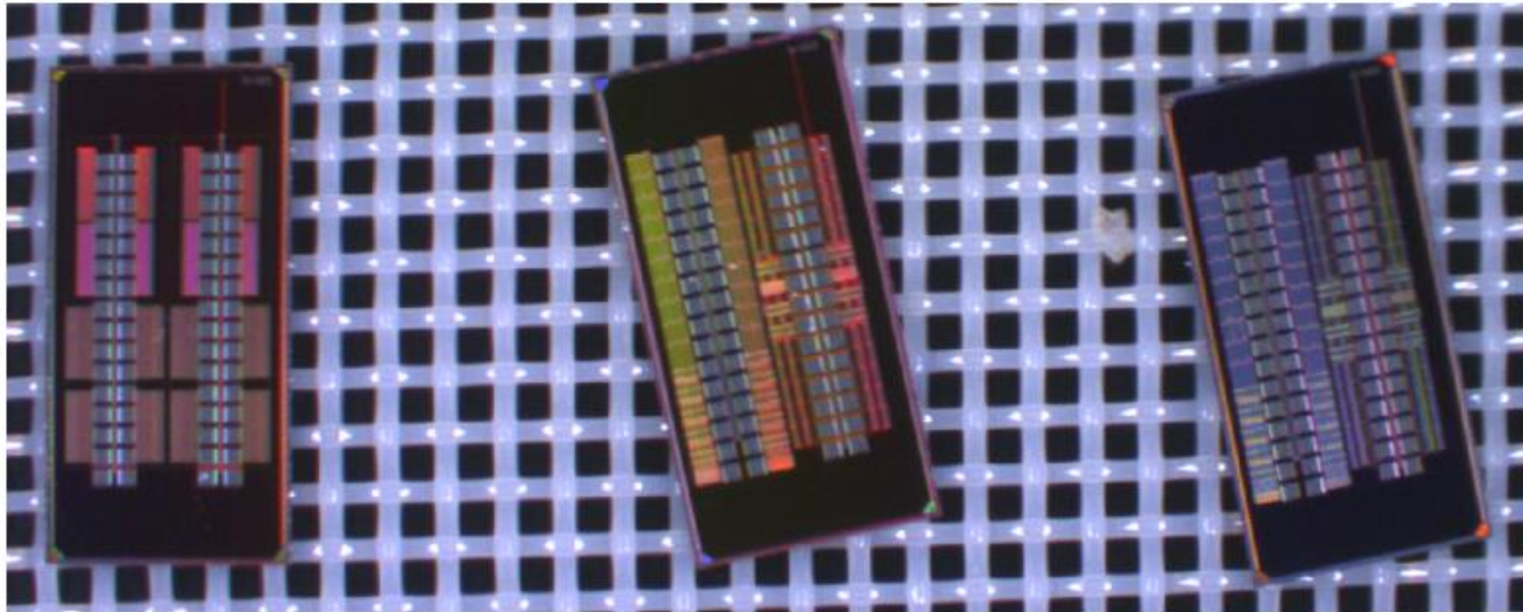
- GDS submission in Dec 2020
- Chip delivery in July 2021

# 65 nm prototypes, MLR1

## transistor test structures

CERN ALICE

- Compatible with existing test system based on probe card
- Tests have already started
  - no apparent showstoppers so far
  - detailed analysis ongoing and in discussion with foundry

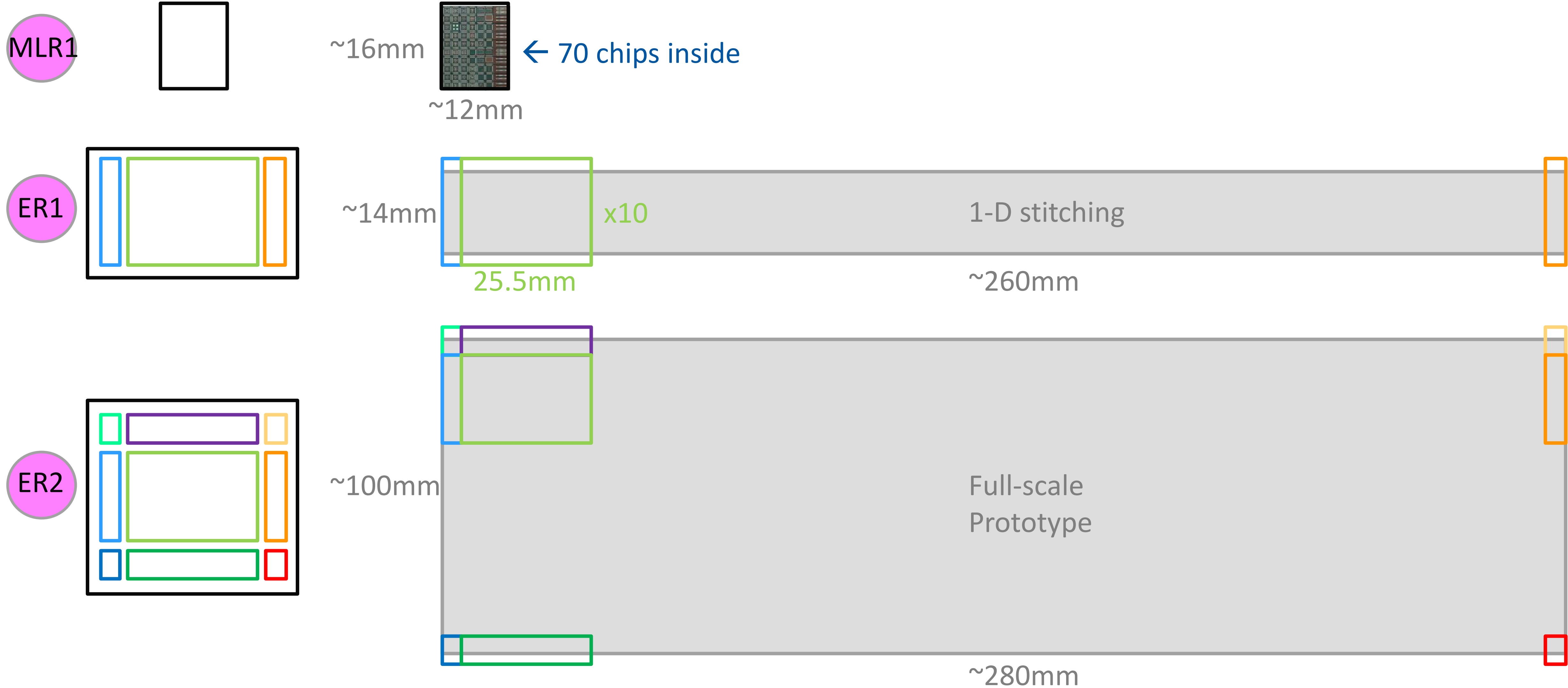


**Very encouraging results, clears first milestone of 65 nm verification**

https://indico.cern.ch/event/1071914/

Magnus Mager (CERN) | ALICE ITS3 | CERN detector seminar | 24.09.2021 | 49

# Stitched sensor development



# MOSS Monolithic Stitched Sensor Prototype

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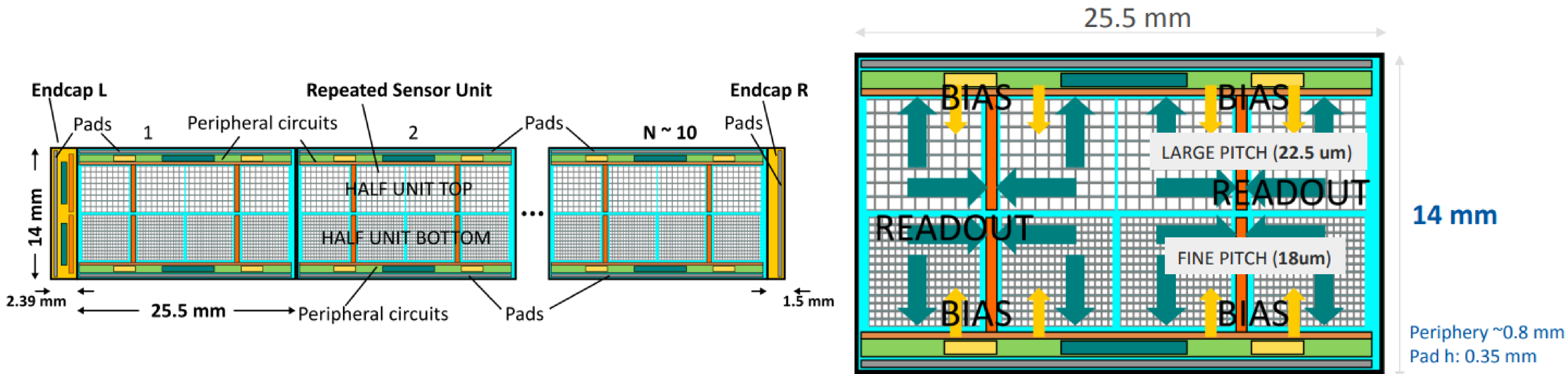
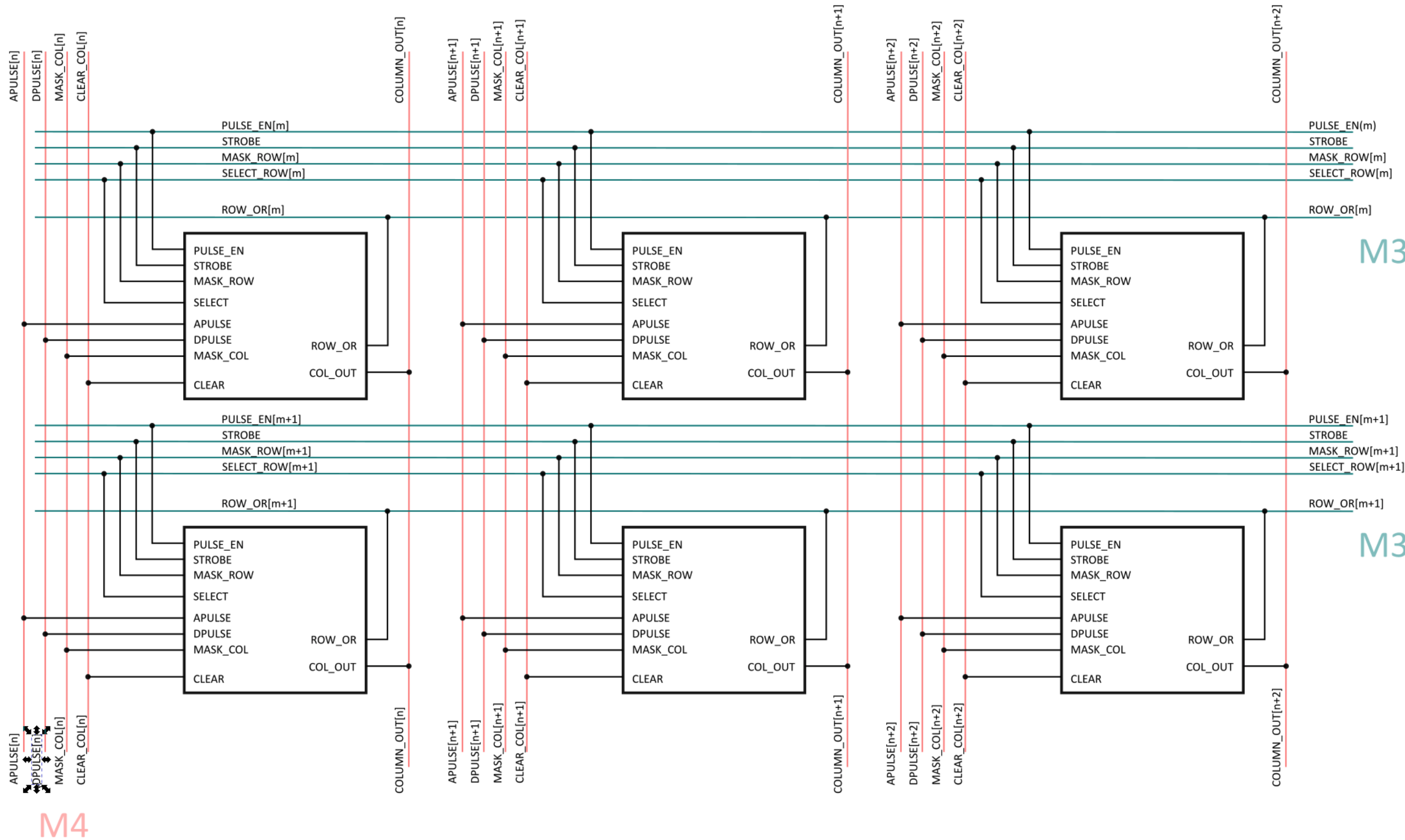



- Implement a large sensor abutting identical but functionally independent sub-units
  - Repeated Sensor Unit, Endcap Left, Endcap Right
  - Stitching used to connect metal traces for **power distribution** and **long range on-chip interconnect busses for control and data readout**

https://indico.cern.ch/event/1091910/

# Concept for Pixels Readout in a Region




Global Strobe

In-Pixel Latch

*Row* OR output line

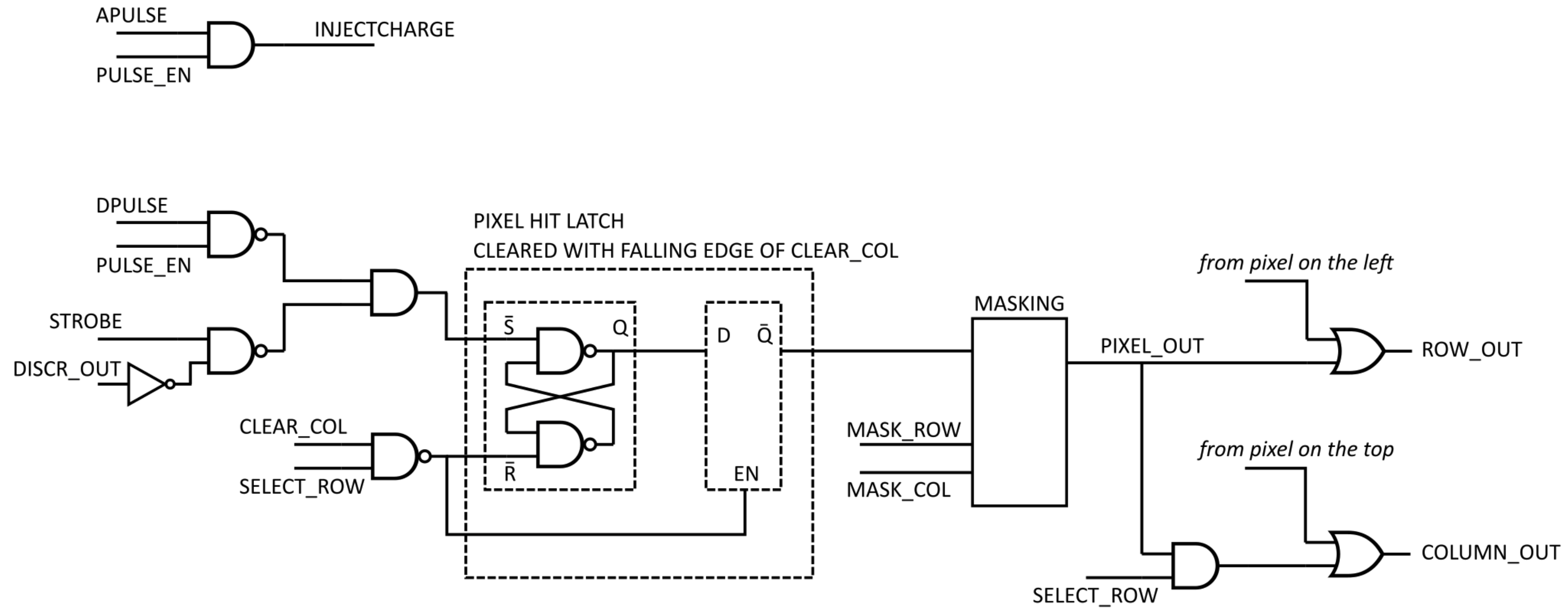
Selection of row (token)

Skip rows with no hits

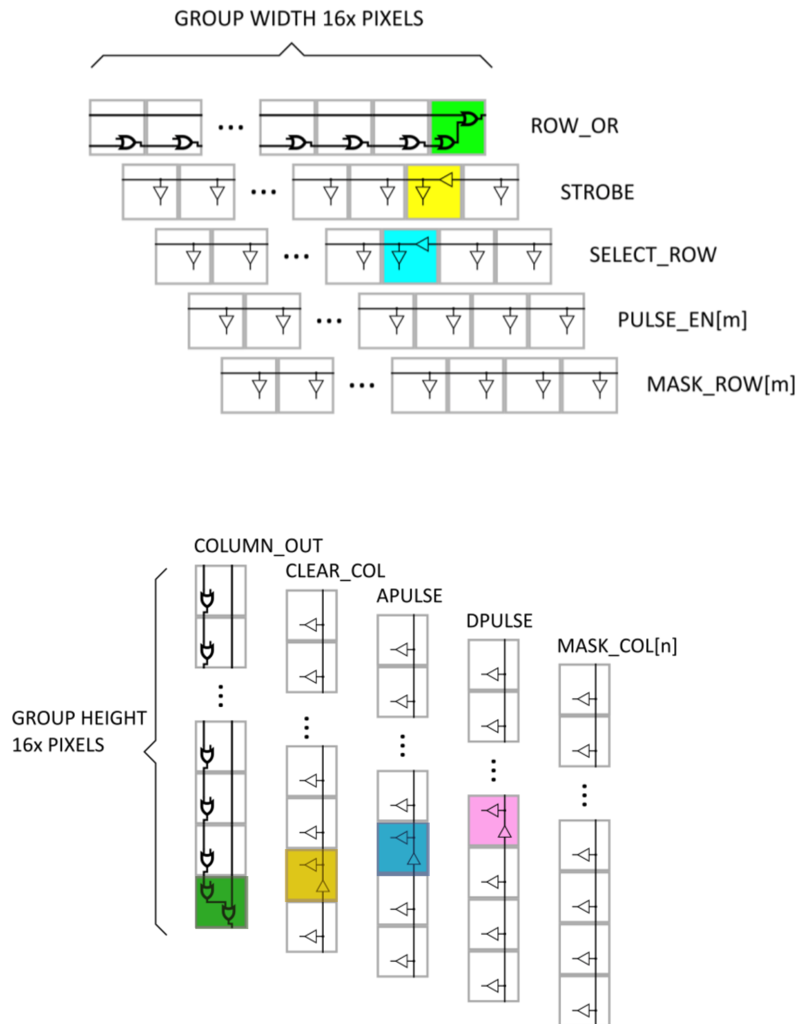
Column out line

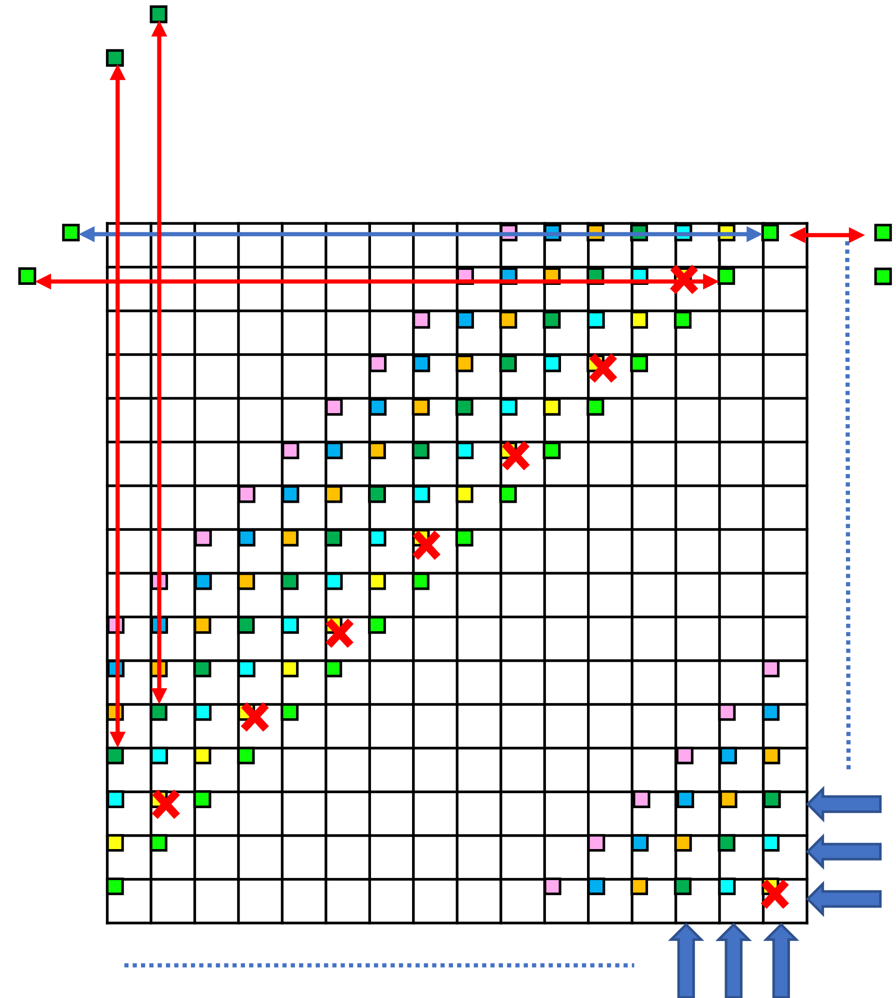
Pixels of the selected row drive the column line

# Digital pixel logic

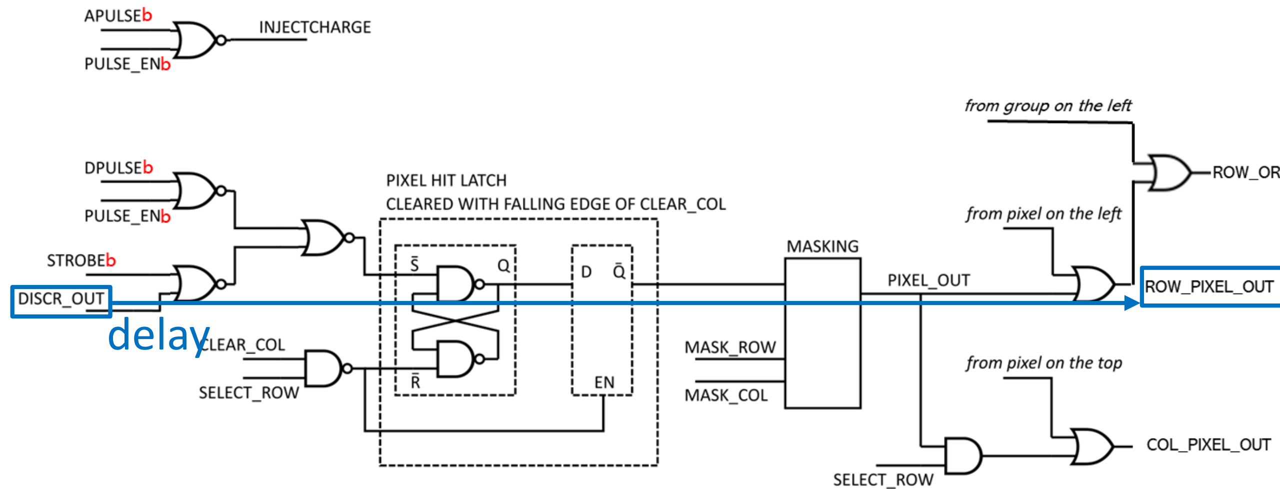


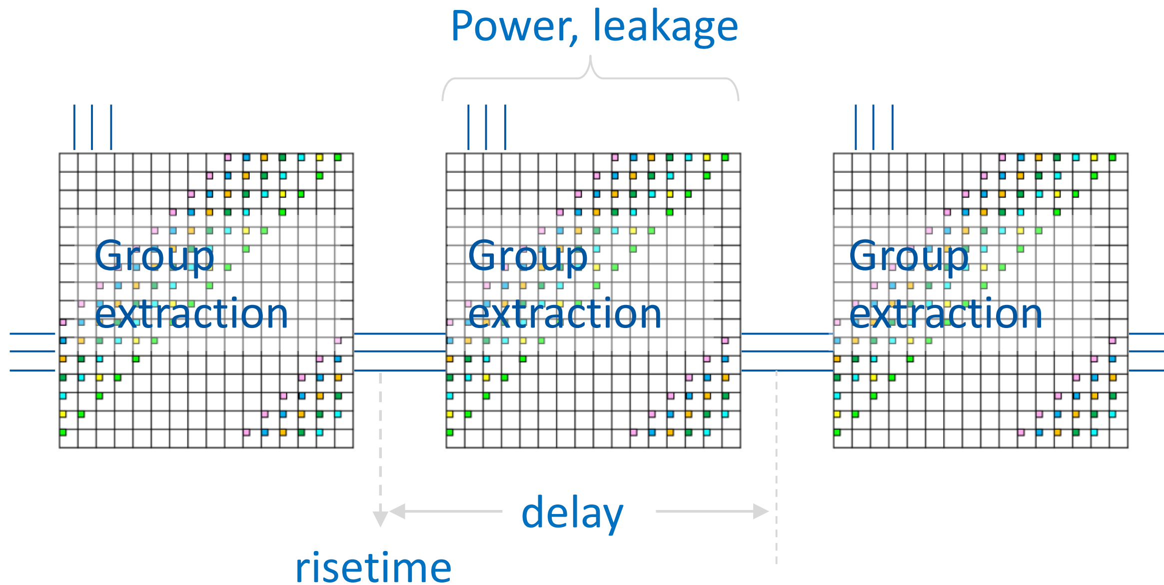
# Signal Regeneration



# Post-layout extraction simulation results




PWELL=0 V

Typical corner (1.2V, typical process, 27degrees)

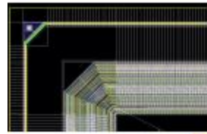
- Output delay
  (FE output over Vth 0.6V → ROW_PIXEL_OUT) : 24 ns
  (ROW_PIXEL_OUT → ROW_OR) : 1.022ns
  (ROW_OR → ROW_OR) : 0.612ns

- STROBE group-to-group delay 0.719ns
- STROBE regeneration dynamic energy 84.1 fJ
- SELECT_ROW group-to-group delay 1.21ns

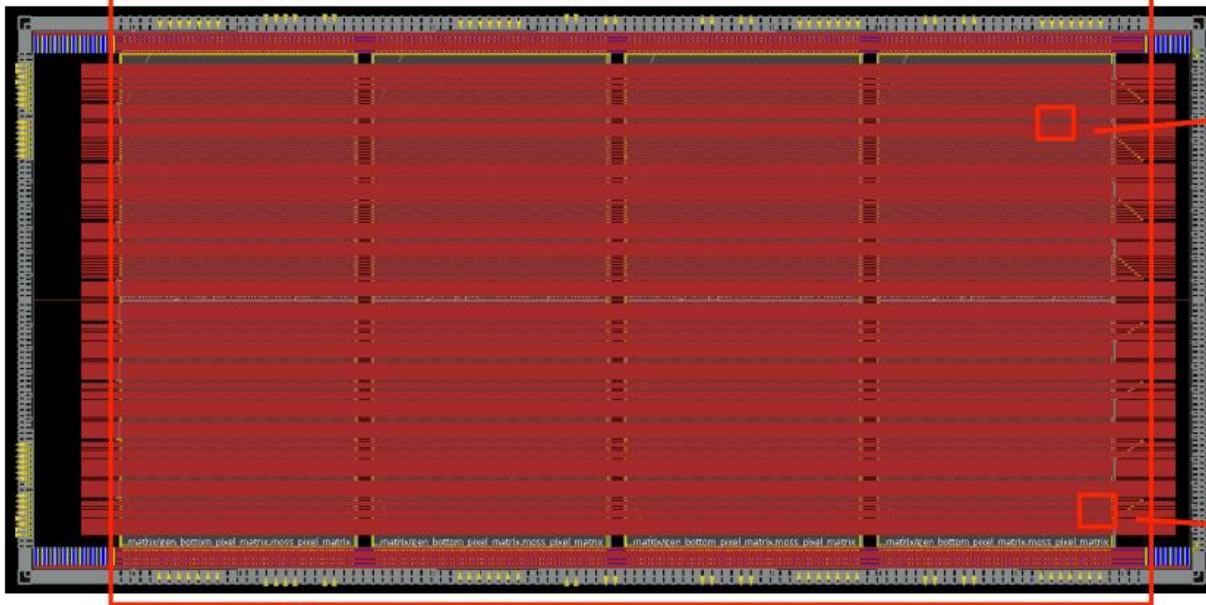
- Pixel digital
  Dynamic energy 2.32pJ
  Static energy 16.2fJ for 5us
  Static leakage current 2.71nA

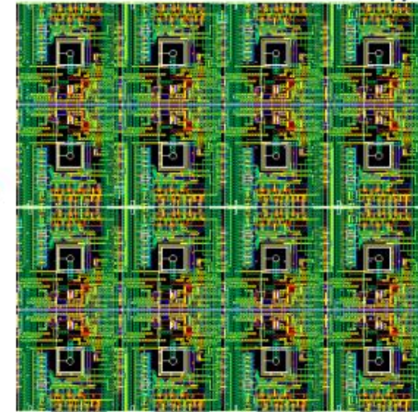
- Group digital
  Static energy 3.65pJ for 5us
  Static leakage current 608nA

# Pre-mock submission – Dec 2021

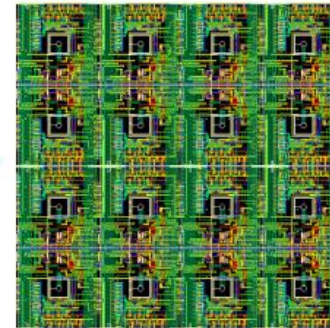


1 of 10

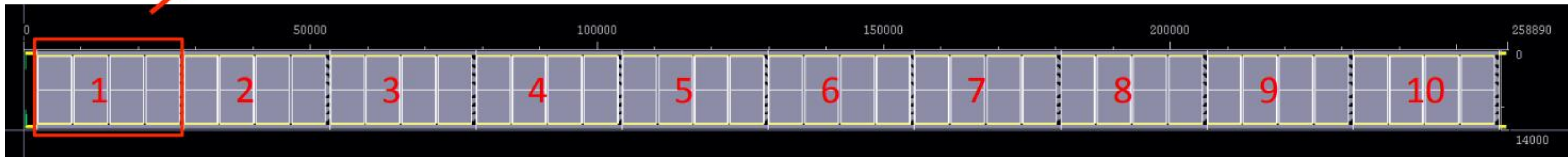




Pitch 22.5 um



Pitch 18 um




https://indico.cern.ch/event/1104620/

# Next generation sensor design for LS3

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- Good timing (10's of $ps$?)
  - Avalanche photodiode
  - Digital operation without the analog front end
- High spatial resolution
  - Pixel detector
- Low power consumption
  - Low digital activity (~ low occupancy)
  - Digital periphery with the sparcified readout
- Simple operation
  - Built-in tolerance in the APD operation

# Digital pixel coupled with low gain APD

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- Thick epitaxial layer of about 25 μm for charge collection

$$Q_{Gen} = 0.1 \cdot 50e/\mu m \cdot 25\mu m = 0.1 \cdot 1250e = 125e = 2.0 \cdot 10^{-17}C$$

- Low gain APD ($m = 50$)

$$Q_{Col} = m \cdot Q_{Gen} = 1.0 \cdot 10^{-15}C$$

- Collection electrode with small capacitance

$$C = 3.2\ fF$$

- 1.2(V) LVCMOS digital pixel operation

$$V_{Sig} = \frac{Q_{Col}}{C} = 0.313\ V > V_{th} = 0.3\ V$$

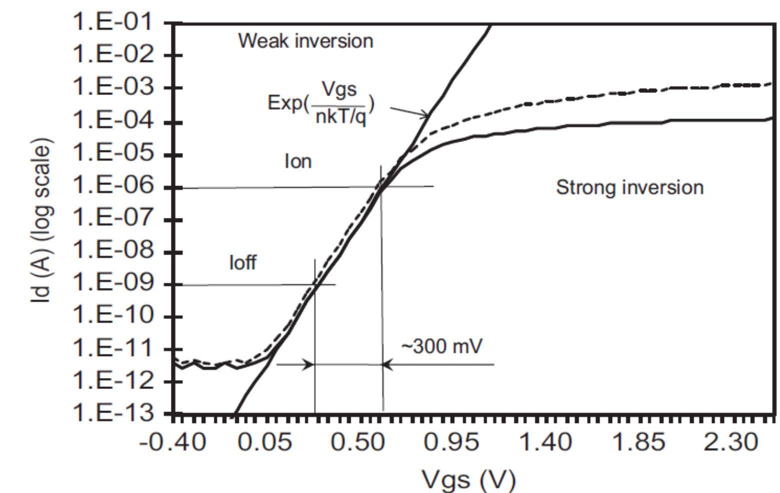
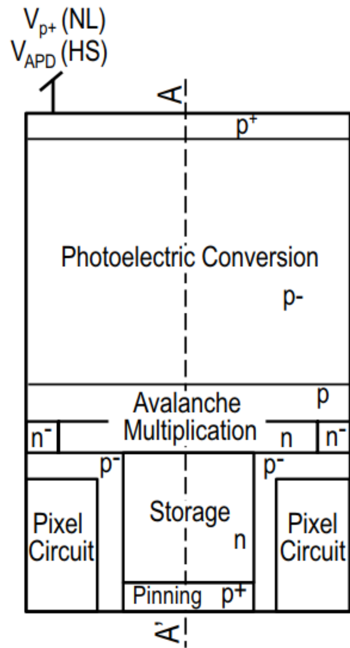
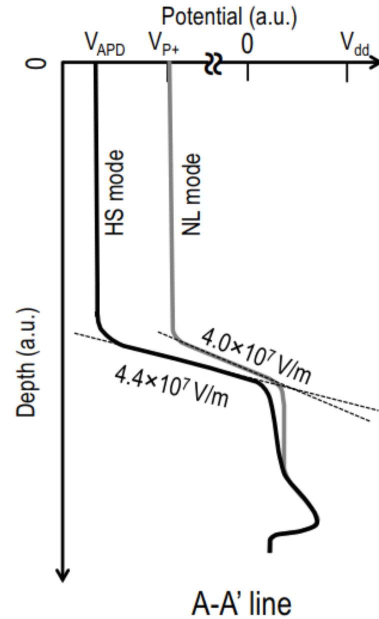


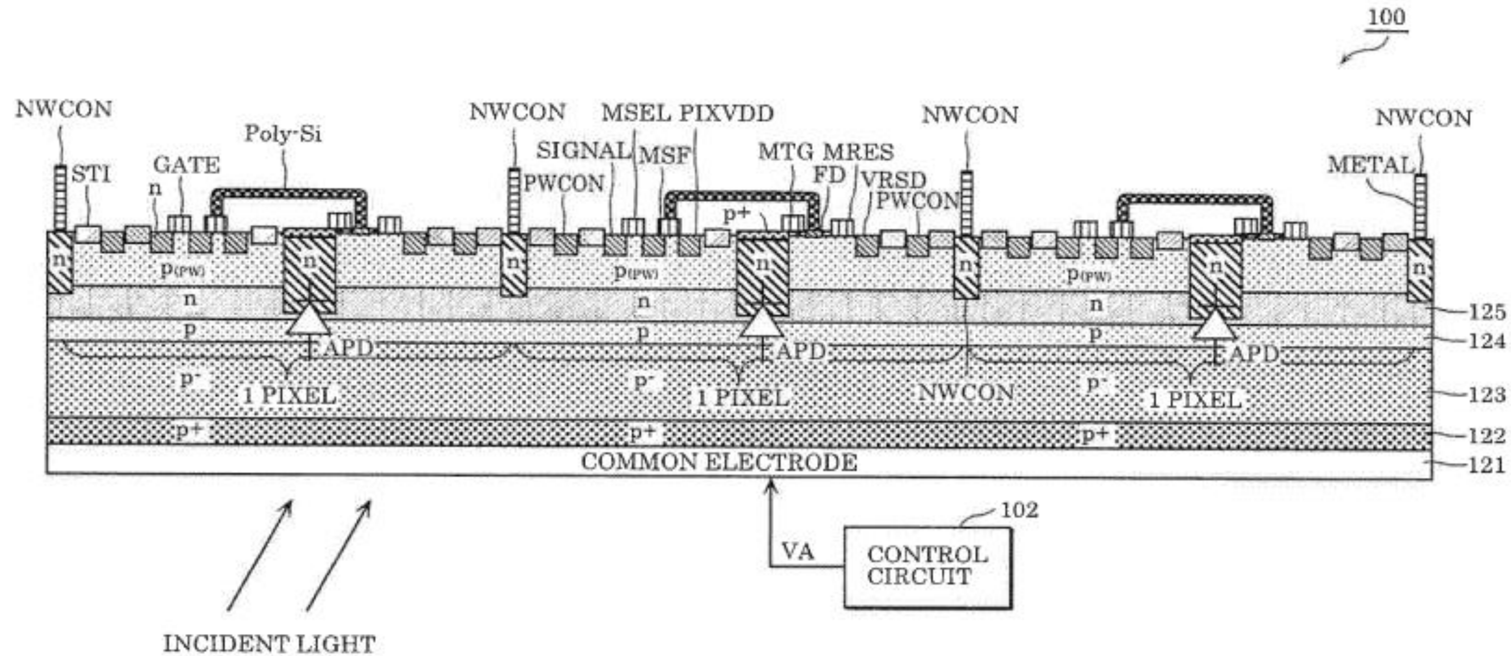

**Fig. 4.** Log(Id) vs Vgs for an example transistor, 300 mV are necessary to increase the current by a factor 1000.

Snoeys, W. "CMOS monolithic active pixel sensors for high energy physics." Nuclear Instruments and Methods in Physics Research Section A 2014

# Publications of interest



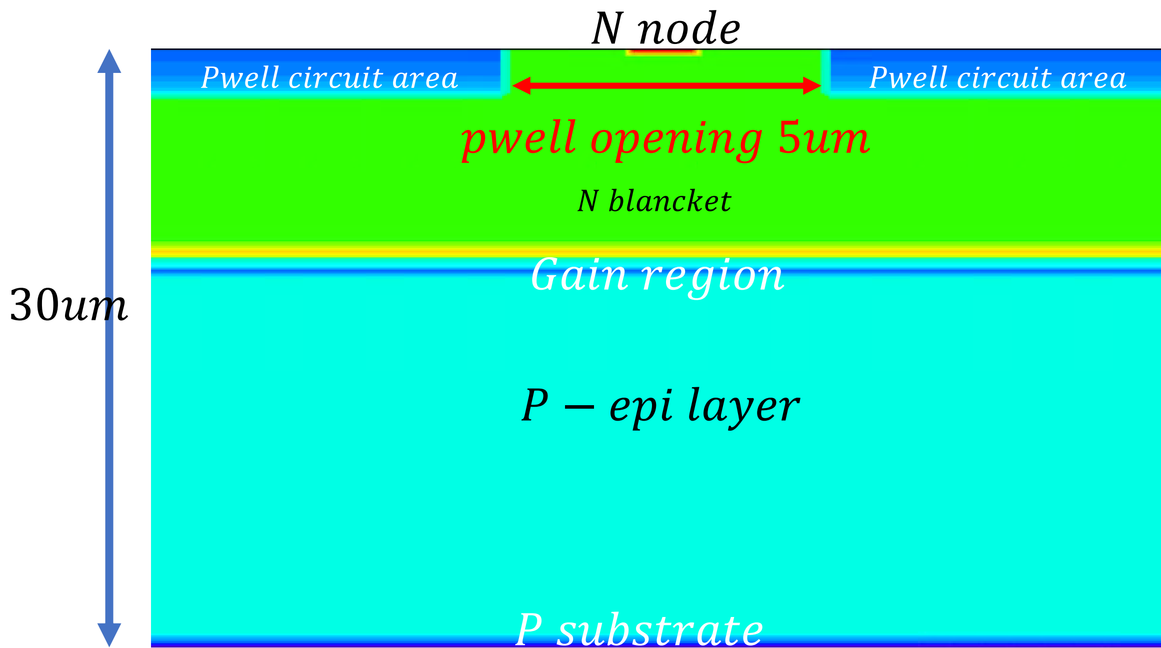




- 3.8um pixel
- Normal mode / High-sensitivity mode
- Abrupt p-n junction between a p- region and n region
- Vertical field strength is controlled by the potential of a surface p+ layer (either $V_{p+}$ or $V_{APD}$)

Mori, Mitsuyoshi, et al. "6.6 A 1280× 720 single-photon-detecting image sensor with 100dB dynamic range using a sensitivity-boosting technique." 2016 IEEE ISSCC
Patent EP 3448018A1 - PANASONIC 2019

# APD into the pixel

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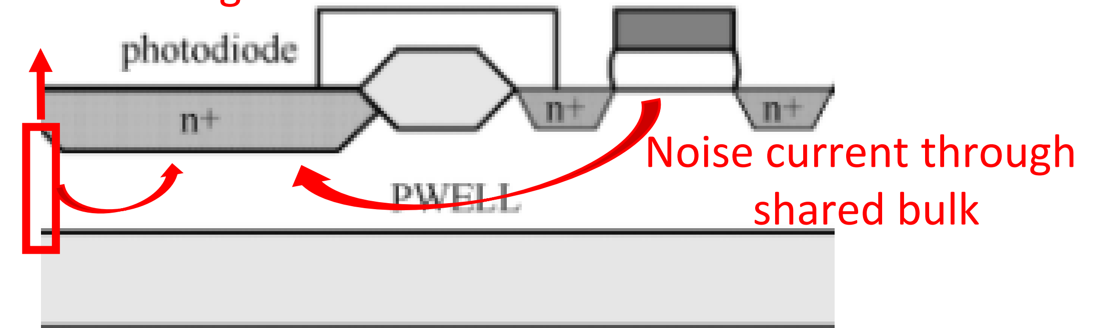
# Junction Termination Edge




Kiwon seo

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