Status and Perspectives of Silicon Detectors

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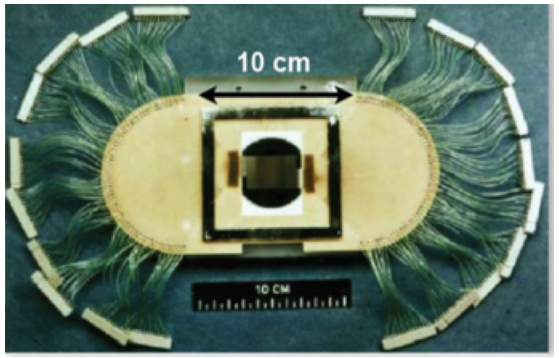
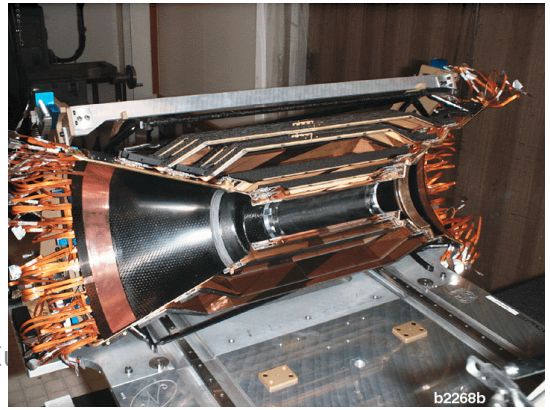
The Past: A Bit of History





First large-scale use of silicon detector in 1978-1982 in NA11/NA32 – first experiments to use a Silicon-based tracker

VLSI integration on silicon-strip trackers started in 1985

In the 90's and early 2000 many fundamental results were obtained thanks to silicon-based vertex tracker: CDF, LEP-based experiments, BaBar, all using silicon strip detector with readout at their edges .

The development of Silicon-based detectors followed, and profited from the continuous innovation in the microelectronics sector, making it possible to build ever more complex, reliable, and precise detectors

Silicon detectors are common among HEP experiments, but after 40 years of evolution they are still one of the most technologically advanced detectors

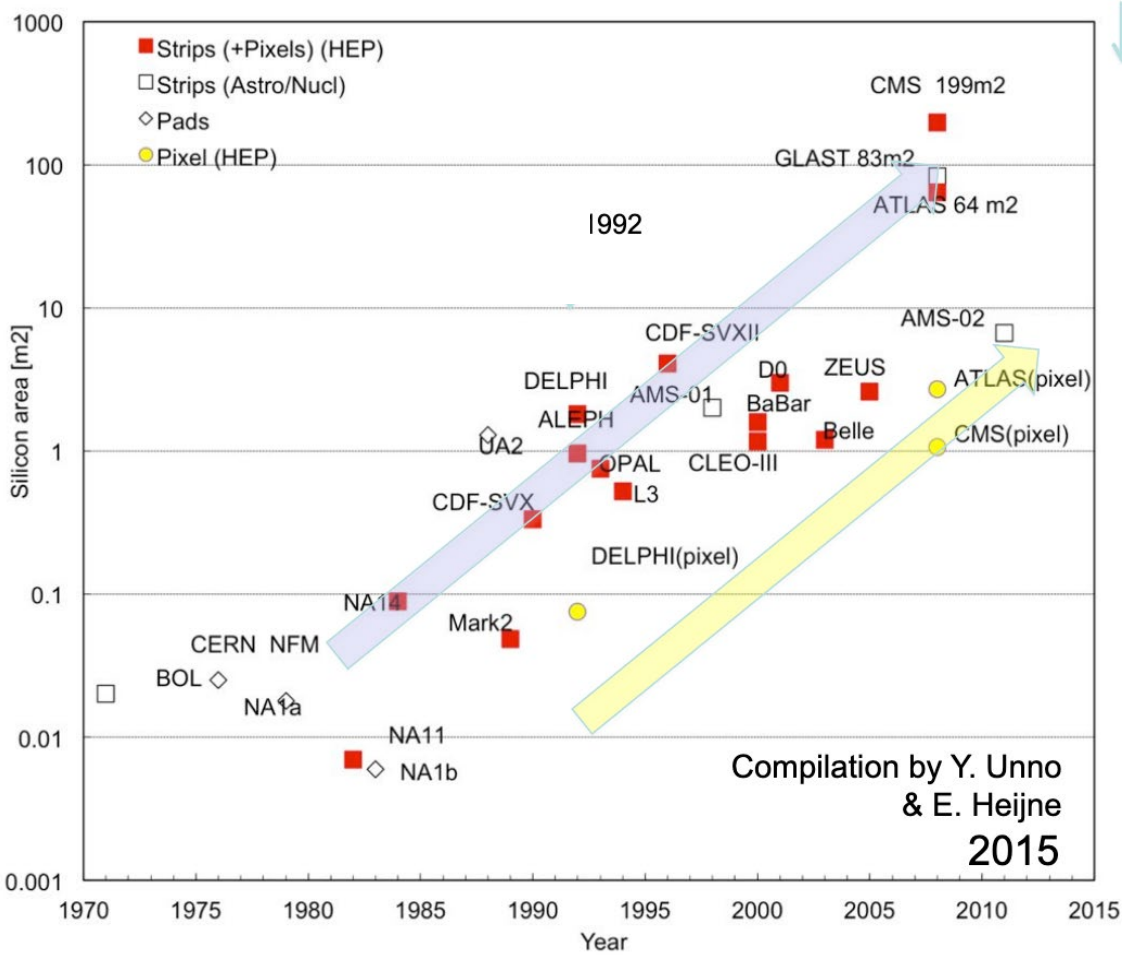
Silicon Detector Evolution

The surface and hence the number of channels of silicon detectors increased exponentially in time

Tracking systems operate the closest to the interaction region → harshest environment in term of radiation hardness

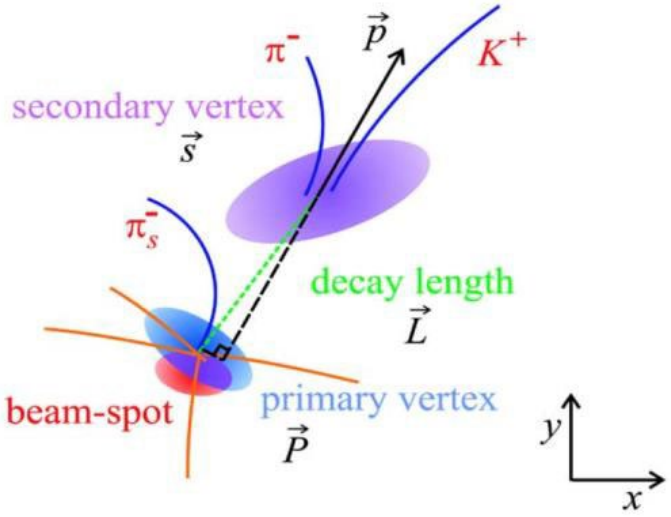
With high rate environments and the need of better resolutions Pixel systems have been the core of the tracking systems of the present era

Different environments of operations call for different solutions with a continuing evolution in technologies, segmentation, and surface increase



Similar goals, different environments, different solutions

$$D^{*+} \rightarrow D^0 \pi_s^+ \rightarrow (K^- \pi^+) \pi_s^+$$



Detector development and choice depends on physics, environment, and beam line driven constraints

EIC

Higher B-Field and larger beam pipe → farther first point for tracking → need better resolution

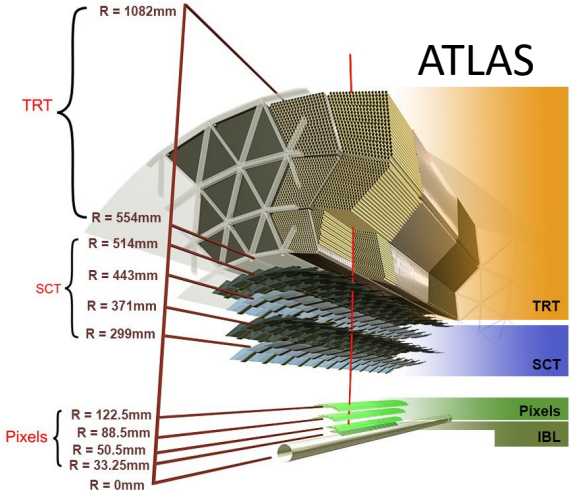
Background from collisions → Higher granularity, looser requirements on timing

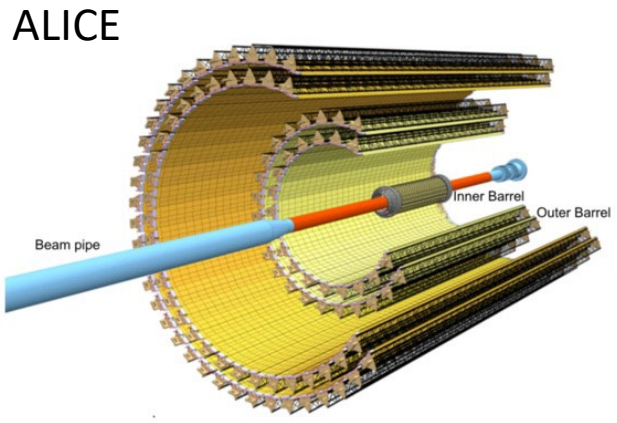
Belle-II upgrades

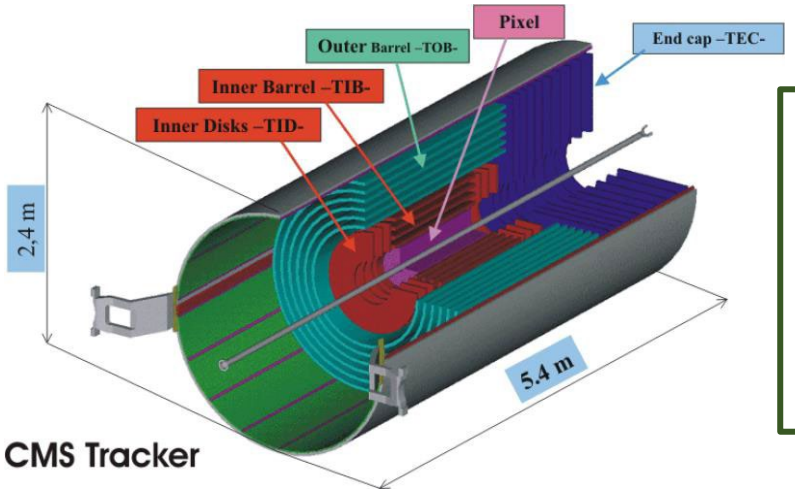
Smaller beam pipe → closer to beams → higher radiation

Background from beams → better timing resolution needed

The Present: The LHC-Era







Similar characteristic: Pixel + strips (+ other tracking systems)

Hybrid Pixels used by all experiments

ATLAS and CMS detectors tracking systems operate in high B-Fields

All the trackers designed to survive 10^{12}n.eq. Fluencies

ATLAS and CMS Performances for single point resolution of O(10)um, vertex position resolution

ALICE has poorer resolution O(1-10) mm but is able to cover larger transverse momenta range

The Present: The LHC-Upgrades

LHC HI-Lumi upgrade is the earliest benchmark for new silicon detector technologies

Fluency from 10^{12} to 10^{16} n.eq. → radiation hardness for all pixel

Need to cope with higher rate → smaller sensors and higher data flow

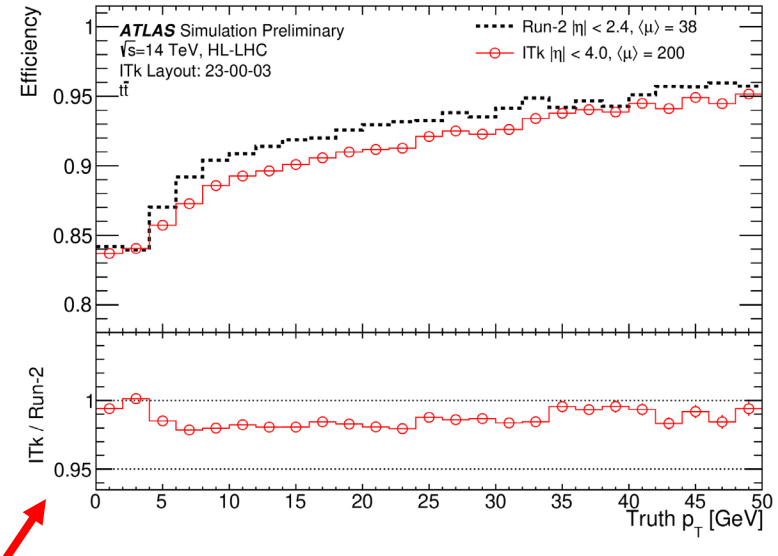
CMS and ATLAS →

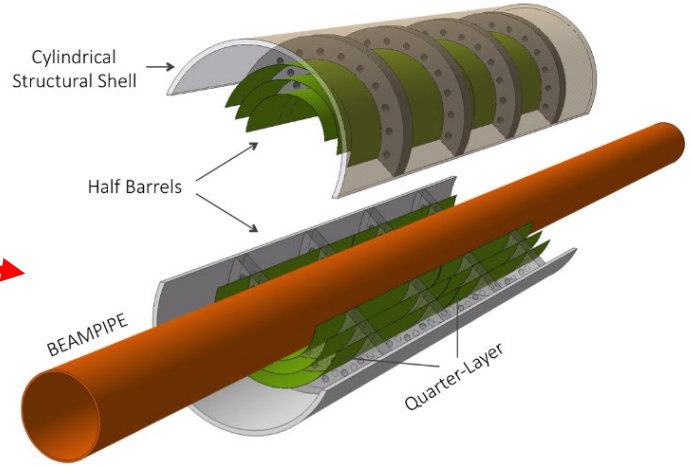
- Increase the eta coverage and the surface of silicon detectors.
- Similar technology, upgrade with hybrid pixels
- Better performances expected even in higher pile-up conditions

ALICE →

- Going for a fully silicon based tracking system
- New technology → first use of monolithic pixel sensors for HEP

ATL-PHYS-PUB-2021-024





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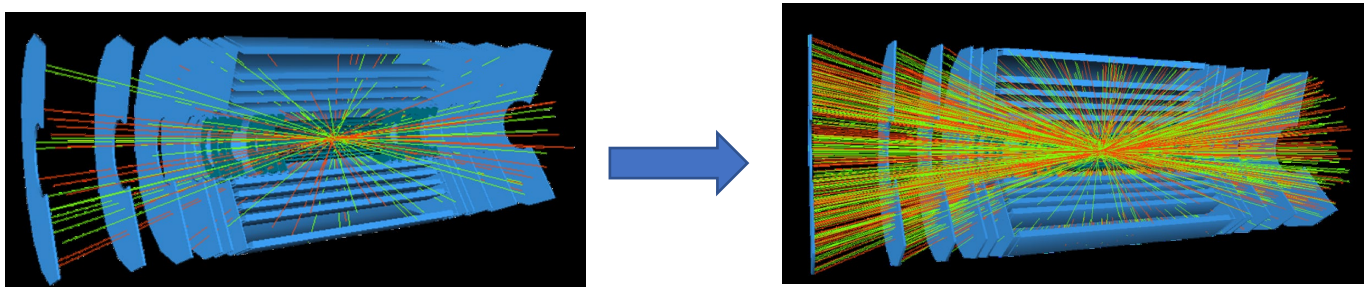
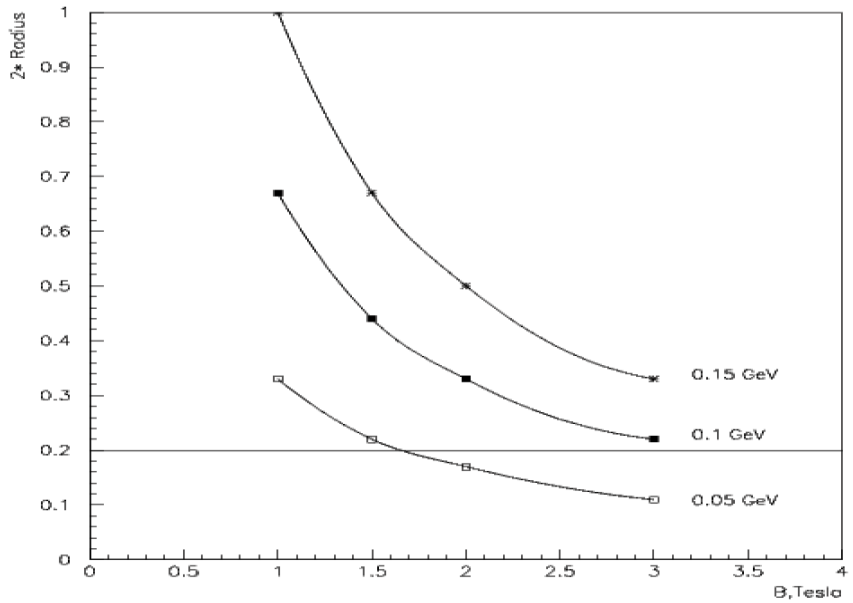
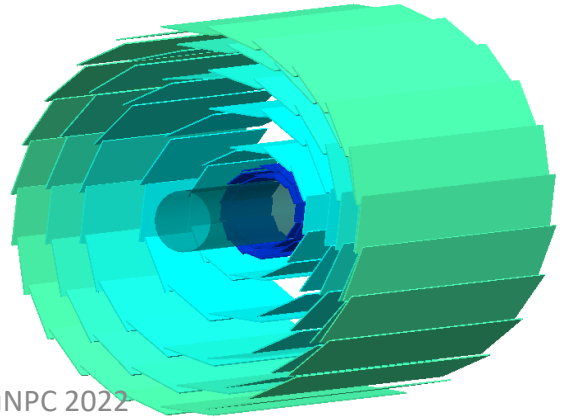


Future experiments: the EIC case





Need to measure down to very low pT: stand-alone tracking capabilities → many measurement points, small lever arm

At least 3 layers needed in the innermost region of the detector <20 cm radius to measure particles of 150MeV pT

Need to minimize thickness to reduce MS → need thin detectors goal is 0.05% X_0

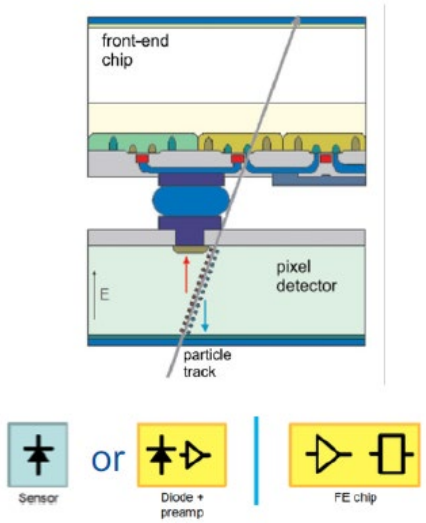
High spatial resolution 20 um resolution goal on single point measurement

Need to sustain high radiation doses and high rate → only possible solution monolithic pixels

Two Families of Pixels

Inner detectors, and in particular pixels are the most constrained component of a detector: harshest environment, large number of channels, need to be light.
Depending on physics case and environment they must satisfy additional constraints. Once the goals and constraints are set pixel inner detector can come in two flavors

Hybrid



Sensor and Front-end electronics are placed on different substrates

Development happens separately

No technology commonality needed

The substrates need to be connected

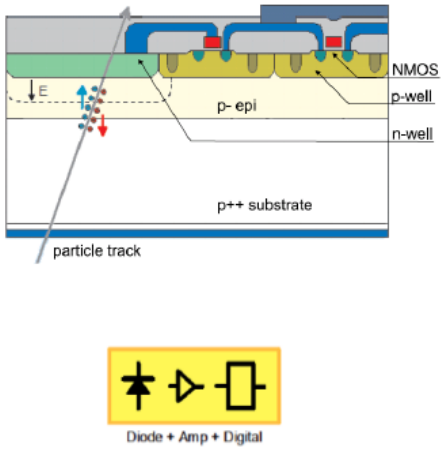
Monolithic

Sensor and Front-end electronics are designed in the same substrate

Development of both happens simultaneously

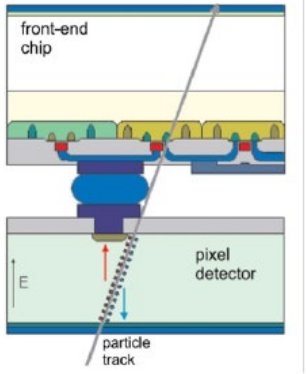
Need to share the production process

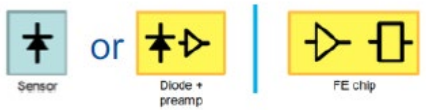
No connection needed between Sensor and FE



Hybrid and Monolithic Pros and cons

Hybrid





Each component developed separately

High resistivity sensors good option in terms of radiation hardness

Interconnection is expensive and limits the pitch reduction

Thick (two layers)

Large Sensors

Monolithic

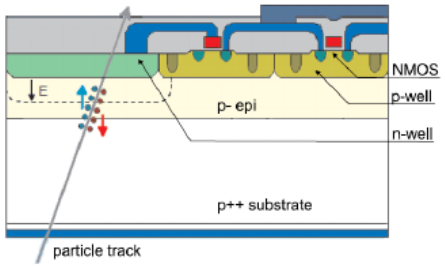
Industrial process → can be reproduced in large scales

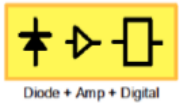
Reduction of charge collection with high Radiation doses

No need for interconnection, small pitches achievable

Thinner (one layer)

Limited module sizes





Now

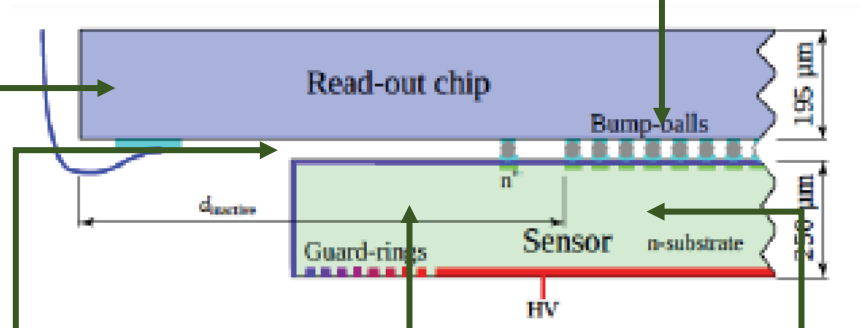
Future

Hybrids: paving the future

How can we overcome the limitations of hybrid pixels in harsher operation conditions and for larger areas?
many paths are in front of us

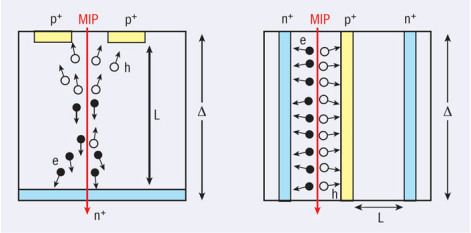
Improve efficiency at the edges (slim-edges)

Pixel size, pitch, and interconnection technologies



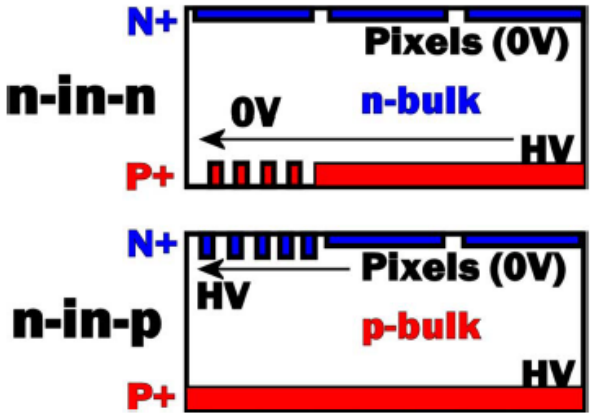
Avoid discharge at the edges of sensor

Different sensor technologies



Sensor Bulk material (p- or n-type)

Hybrid: bulk material

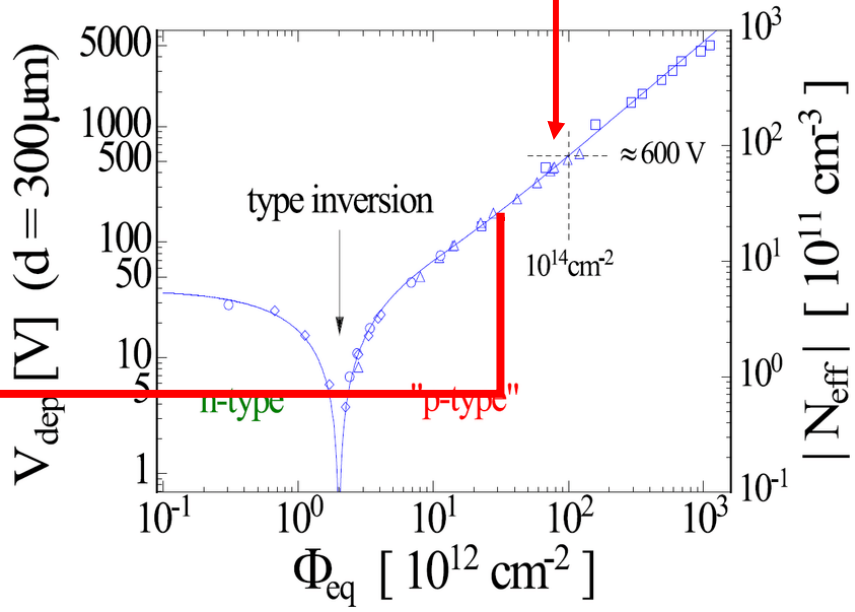


n-in-p is the used technology @ LHC

Guard ring and pixel on the same side
→ cheaper to produce than n-in-n

p-doped bulk does not undergo type inversion, on the other hand…..

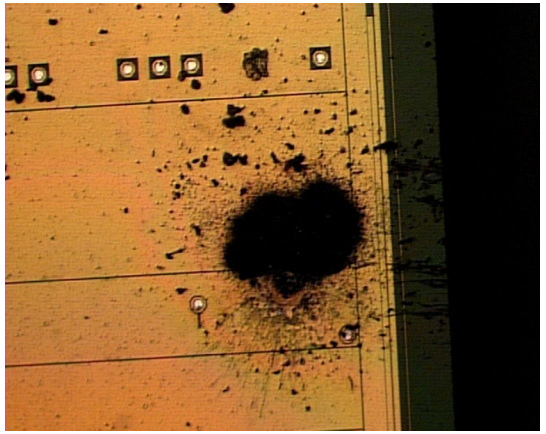
Large increase in operating voltage

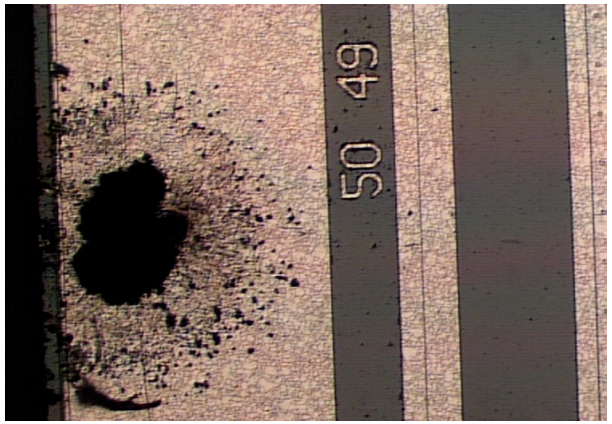


The corner of the sensor, depleted at very high V is now close to the electronics at 0V → possible damage due to sparks

Hybrid: HV protection at edges

Pixels damaged by sparks

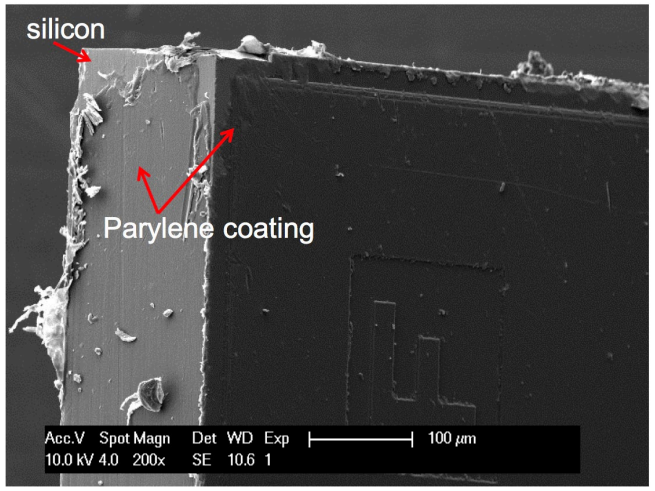




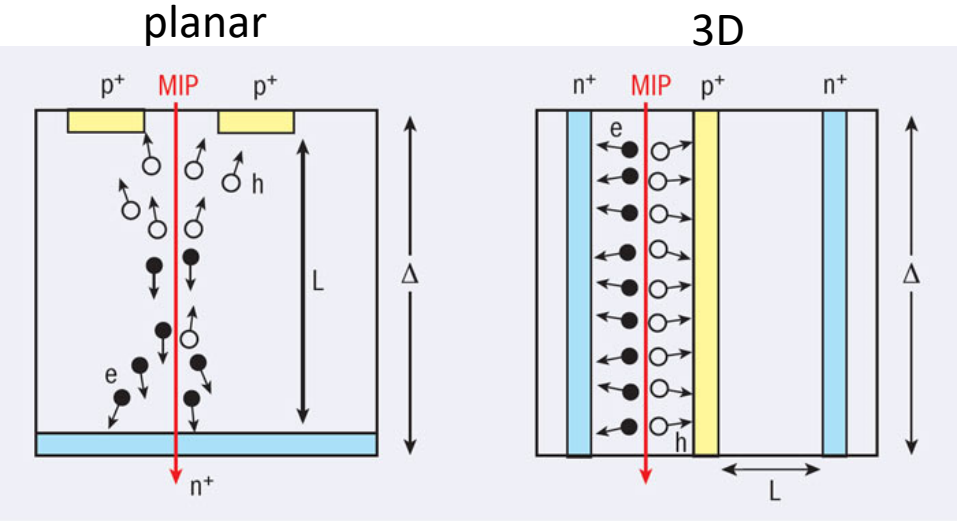
Large voltage differences (400-600V) over 10um between sensor and FE electronics may cause sparks

Need an insulation system to avoid damages to sensors and electronics→ 2 approaches

- Apply an insulation during the sensor lithography, no need to protect electronic structures during process, but expensive
- Deposit an insulating cover over the sensor: no increased complexity in production, need to protect the FE structures during deposition



Hybrid: sensor technologies



Moving from planar to 3D structure: drift is not coupled with the detector thickness → radHard

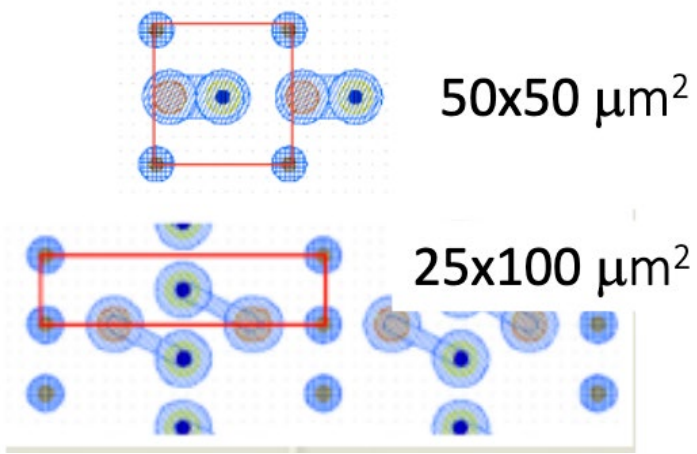
First models suffered from low efficiency along columns: mitigated by tilting the sensor w.r.t. tracks

First use on large scale in IBL upgrade for ATLAS

The 3D cell design is more complex than planar → higher prices and lower yield

Now yield is O(80%) during production

Improvement in the process allowed also for smaller pitch cells



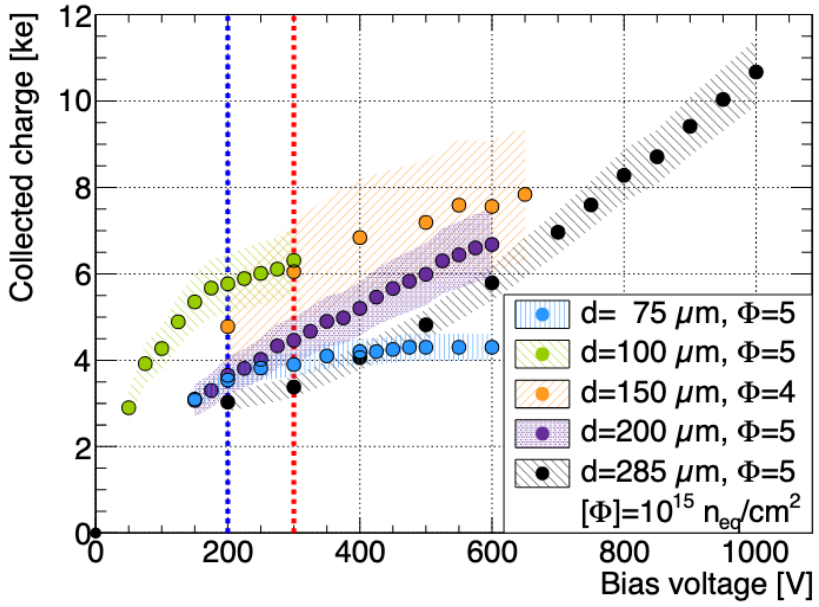
Hybrid: Thin Sensors

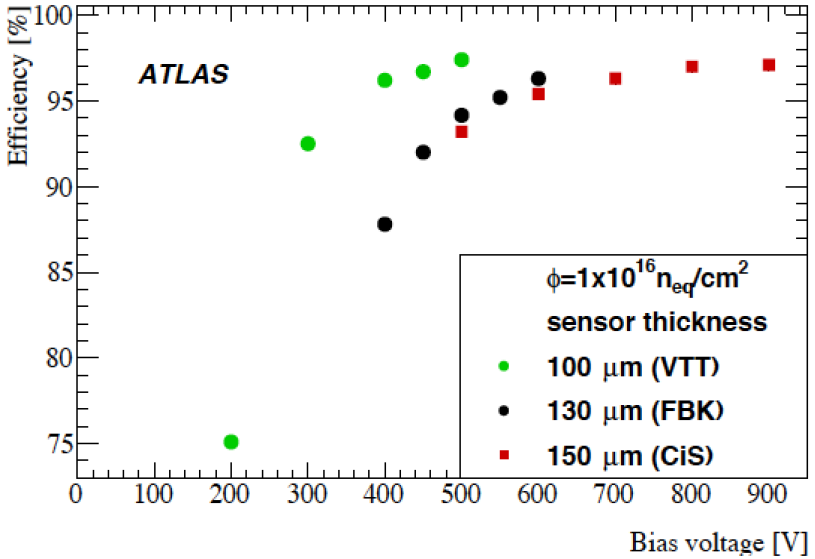
With radiation damage → large voltage need for full depletion → thinner detector easier to operate

thin sensor reduce drift length, stronger electric field, faster collection, lower power dissipation, Less material budget

They are also optimal for timing detectors!

arXiv:1612.01281





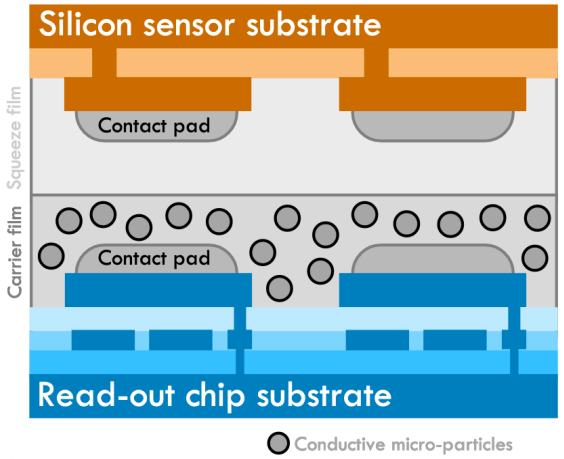
High efficiency even after irradiation and at large operating voltages

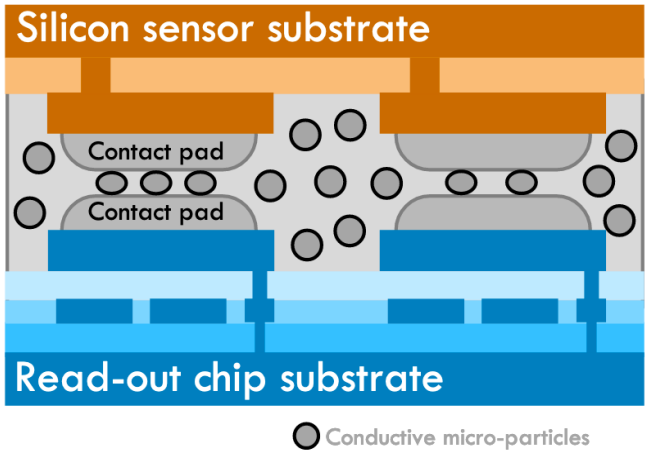
Thin detectors are reliable at track reconstruction for very long operation runs

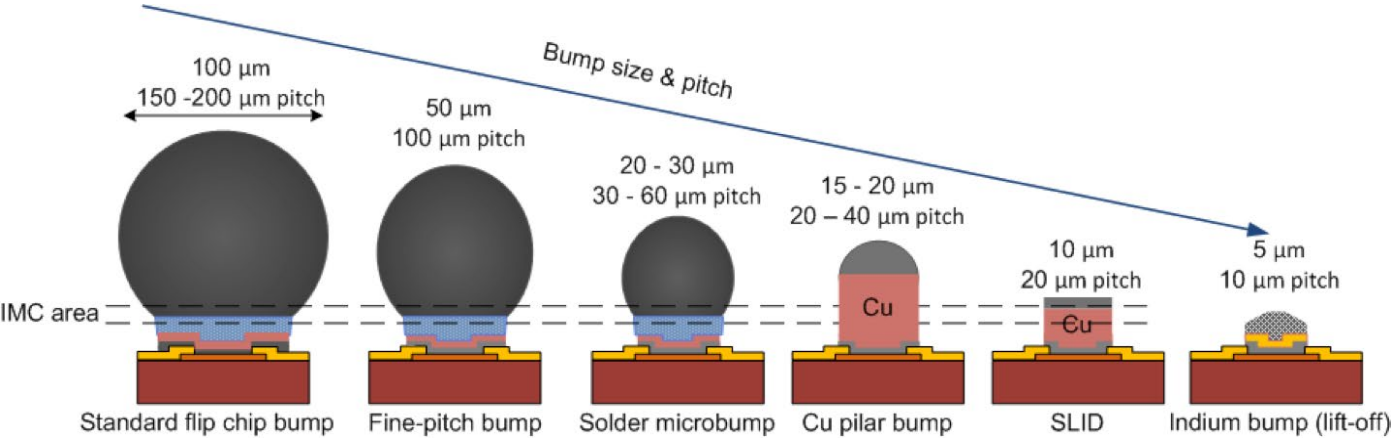
Hybrid: Small pitches

Pixel pitch and size can be limited by the interconnection size to the FE

Standard soldering or copper pillar would «limit» the pitch to 10um → new techniques needed for smaller pitches







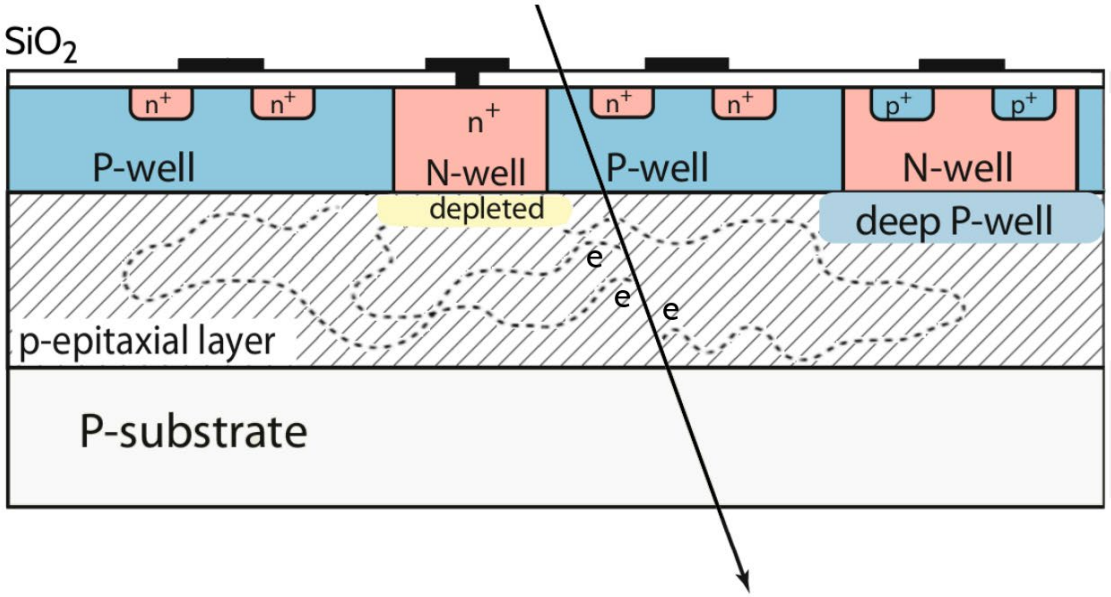
Anisotropic conducting films are now being tested for sensor front-end coupling

Cheaper options

Decouples the bump-bonding size from the minimum pixel size

https://indico.cern.ch/event/983068/contributions/4223158/

Monolithic: MAPS



Depletion zone in a thin 10-30um around p-type bulk or a high resistivity substrate

Front-end electronics designed inside a deep n-well

Production made in CMOS processes: widely available, cheap, allow for large number of detector elements

Very shallow depletion region, charge mainly collected through diffusion→ can go thin up to 50um thick detector

Allows for trackers of overall thickness of 0.3% X_0

Drawbacks:

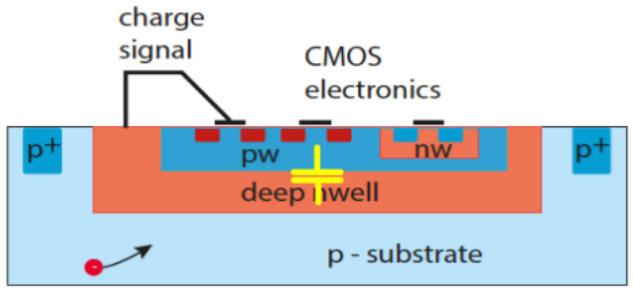
small Signal (SMIP ~ 80 eh-pairs/µm)

limited radiation tolerant

slow (charge collection by diffusion)

Monolithic: MAPS design

Large Electrodes



Electronics in collection well

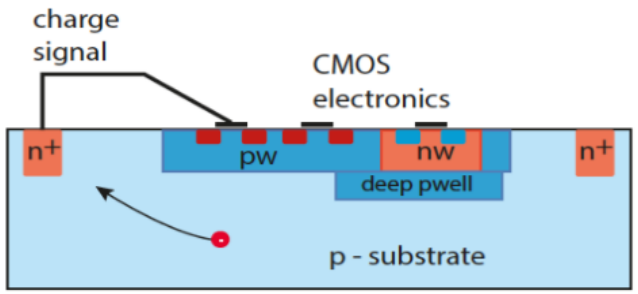
No or little low field regions

Short drift path for high radiation hardness

Large(r) sensor capacitance ->higher noise and slower

Potential cross talk between digital and analog section

Small Electrodes



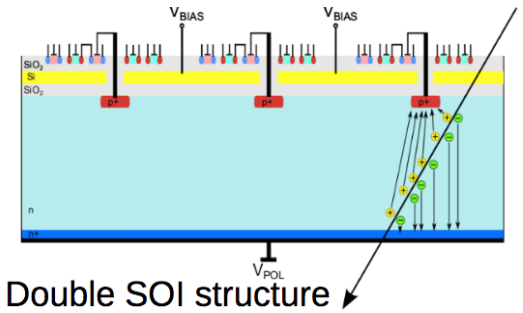
Electronics outside collection well

Small capacitance for high SNR and fast signals

Separate analog and digital electronics

Large drift path -> need process modification to usual CMOS processes for radiation hardness

Buried Electrodes



Electronics and sensor in separate layer

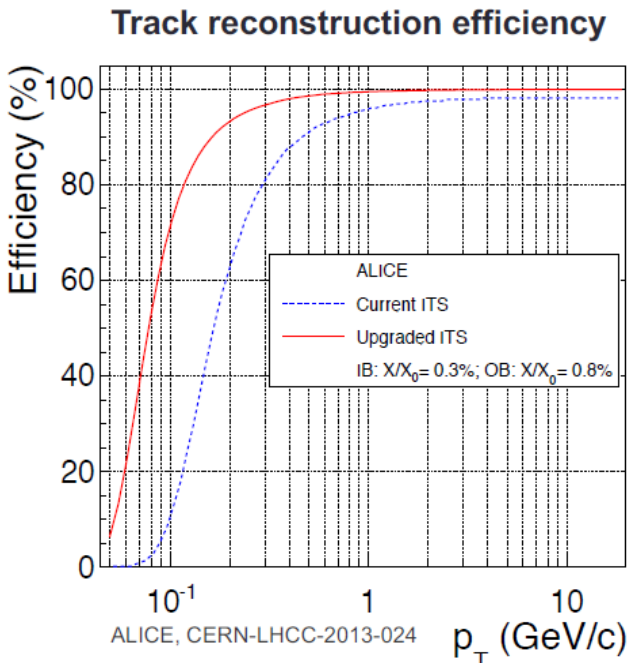
Can use thick or thin high resistivity material and HV

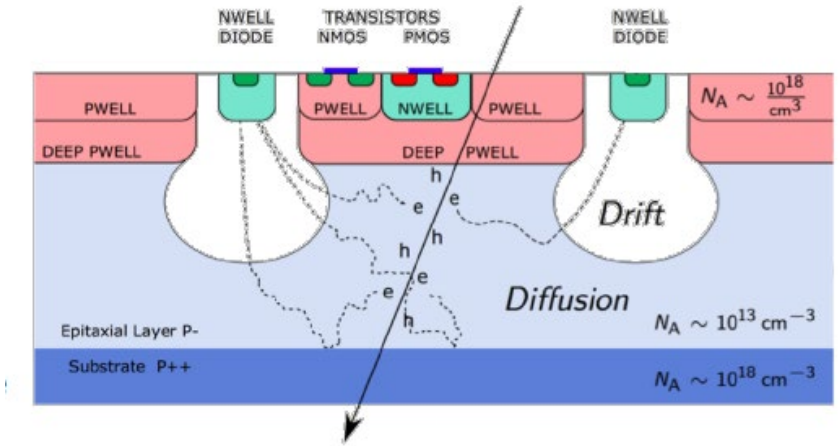
Special design to overcome radiation induced charge up of oxides

Monolithics: ALICE Upgrade

Design requirements
Get closer to IP: 39 mm→ 21 mm (layer 0)
Reduce beampipe radius: 29 mm → 18.2 mm
Reduce material budget: 1.14 % X0 →0.3 % X0 (inner layers)
Reduce pixel size: (50 µm x 425 µm)→ O(30 µm x 30 µm)

Standalone tracking for low momenta



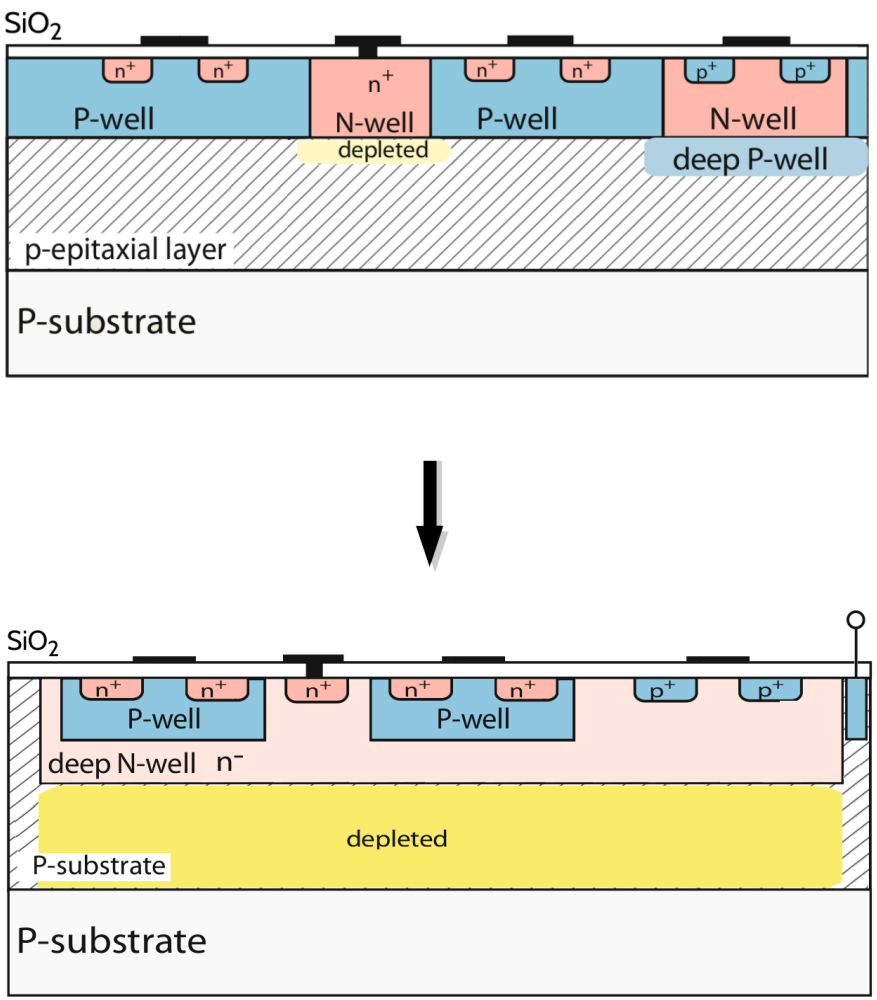


N-well collection electrode in high resistivity epitaxial layer

High resistivity (> 1kΩ cm) epi-layer (p-type, 20-40 µm thick) on p-substrate

Moderate reverse bias → increase depletion region around Nwell collection diode to collect more charges by drift

Monolithic MAPS: Depleted CMOS



Depleted → using drift CMOS pixel natural choice:

Light weight as other MAPS
Depetion region proportional to $\sqrt{V_B}$
Fast detectors → collection speed αV_B suitable for LHC-like experiments

Need to overcome technological challenges:

High Voltage processes

High Resistivity substrates

130-180 µm feature size
deep submicron technologies needed for the design of radiation hard electronics multiple well process to decouple front-end electronics from the sensitive region

HV-CMOS Mu3e experiment

planed experiment at PSI, Switzerland searches for LFV process

μ− → e−e+e− with BR 10^{-16}

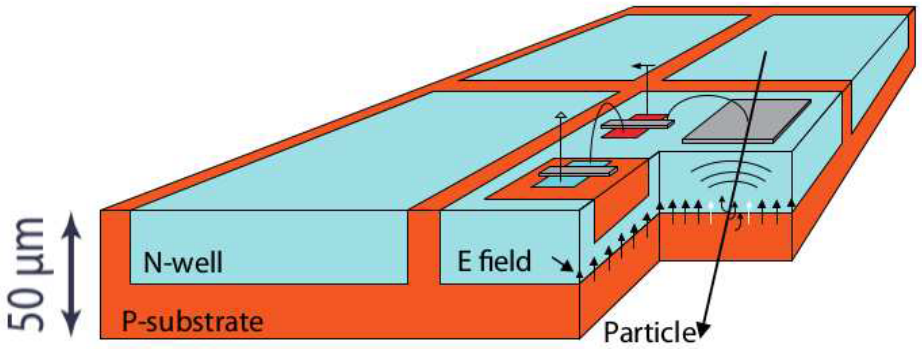
pixel Size	material Budget	time Resolution
80 × 80 μm	≤ 1 ‰/Layer	≤ 20 ns

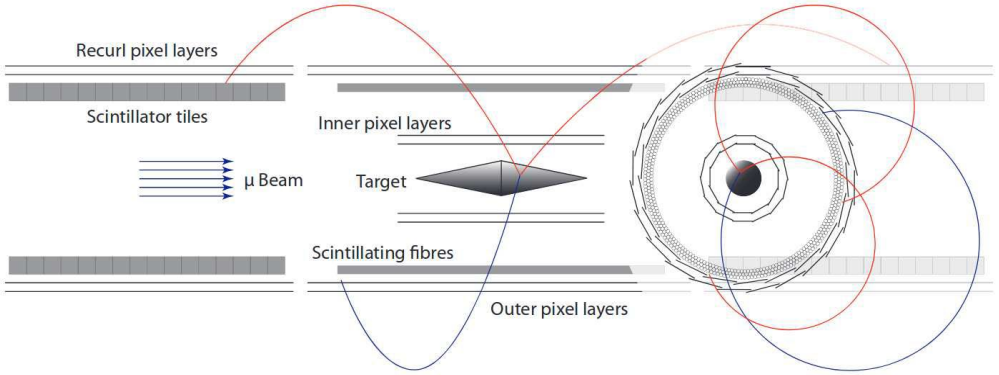
Design requirements

Need to sustain high rate of muons (up to 10^9/s)

Tracking low momenta electrons → reduce thickness up to 0.1% X_0/layer

Need Good timing resolution





A step further: 4D tracking

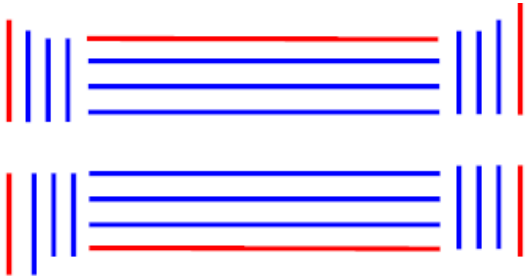
We solved the issue of ghost hits in strip detectors by using pixels: can we resolve tracks also in time to avoid ambiguities?

The question boils down to:

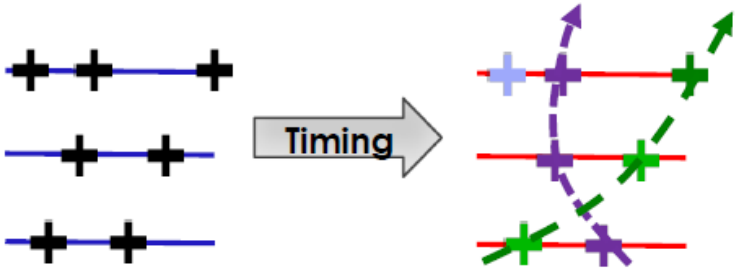
Can we achieve a 10um position resolution and
Can we achieve a 10 ps timing resolution
On the same detector?

Bonus question: can we make it also radiation hard?

Easier: single timing layer, single time and position measurement



Harder: 4D tracking, position and time for each hit along the track

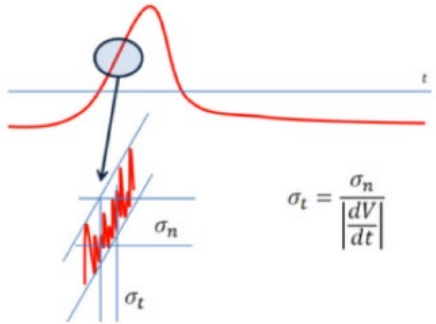


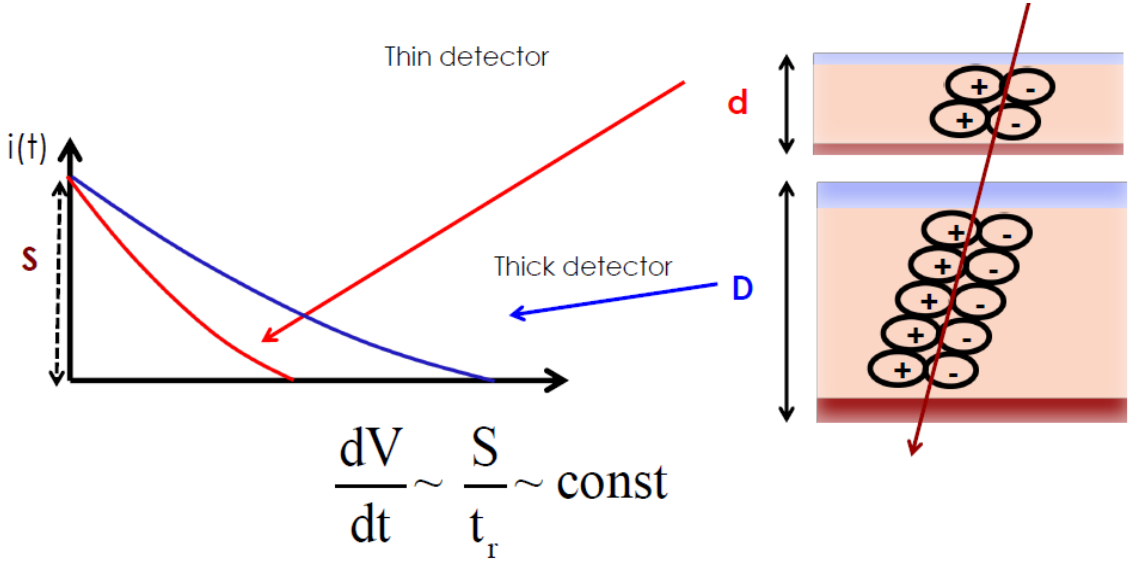
Hardest: 4D tracking, but at high rate

4D tracking: Timing resolution

$$\sigma_t^2 = \left(\frac{Noise}{\frac{dV}{dt}}\right)^2 + (\Delta Ionization)^2 + (\Delta\text{shape})^2 + \text{TDC}^2$$

Strongly depend on the rise speed of the signal → need large dV/dt





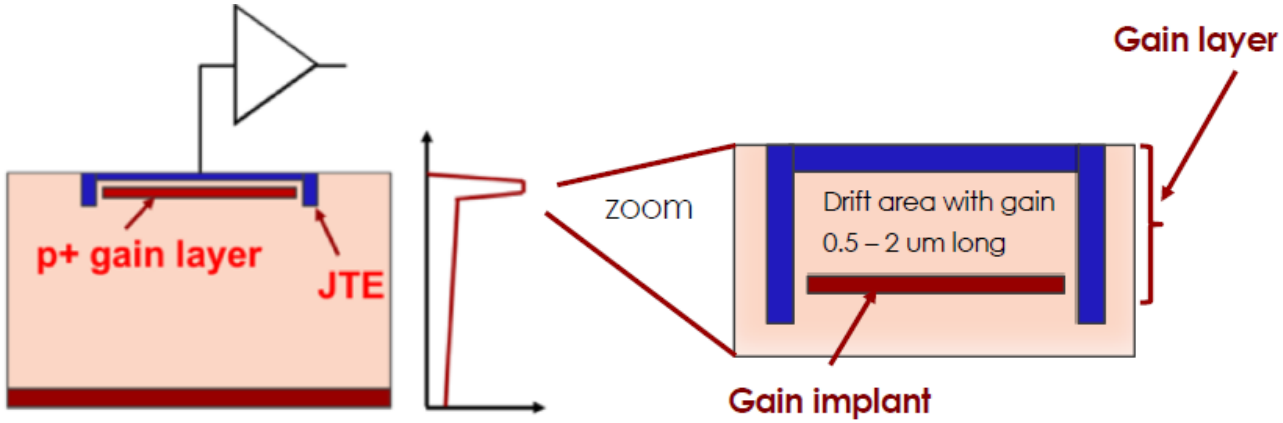
Thicker detectors have longer signals, not higher signals

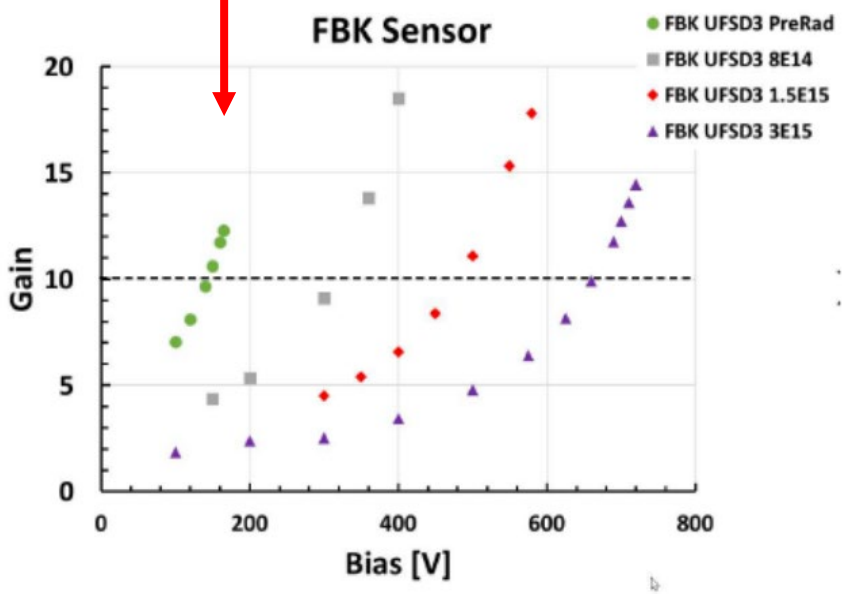
Introducing a Gain layer in a thin detector may do the trick

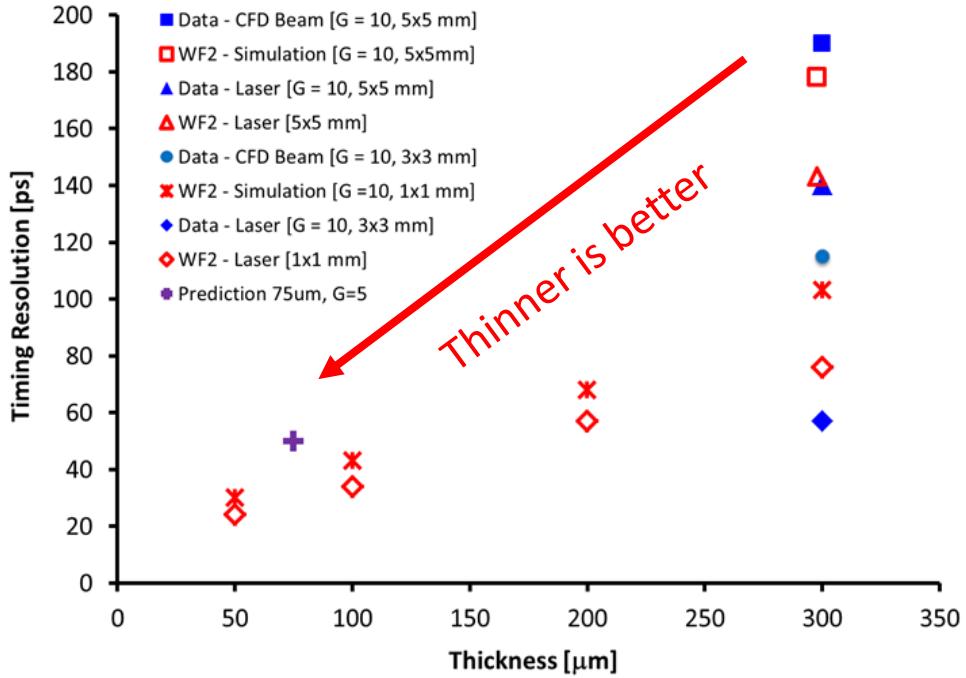
4D tracking:LGAD

Highly doped p+ region below the n+ implant
- This generates a multiplication layer
- Internal gain factor from 10x to 30x (before irradiation)

Gain decreases after radiation (de-activation of the gain layers)







Conclusion and Outlook

- Silicon detectors improved steadily over the last 40 years and are improving day by day
- The interplay with the microelectronics industry helped the developement of more complex, larger, and now cheaper detectors
- Different solutions have been developed to cope with different physics cases and environments

- With the LHC upgrades, and the new projects coming in the next decade we will see the first use in large scales of new technologies
- Hopefully after moving from 2D to 3D position measurement (strip to pixel) we will manage to add one more dimension to our measurement: time

- The next years will see the operations of new technologies and hopefully new discoveries thanks to the silicon detector development