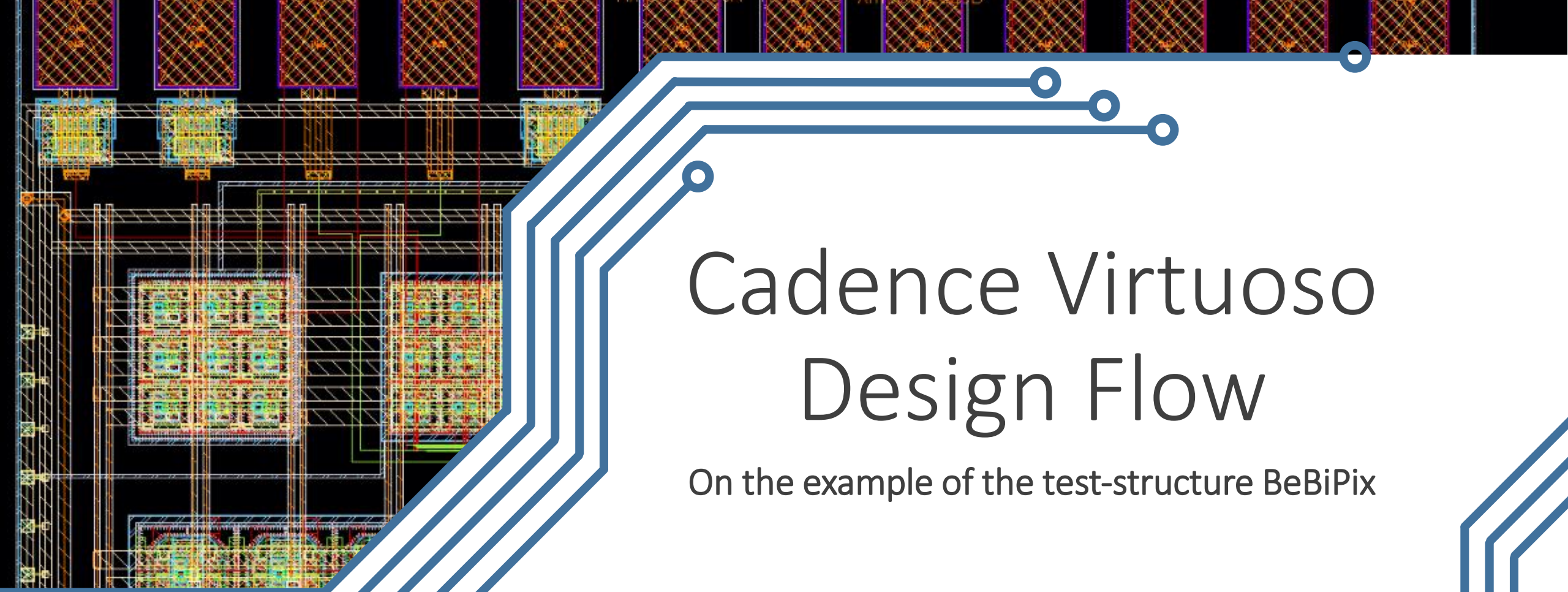


Cadence Virtuoso Design Flow

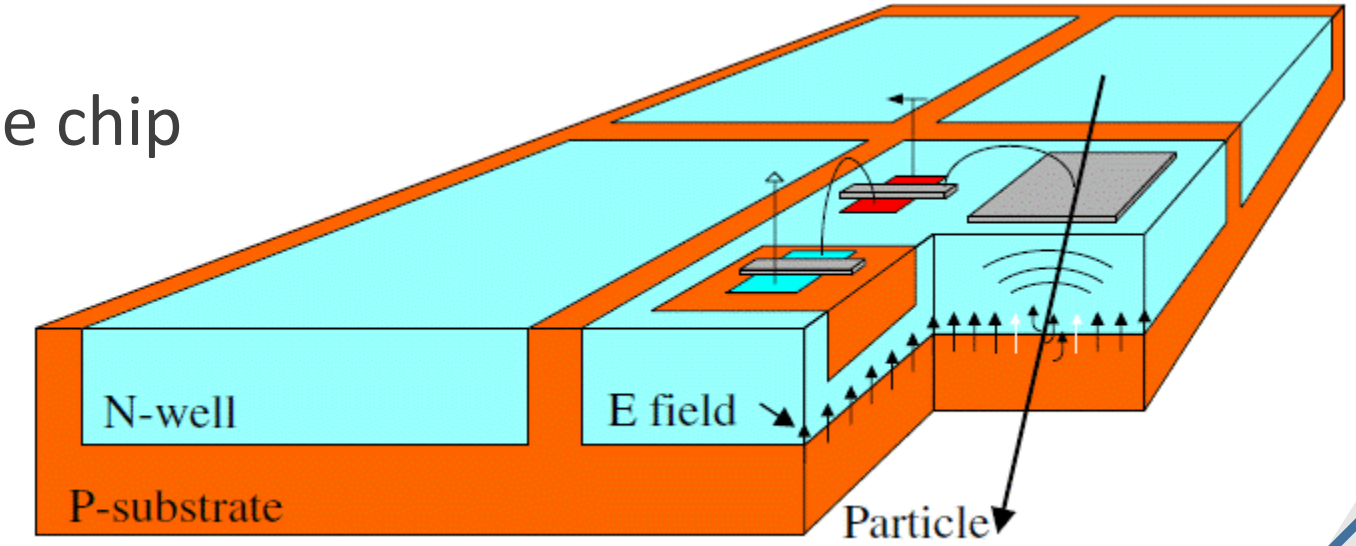
On the example of the test-structure BeBiPix

Benjamin Weinläder

08.06.2022

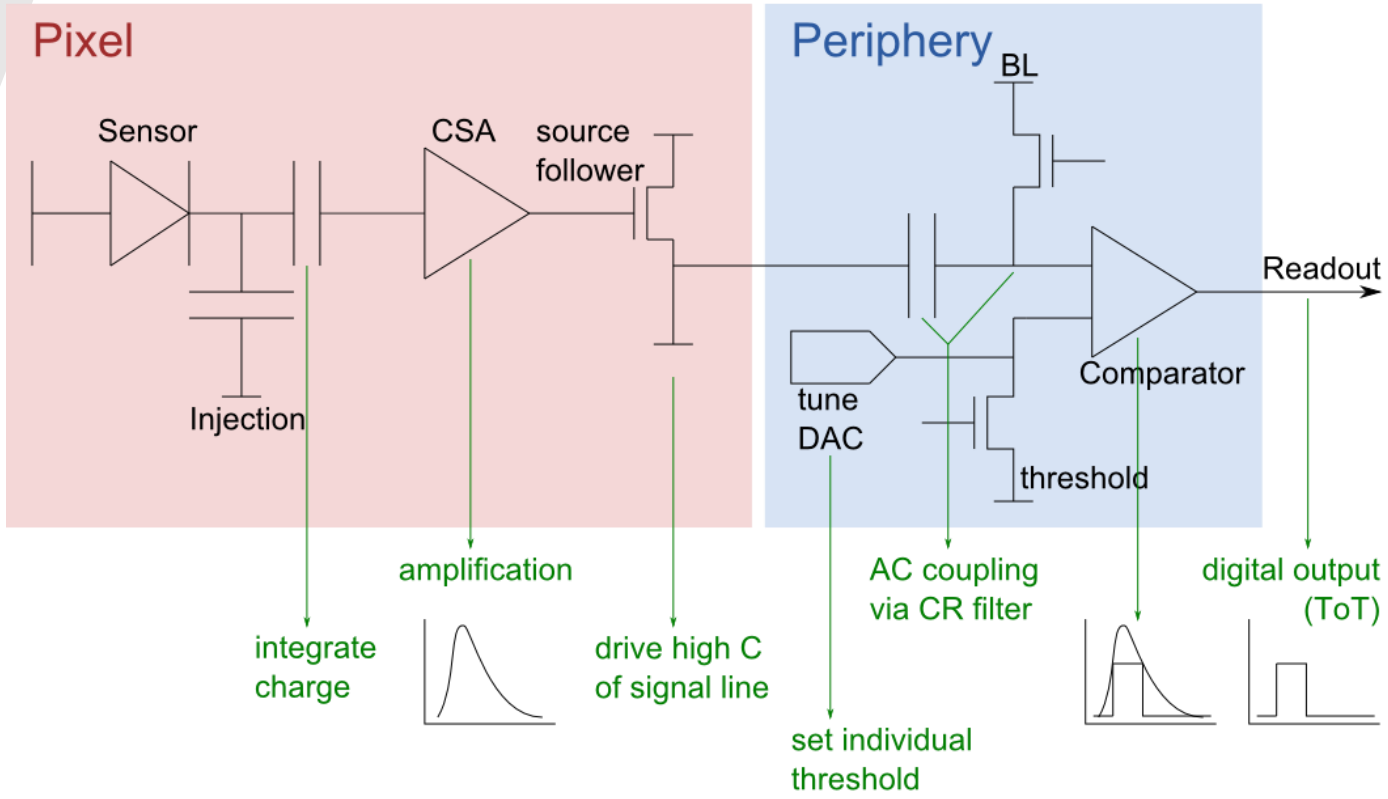
High Voltage – Monolithic Active Pixel Sensors

- detection and readout on one chip
  - in-pixel electronics
- high voltage $\sim 100V$
  - fast charge detection via drift
  - large depletion area
- commercially available processes
- possibility to thin sensors to $\sim 50\mu m$



I. Peric, P. Fischer et al.:
NIM A 582 (2007) 87

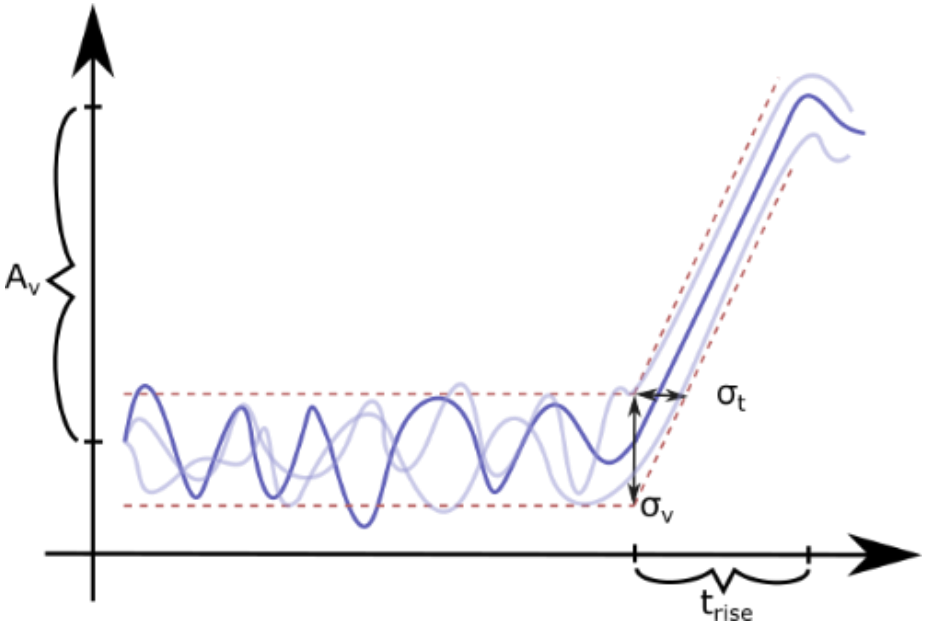
High Voltage – Monolithic Active Pixel Sensors



typical readout schematics:

- in-pixel charge sensitive amplifier
- digitisation in-pixel is possible
- further processing in the periphery

Starting Point: BeBiPix



Task:

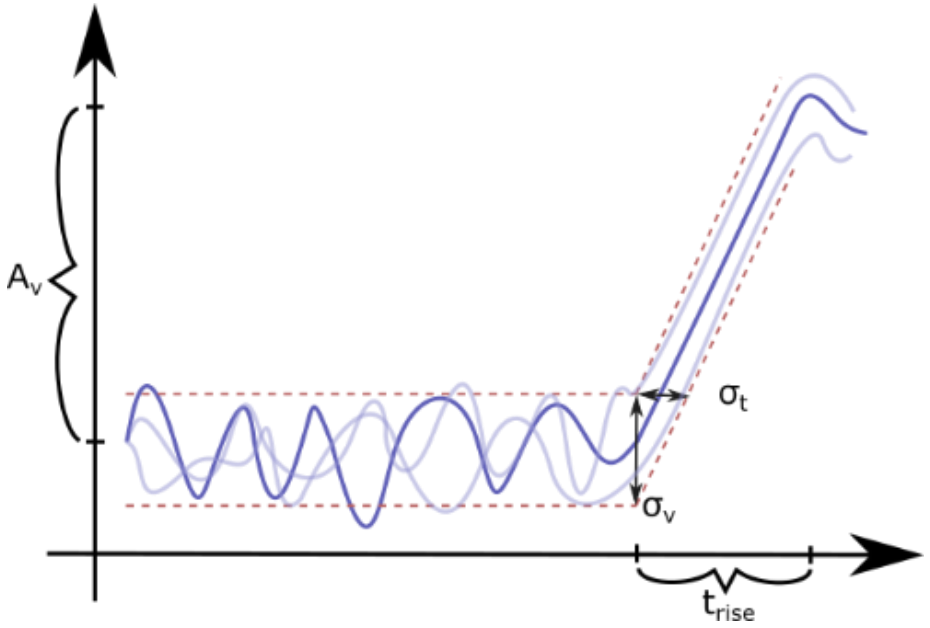
- reduce time resolution to sub-nanosecond regime
- benefit from advantages of BiCMOS-Technology
  - combination of bipolar (HBT) and MOS transistors
- simplified model for the time resolution:
  - $\frac{\sigma_t}{\sigma_v} \approx \frac{t_{rise}}{A_v} \rightarrow \sigma_t \approx \frac{t_{rise}}{SNR}$

mostly influenced by the amplifier
→ use bipolar transistor here

Advantages of BiCMOS

- $\frac{\sigma_t}{\sigma_v} \approx \frac{t_{rise}}{A_v} \rightarrow \sigma_t \approx \frac{t_{rise}}{SNR}$
- comparison MOSFET and BJT:
  - τ = integration/measuring time

$$ENC^2 \sim \frac{a}{2\tau} C_{in}^2 + \frac{\tau}{2} b + 2cC_{in}^2$$



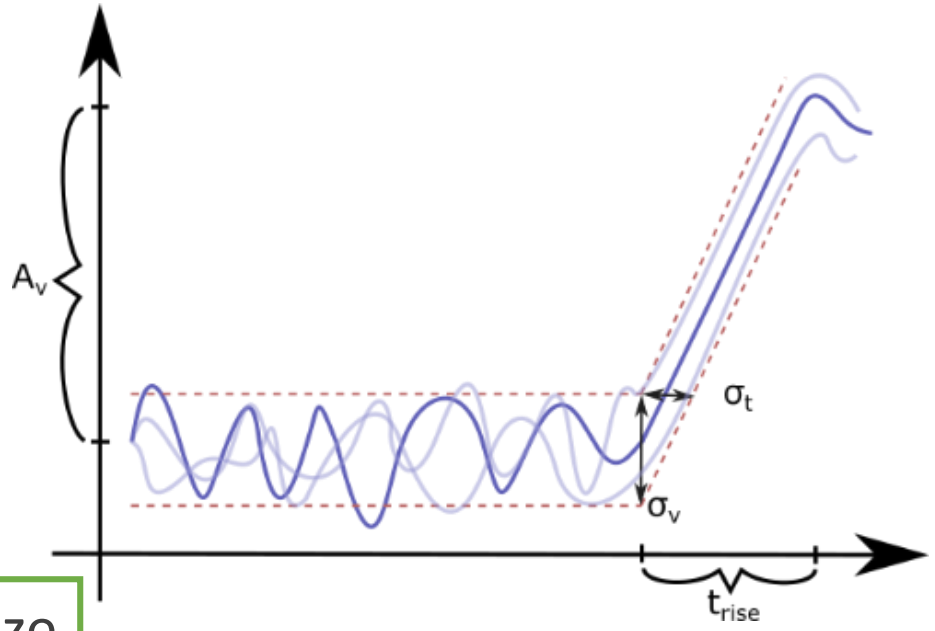
	MOSFET	BJT
a	therm. noise	shot noise
b	shot noise (leakage current)	shot noise (leakage current)
c	$1/f$-noise	-

Advantages of BiCMOS

- $\frac{\sigma_t}{\sigma_v} \approx \frac{t_{rise}}{A_v} \rightarrow \sigma_t \approx \frac{t_{rise}}{SNR}$
- comparison MOSFET and BJT:
  - τ = integration/measuring time

$$ENC^2 \sim \frac{a}{2\tau} C_{in}^2 + \frac{\tau}{2} b + 2cC_{in}^2$$

$\sim\tau \rightarrow$ minimize



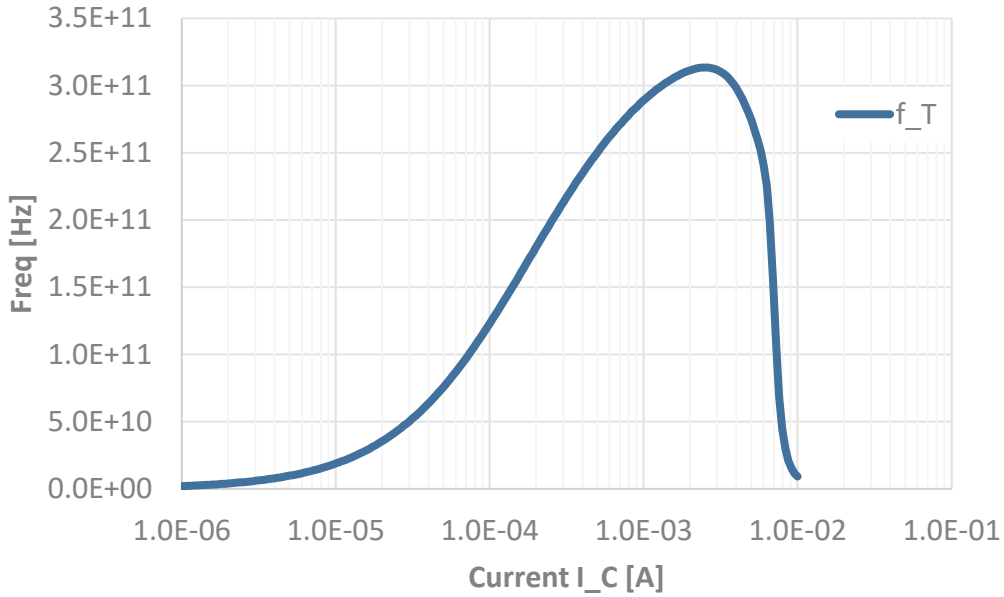
	MOSFET	BJT
a	therm. noise	shot noise
b	shot noise (leakage current)	shot noise (leakage current)
c	$1/f$-noise	-

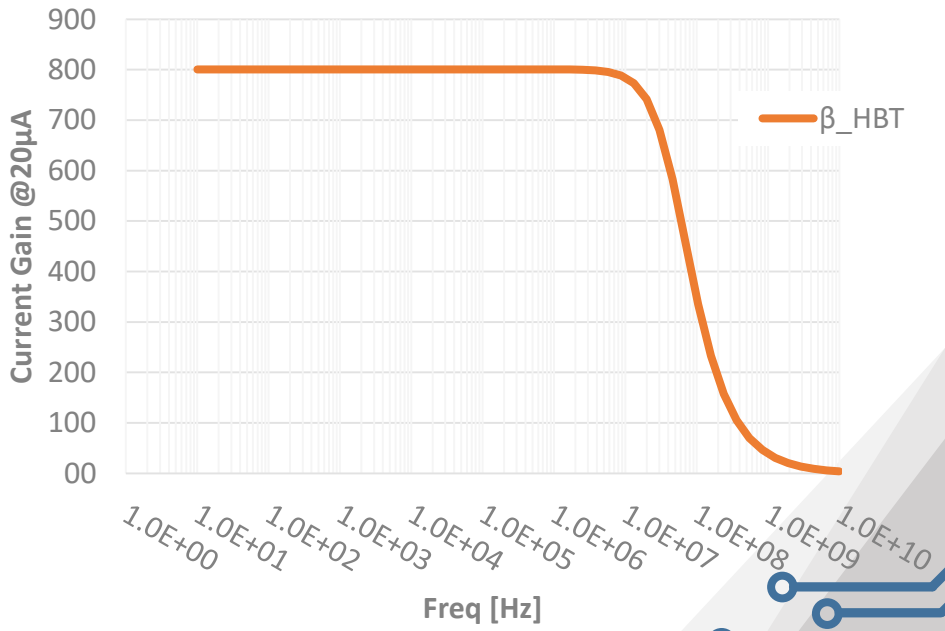
$\sim \frac{R_B}{\beta} \rightarrow$ minimize

Advantages of BiCMOS

- transit frequency f_T:
  - max. Freq. with $\beta = 1$
  - depending on current I_C
- power influences performance

Noise ⟷ Trade off ⟷ Power



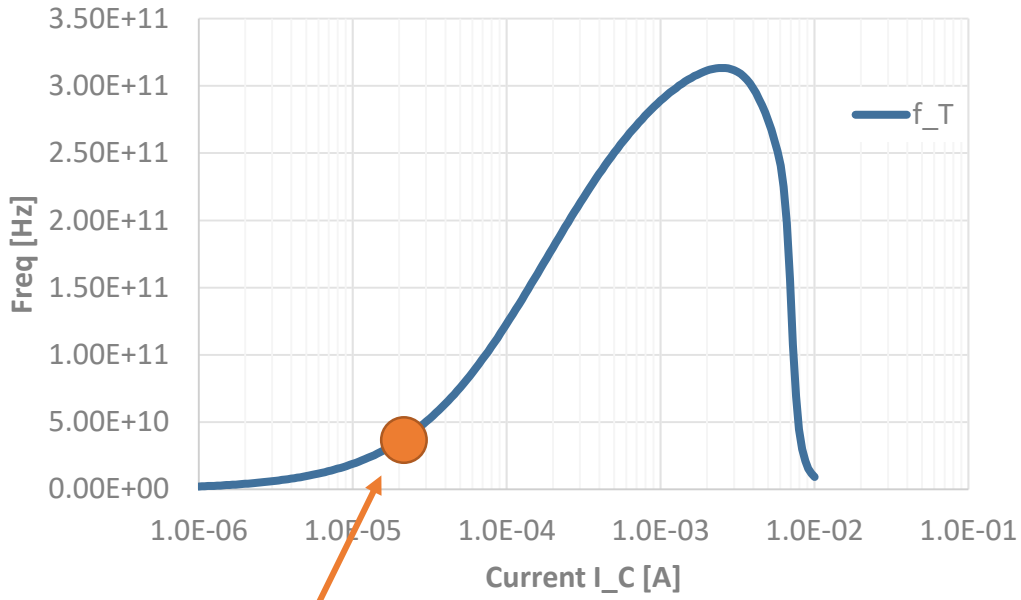


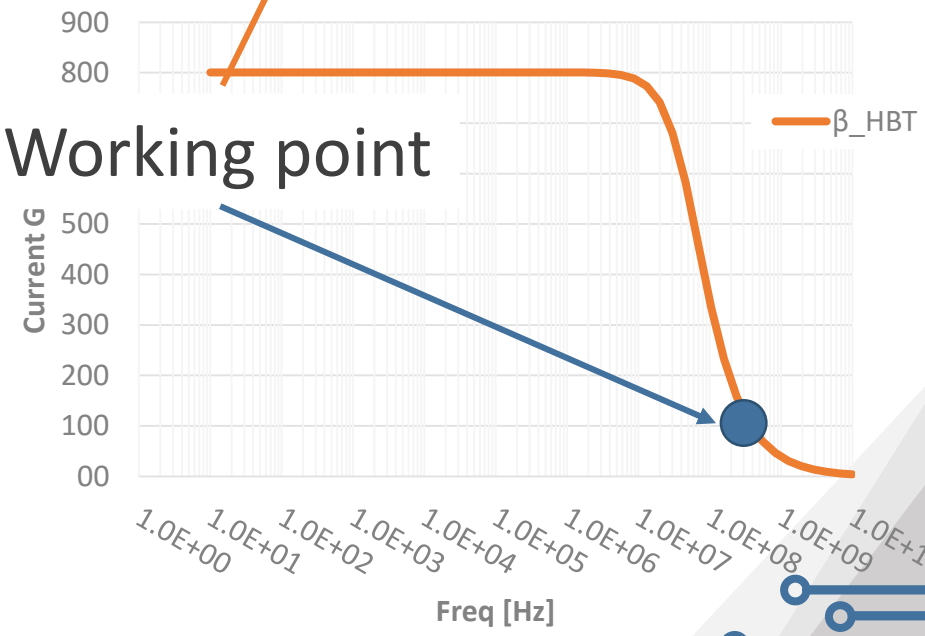
Advantages of BiCMOS

- transit frequency f_T:
  - max. Freq. with $\beta = 1$
  - depending on current I_C
- Power influences performance

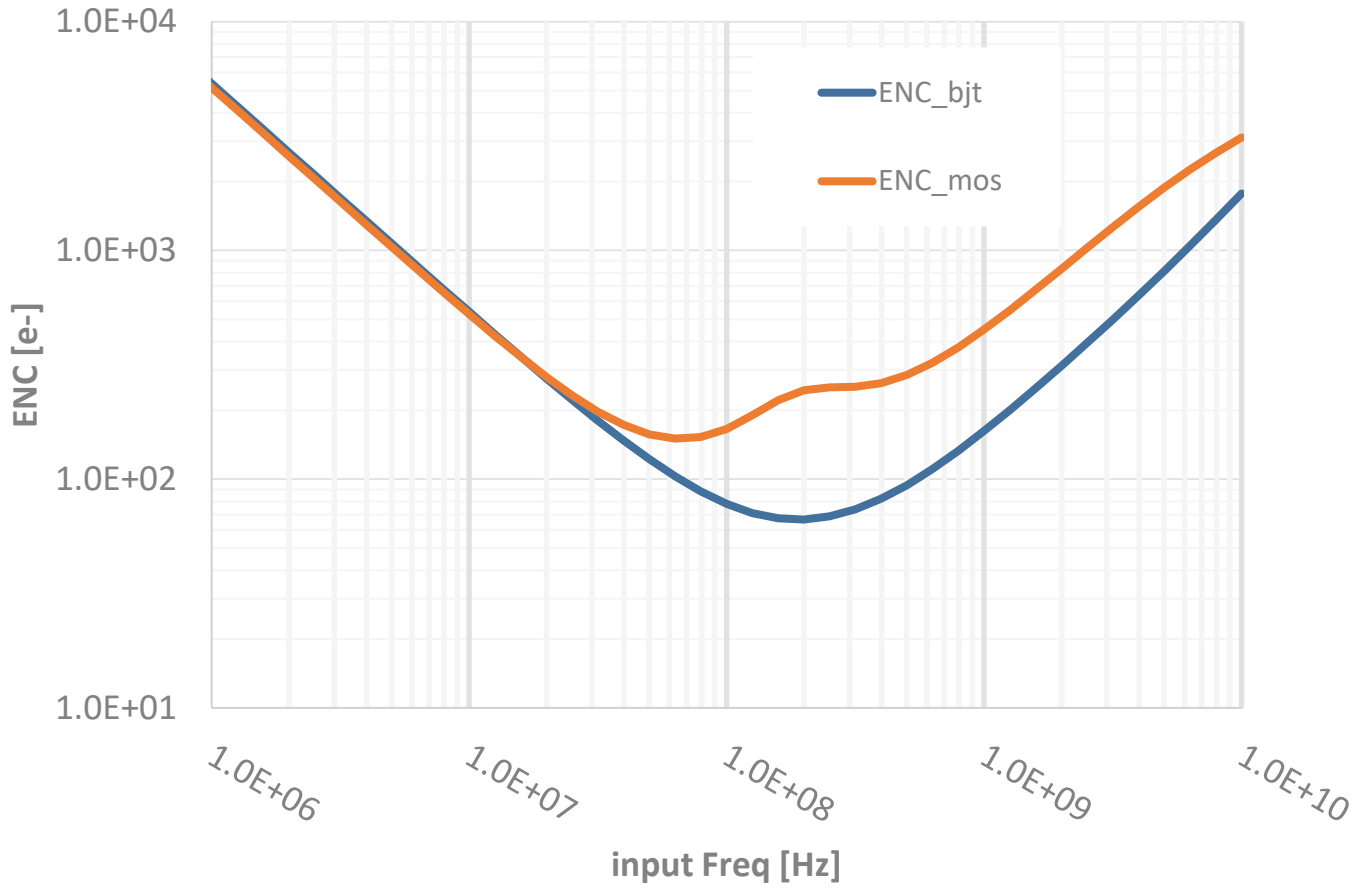
Noise ⟷ Trade off ⟷ Power

Single pre-amplifier with fast rising edge, low noise and low power consumption

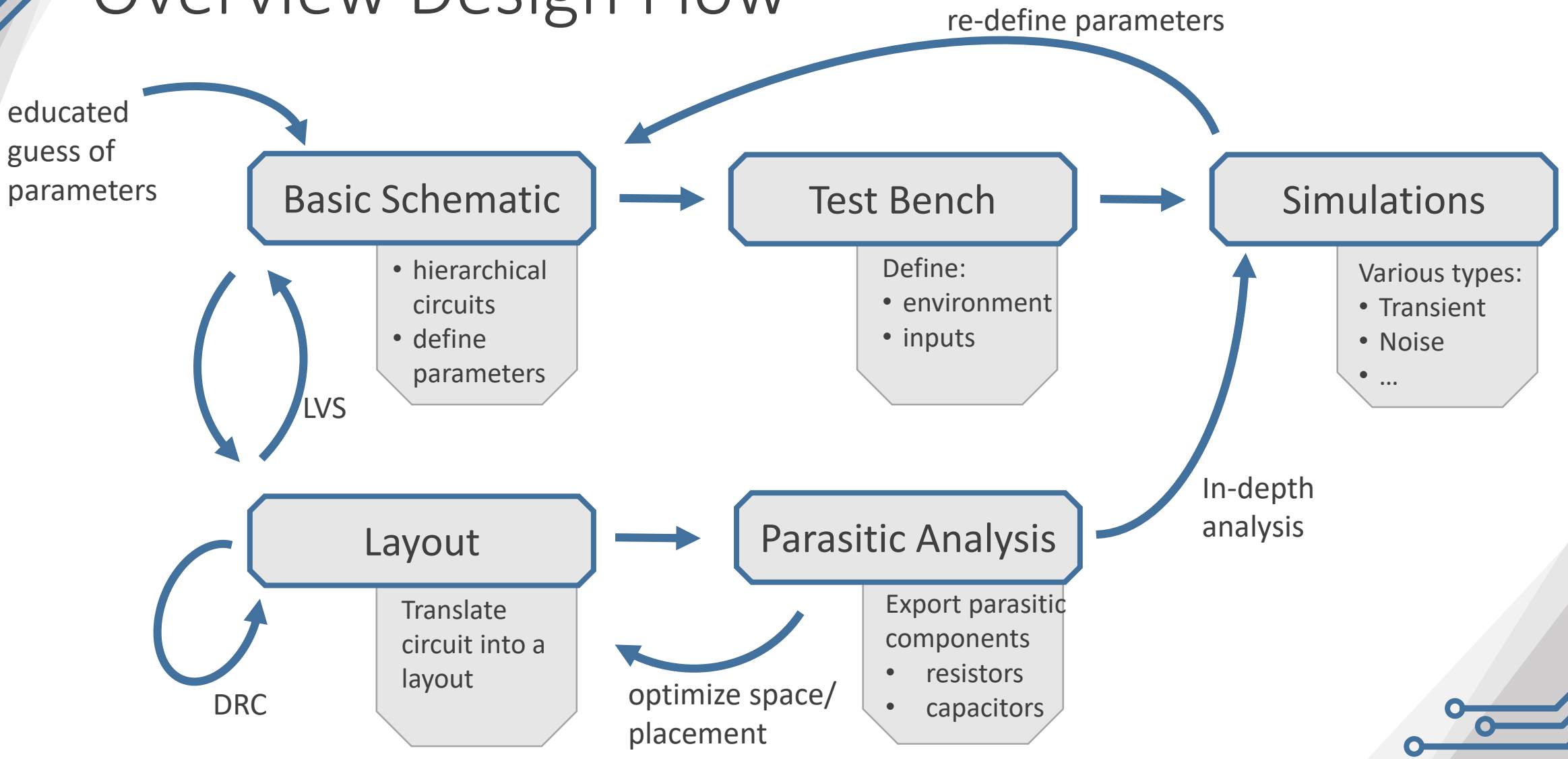




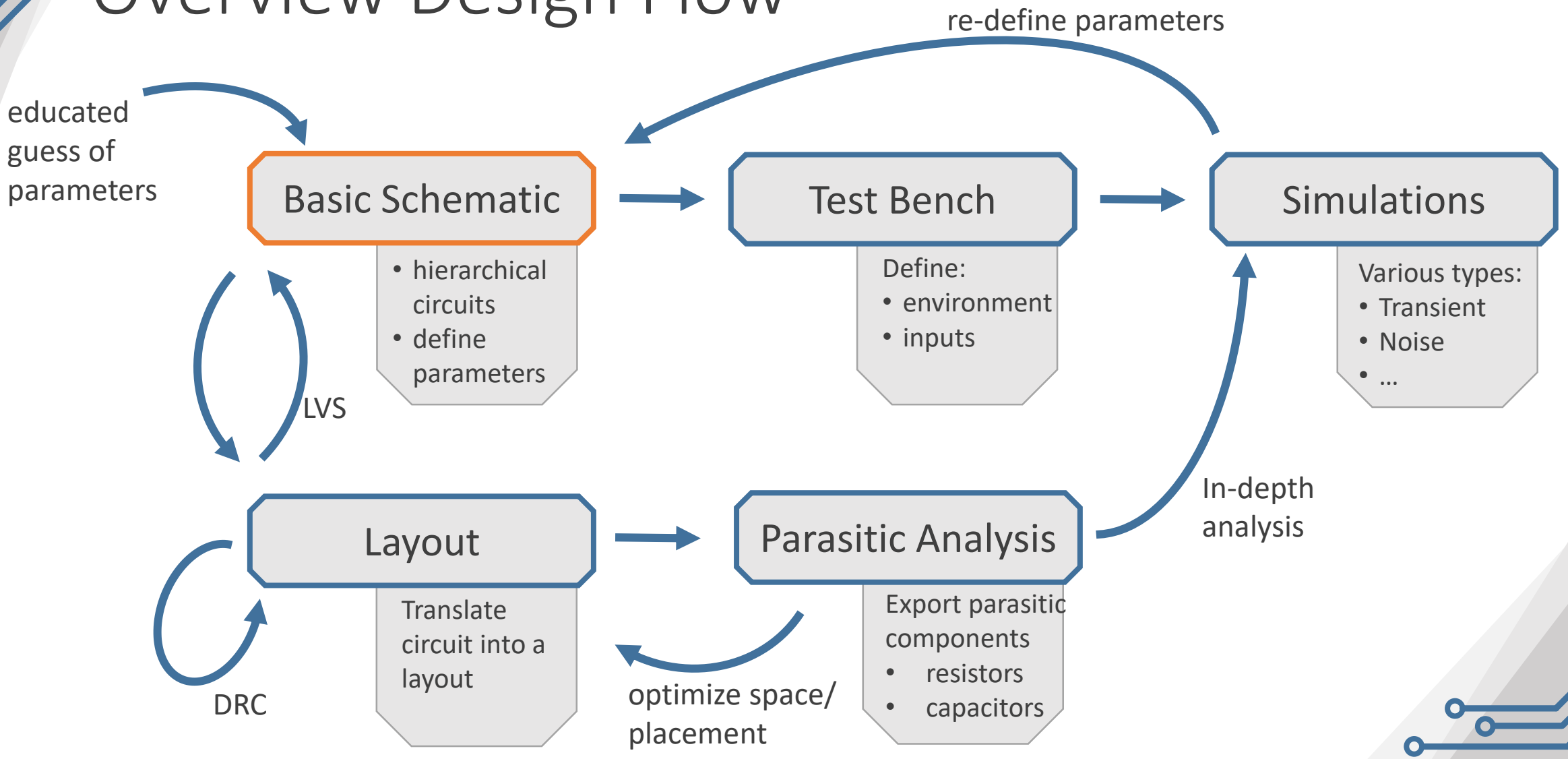
Advantages of BiCMOS



Overview Design Flow



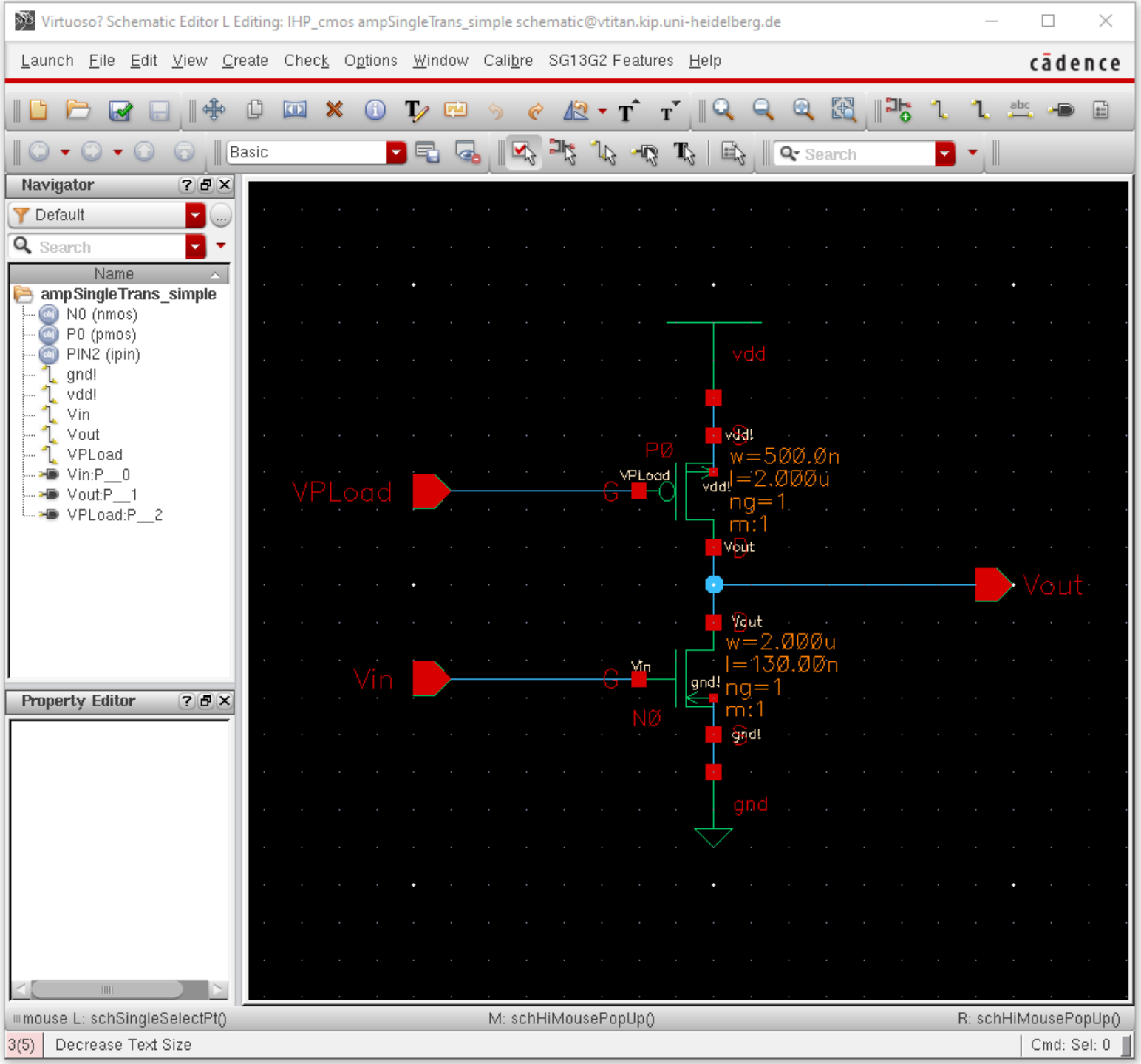
Overview Design Flow



Schematic Editor

simple gain stage:

- pmos current source
- nmos input transistor/ switch



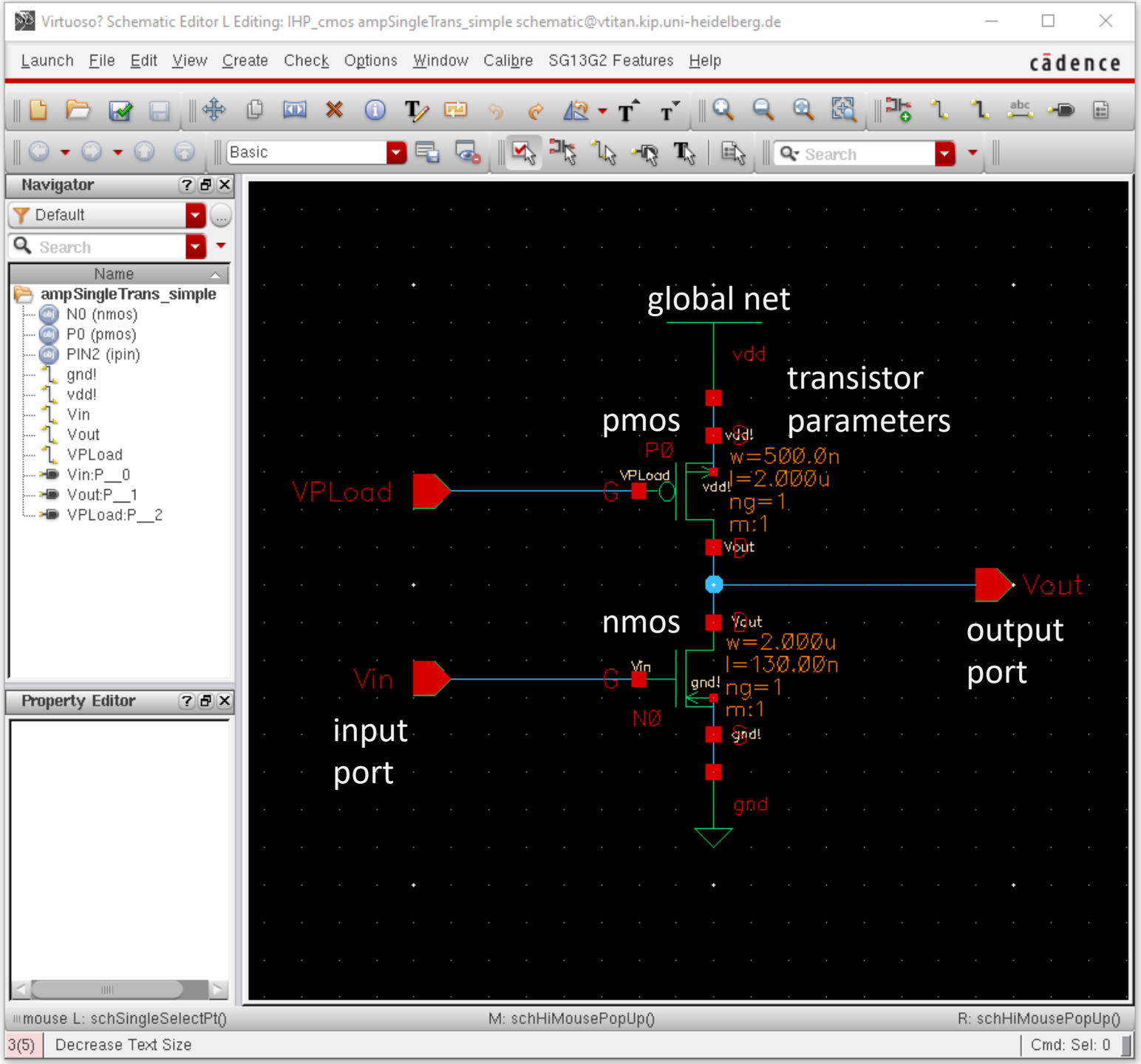
Schematic Editor

simple gain stage:

- pmos current source
- nmos input transistor/ switch

circuit parameter:

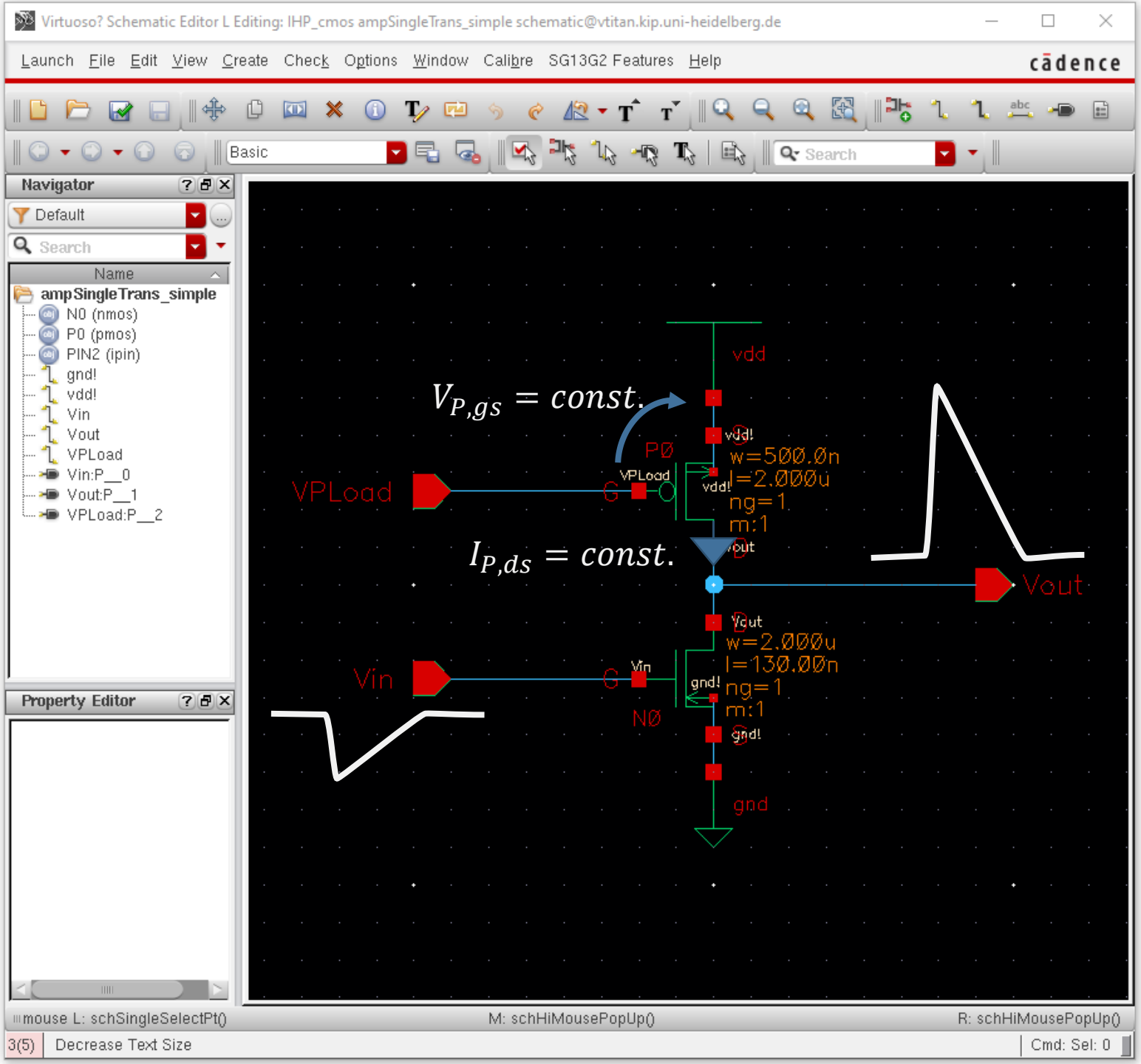
- transistor width/ length
- bias voltages



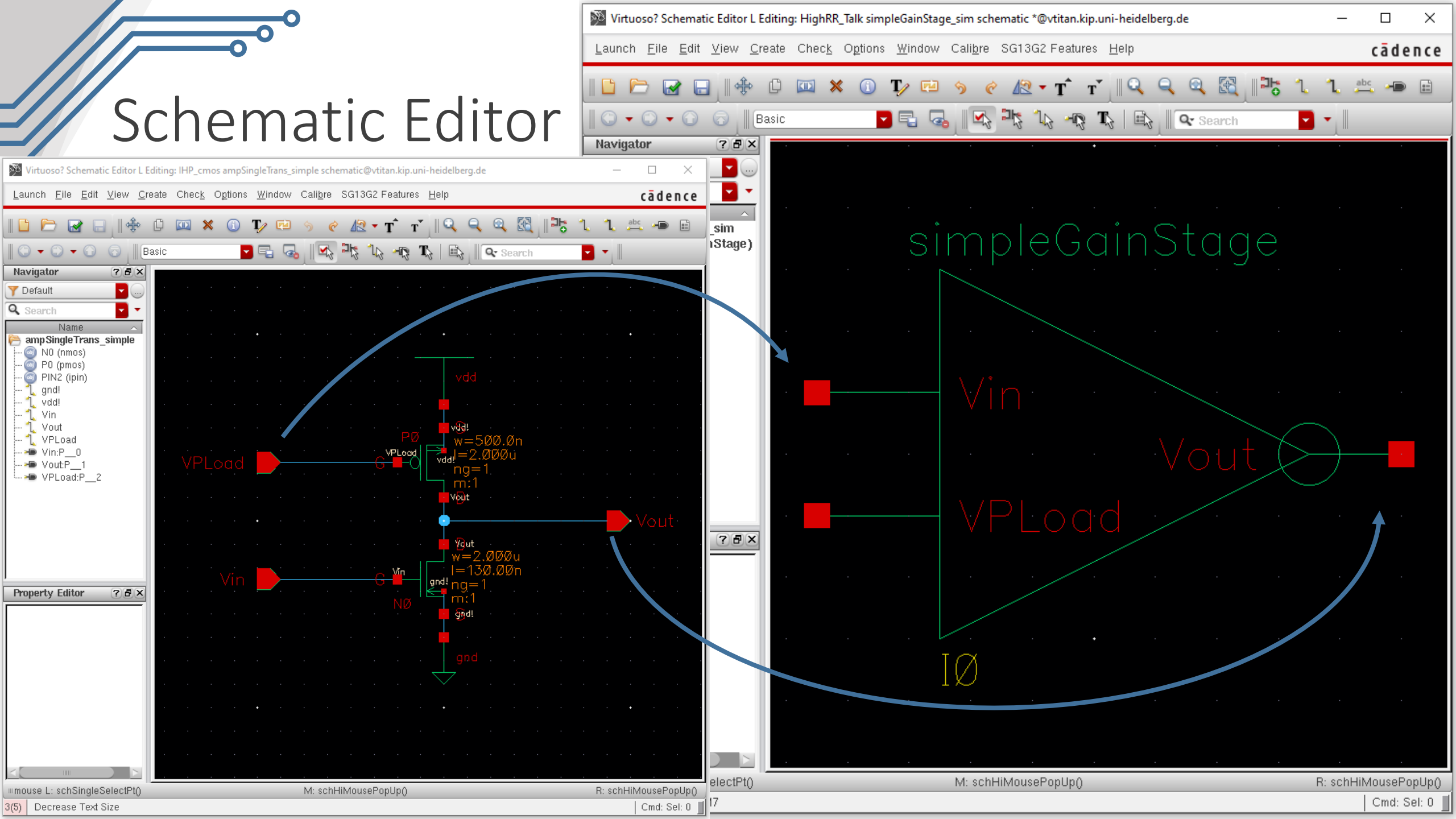
Schematic Editor

simple gain stage:

- pmos current source
- nmos input transistor/ switch
  - $V_{N,gs} \rightarrow vdd \implies$
    $I_{N,ds} \rightarrow I_{sat}$
  - $V_{N,gs} \rightarrow 0 \implies$
    $I_{N,ds} \rightarrow 0$

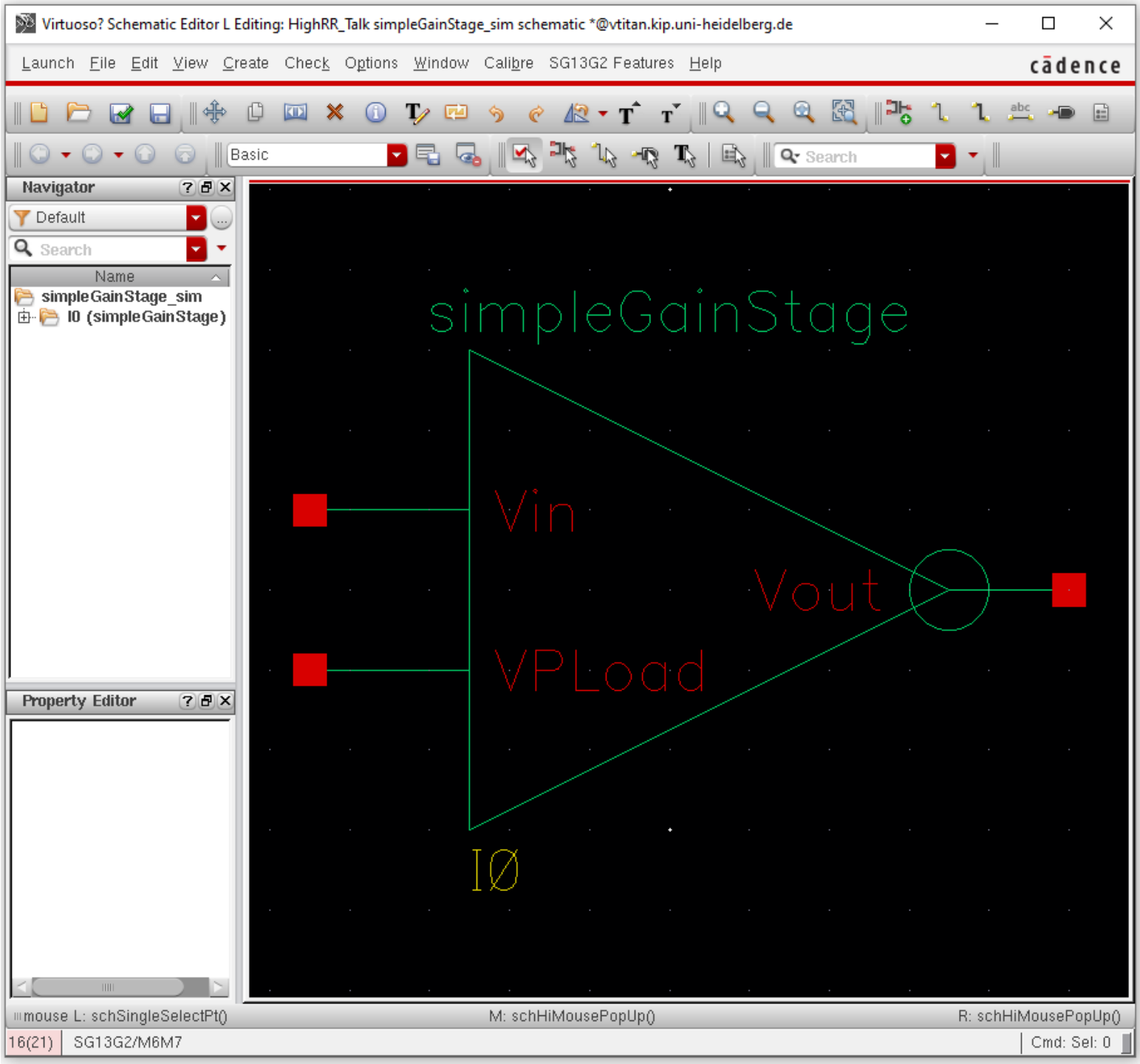


Schematic Editor



Schematic Editor

- hierarchical structure
  - circuits are divided into smaller blocks
  - ports are used to interconnect nets
  - transistors are also just symbols



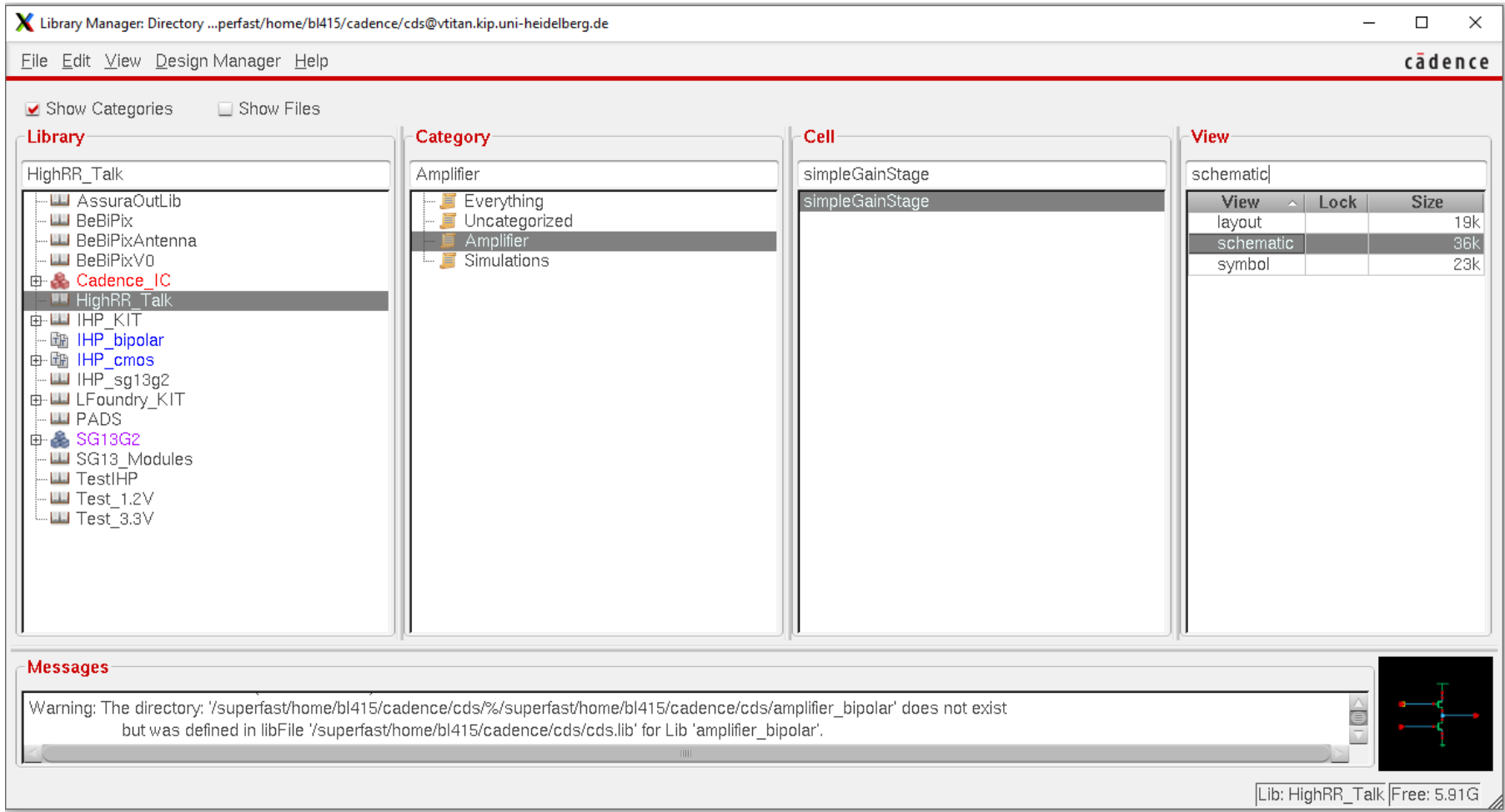
Schematic Editor

Library

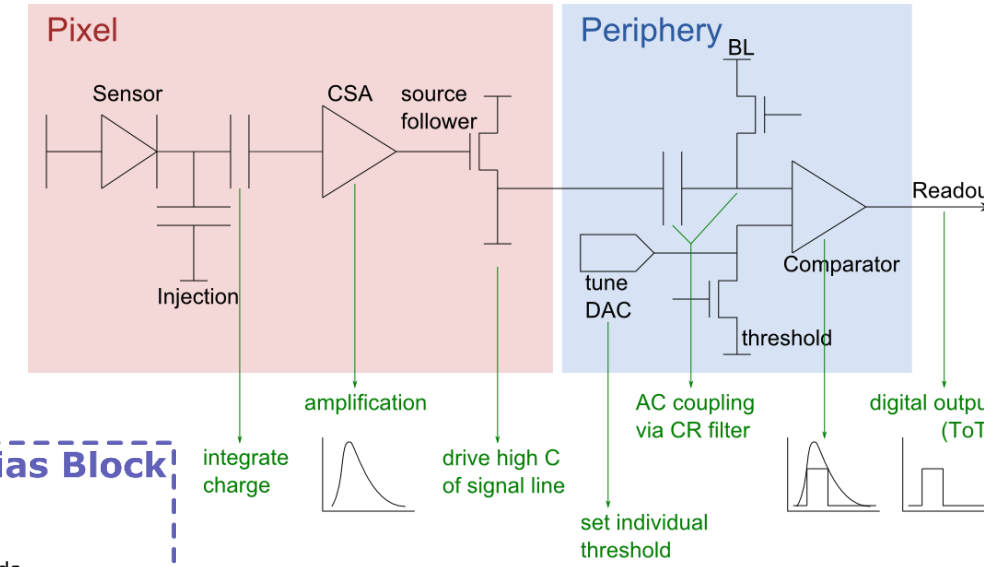
Cell

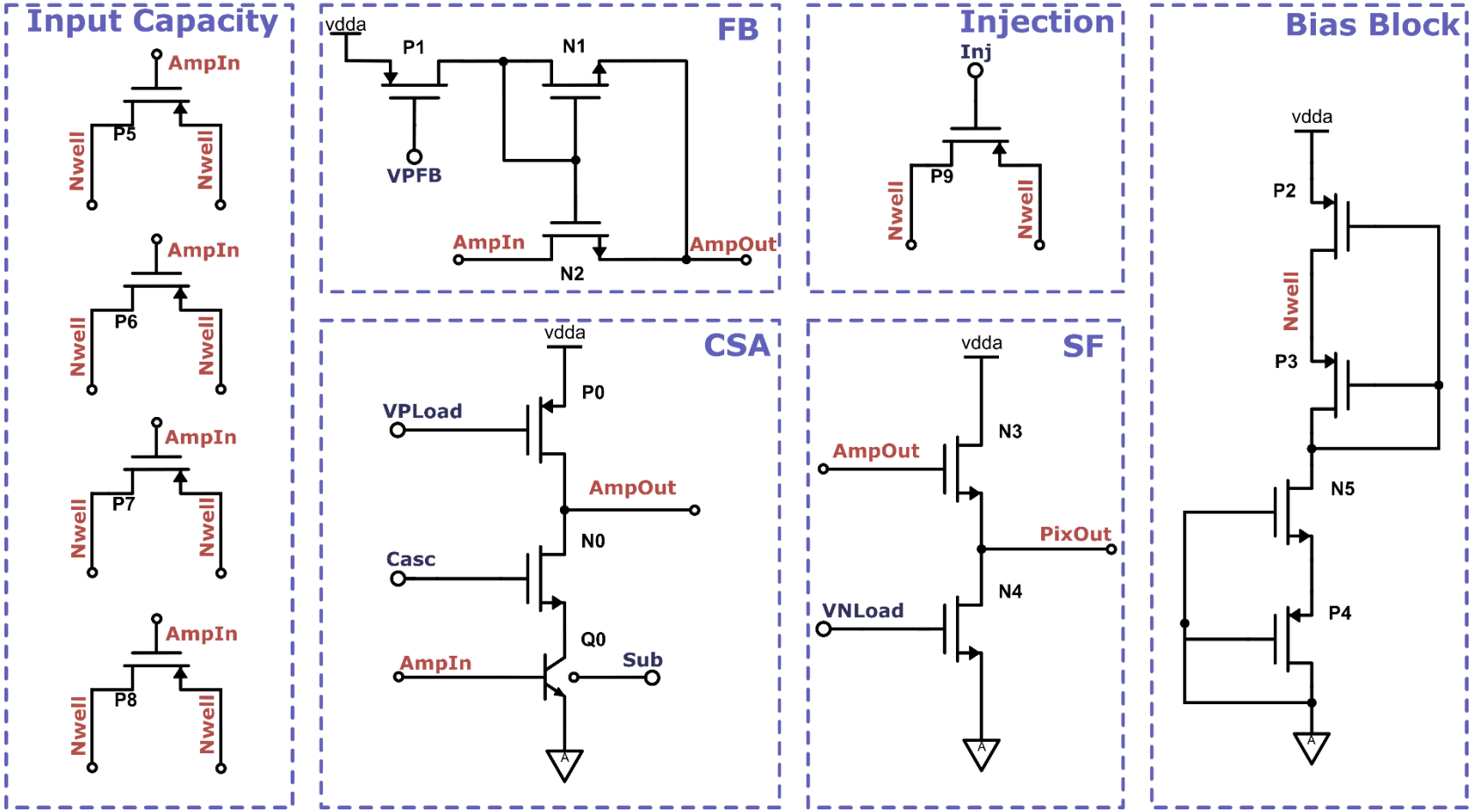
view

- schematic
- layout
- simulation
- …

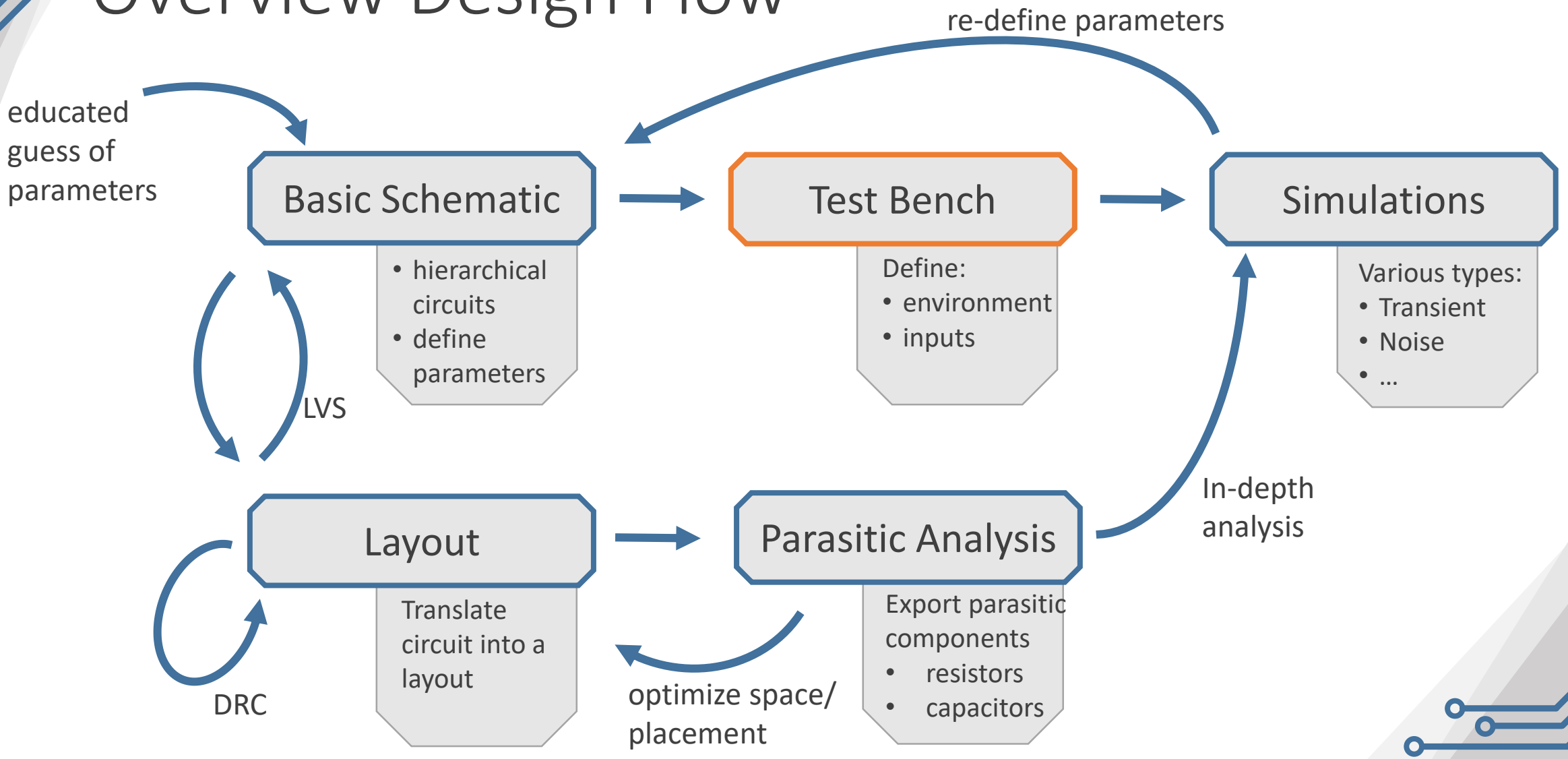


BeBiPix Pixel Schematics





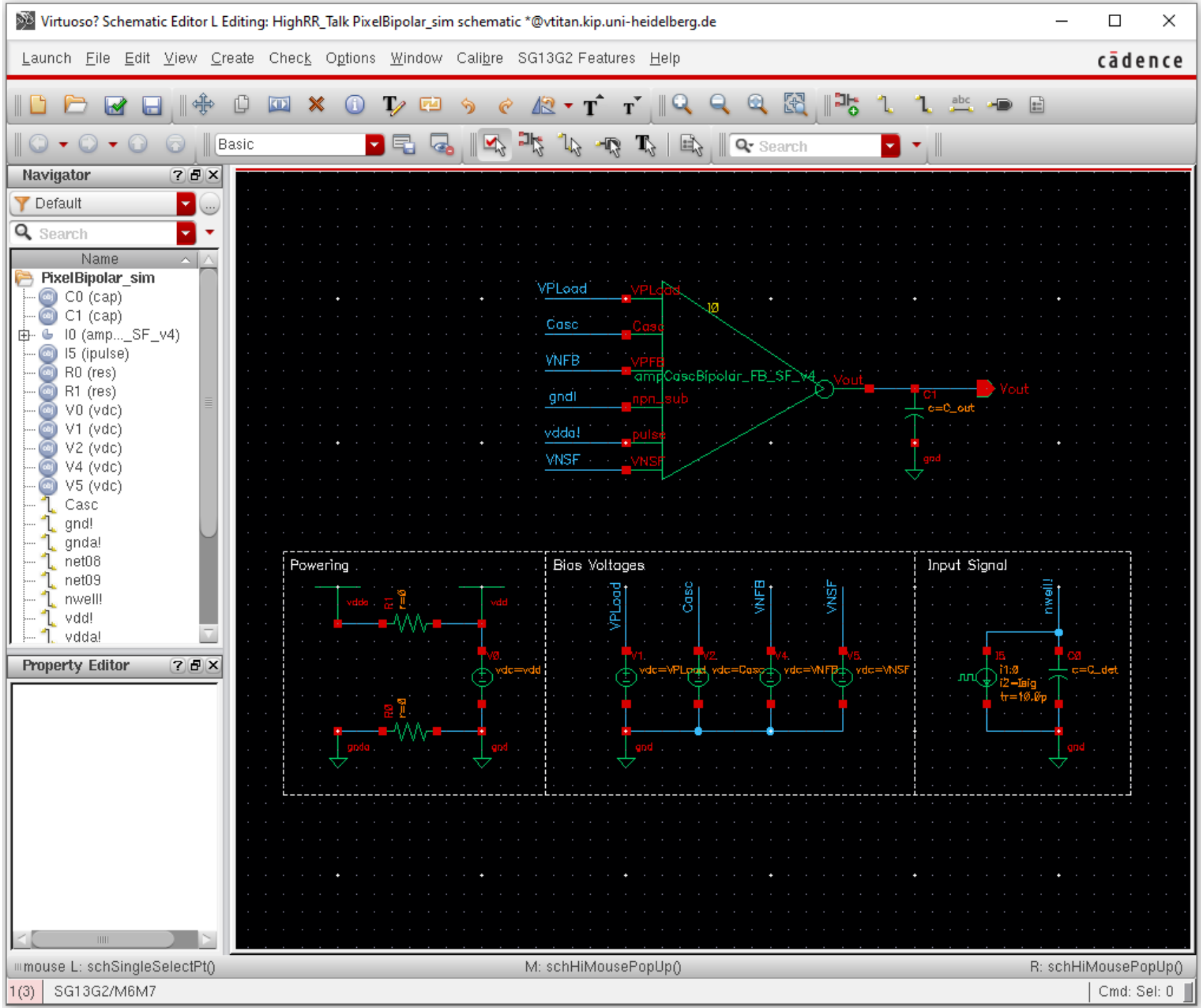
Overview Design Flow



Test Bench

define environment:

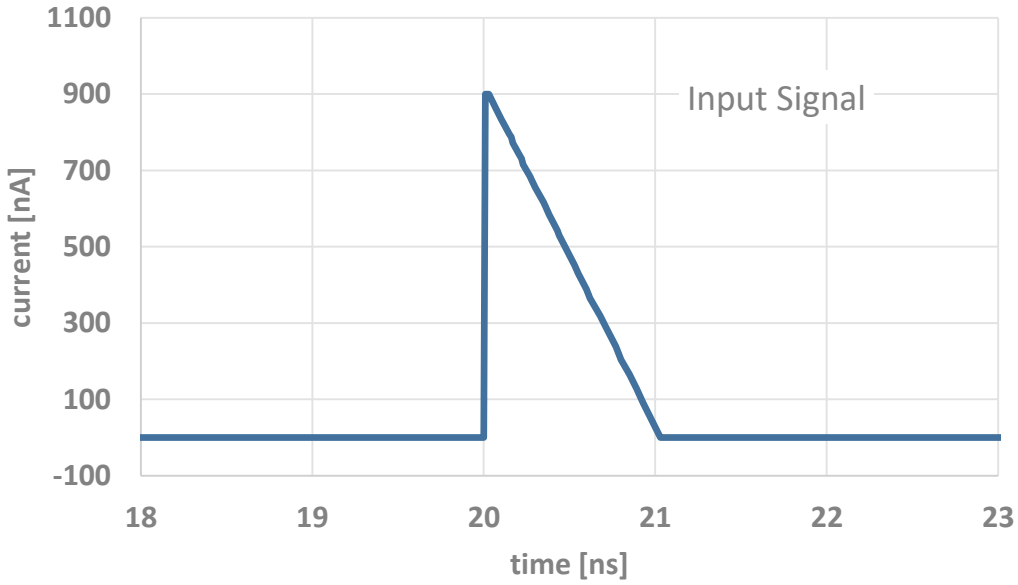
- ideal current/ voltage sources
- use variables
- detector capacity: $C_{det} = 100fF$
- load capacity: $C_{load} = 10fF \rightarrow$ (large transistor gate)



Test Bench

input signal:

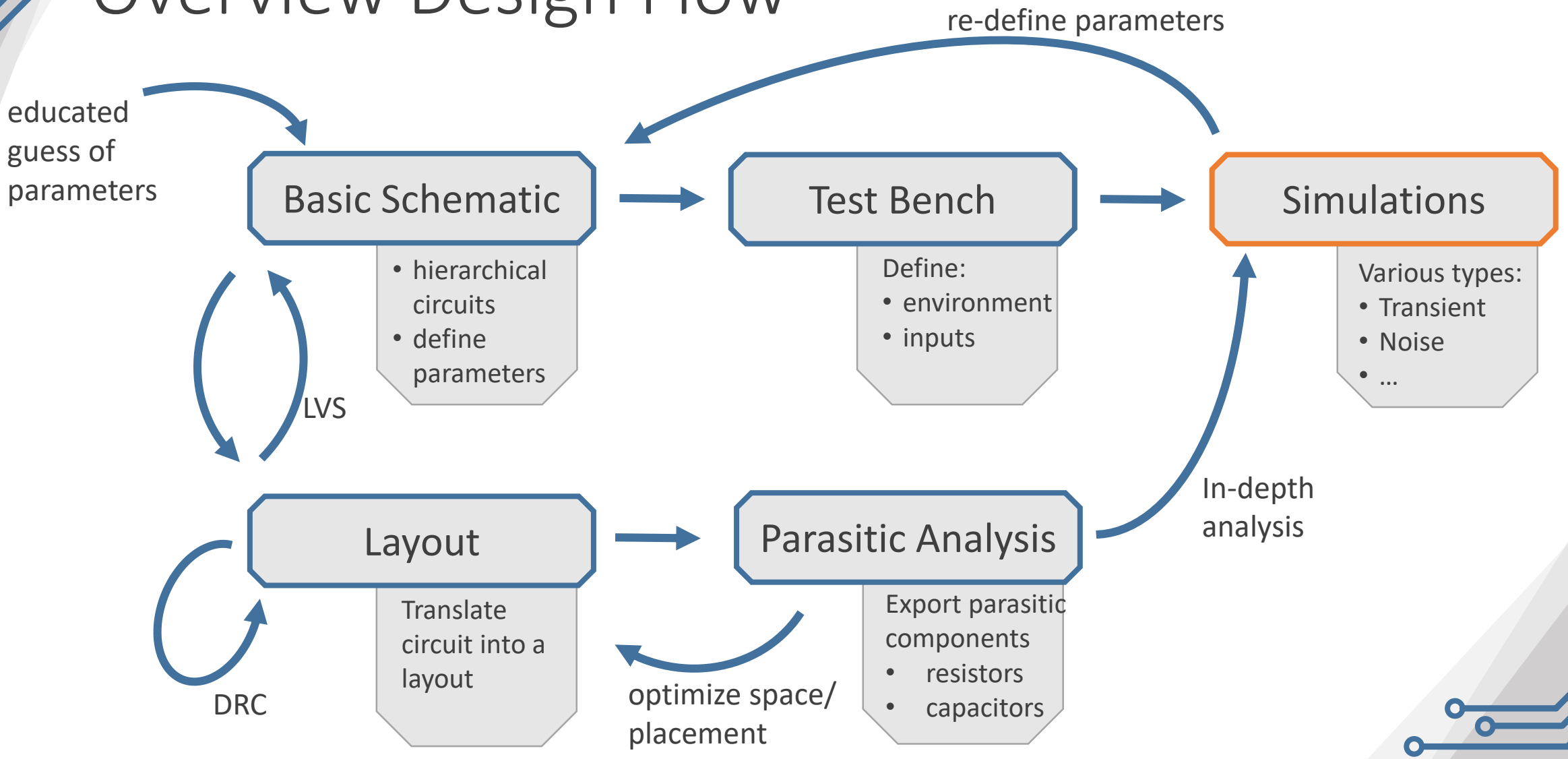
- corresponding to a MIP
- Parameter:
  - $Q_{sig} \approx 0.45fC \approx 2800\, e^-$
  - $t_{rise} = 10ps, t_{fall} = 1ns$



power specification:

- limit power consumption to $\sim 20\mu A$

Overview Design Flow

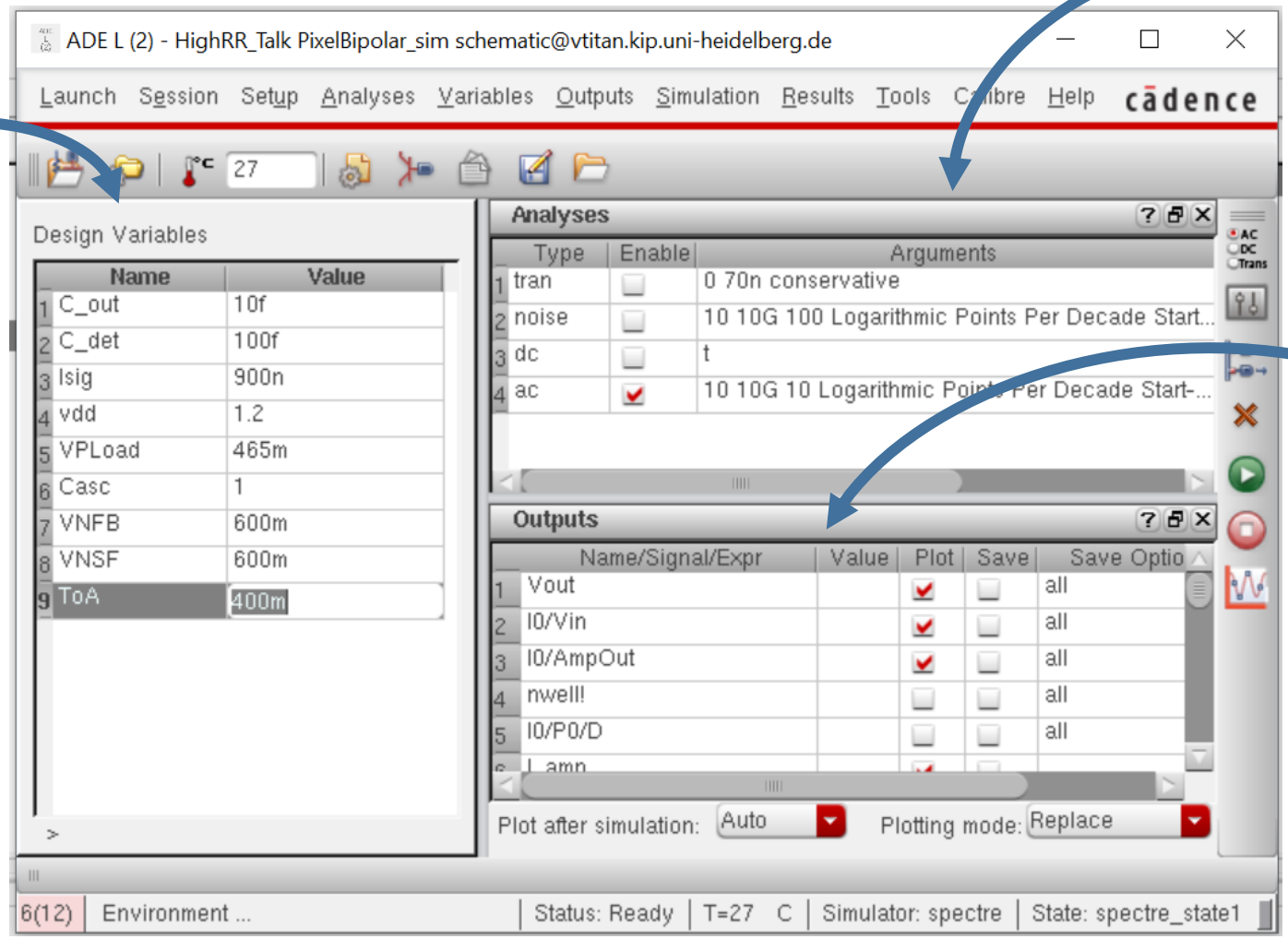


Simulations

define **type of simulation**

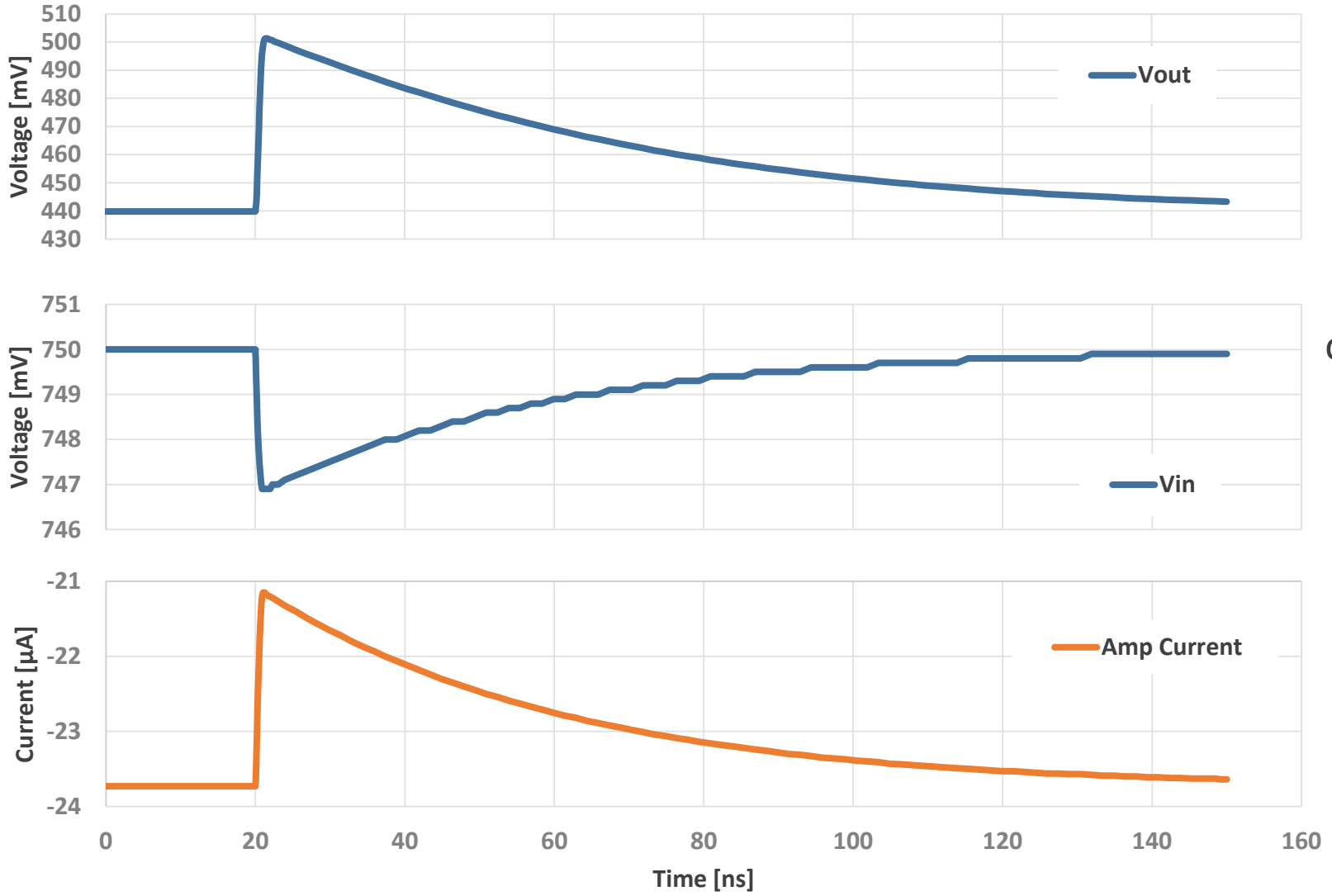
define **variables** from the test bench – also useful to simulate circuit parameters

select **outputs** or define **expressions**



Transient Simulation

shows circuit response to an input signal:

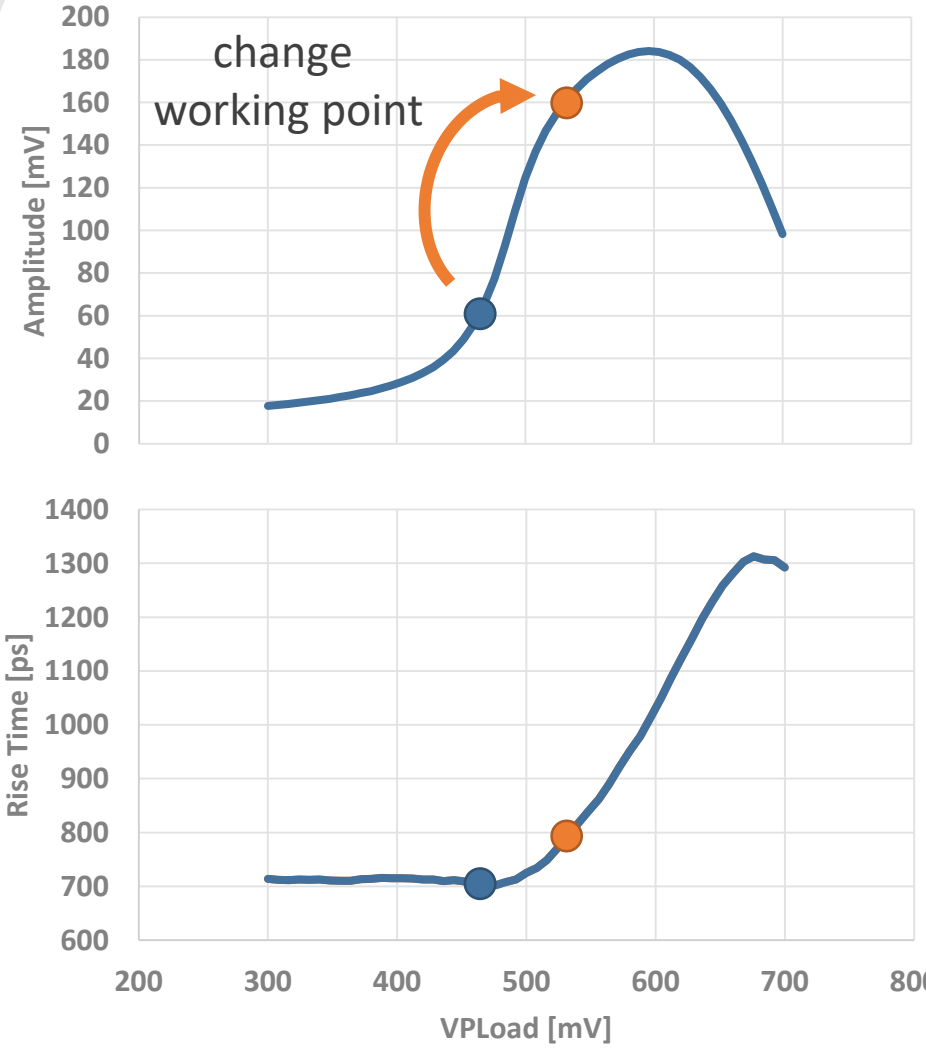


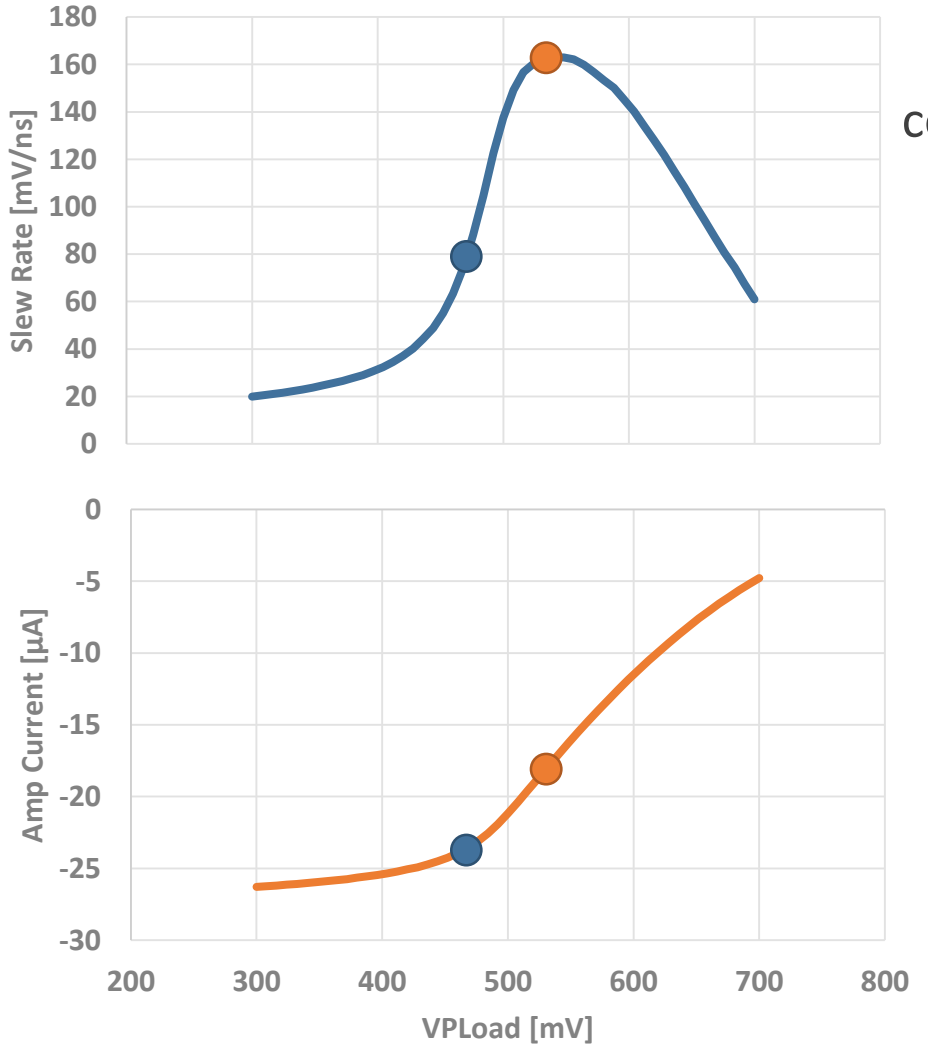
signal results in a $\sim 60mV$ voltage peak at the output

current signal defined in test bench results in a $\sim 3mV$ voltage drop at the input

amplifier current is not constant but only varies a few μA

Transient Simulation – Parametric Sweep

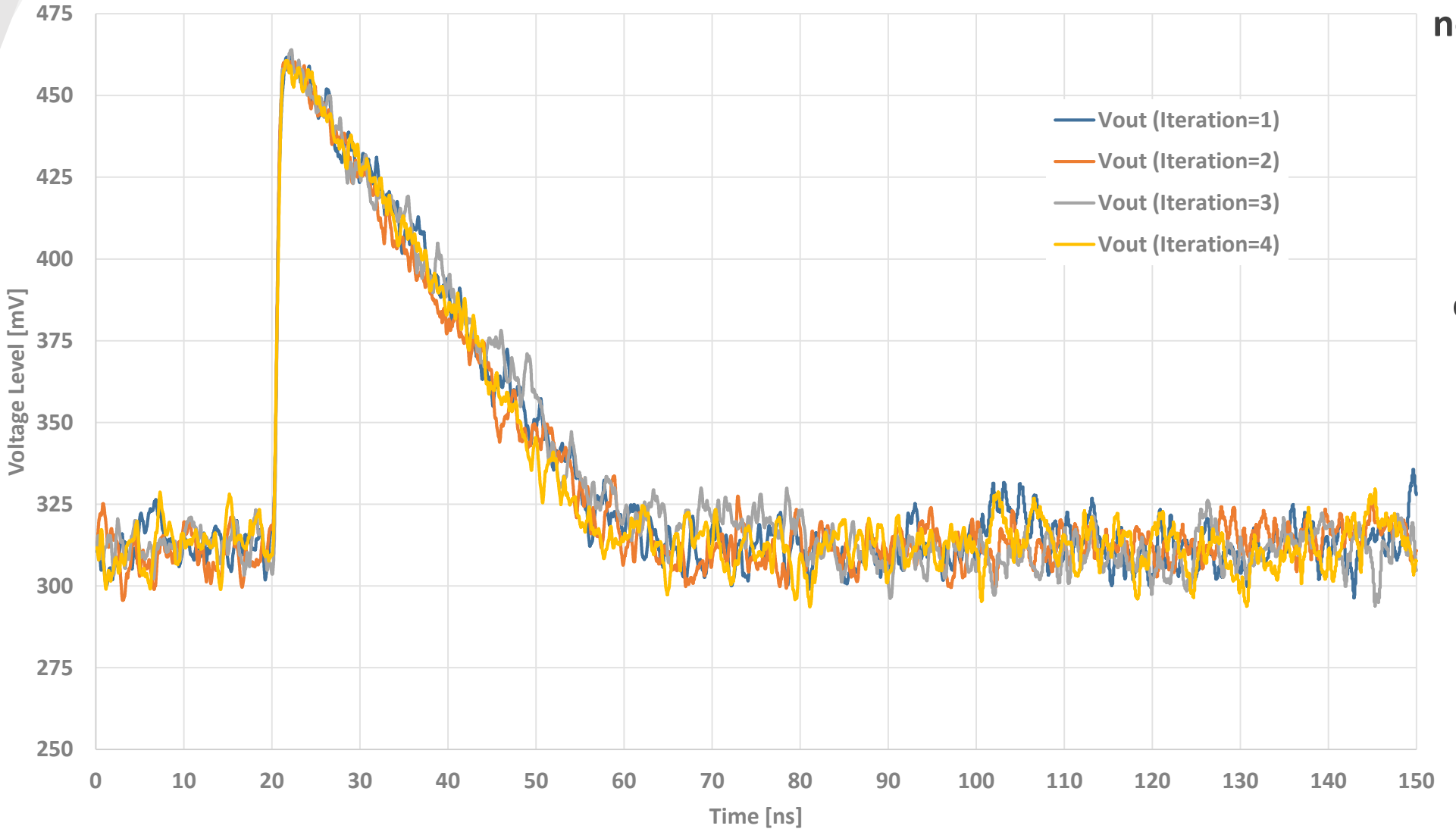




useful to find good operation points:

combine with expressions to observe important parameter

Transient Simulation – influence of noise

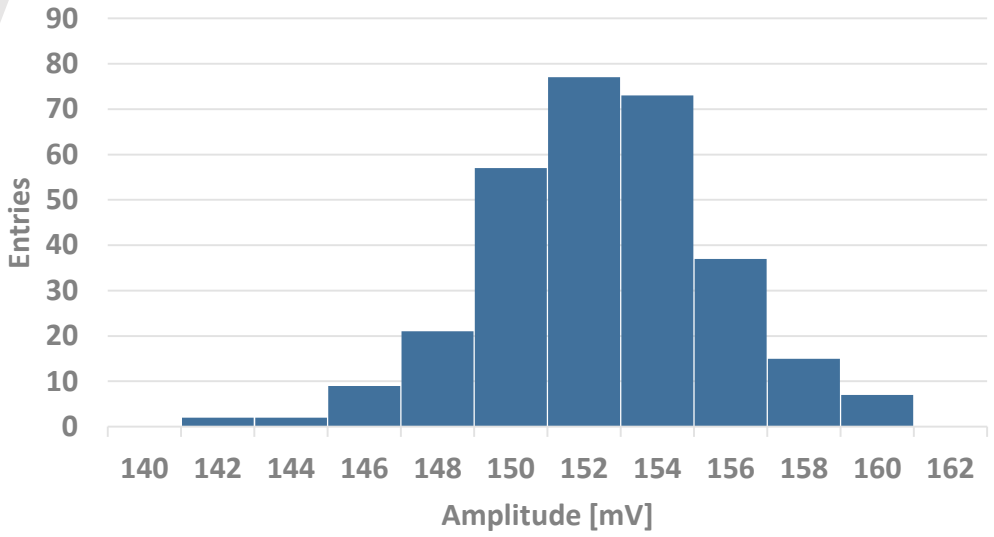


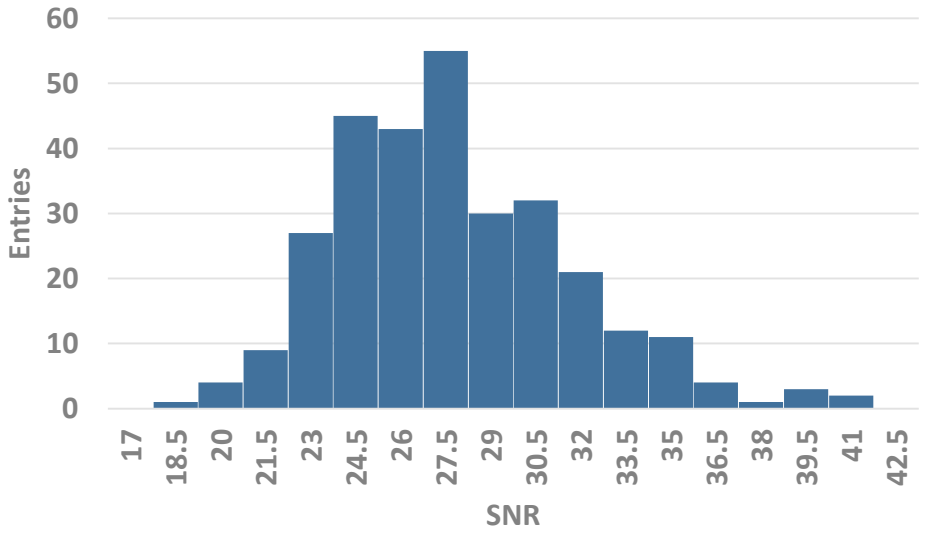
possibility to introduce noise into the simulation:

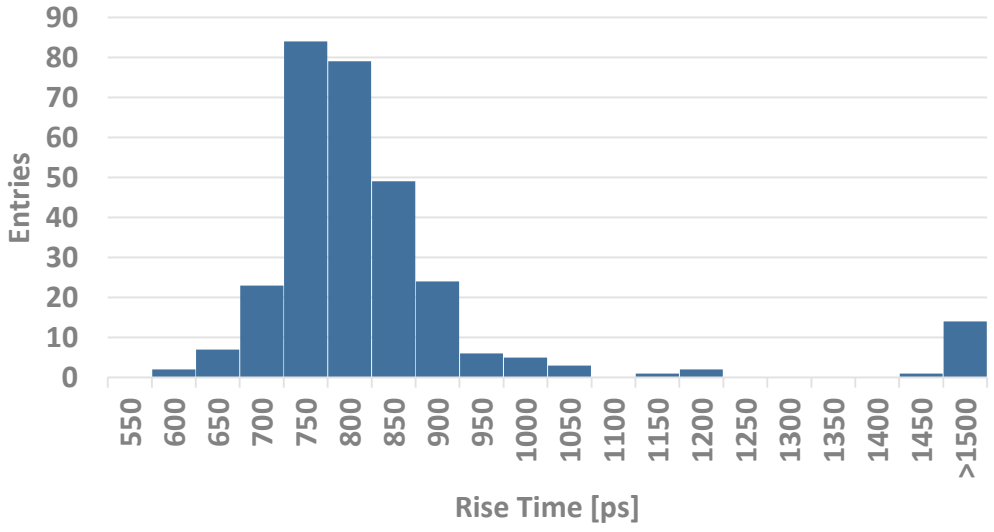
requires significantly more time

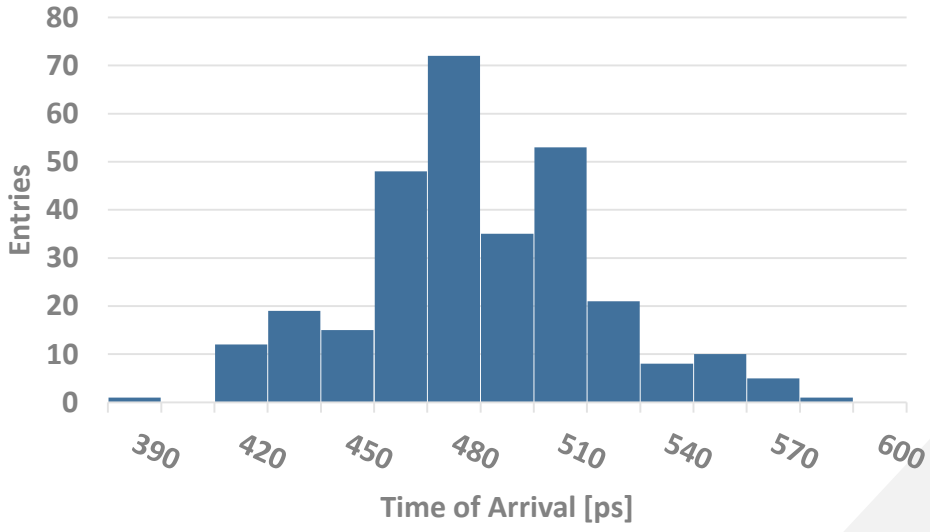
opens up the possibility to investigate various important parameters

Transient Simulation – influence of noise









Noise Simulation

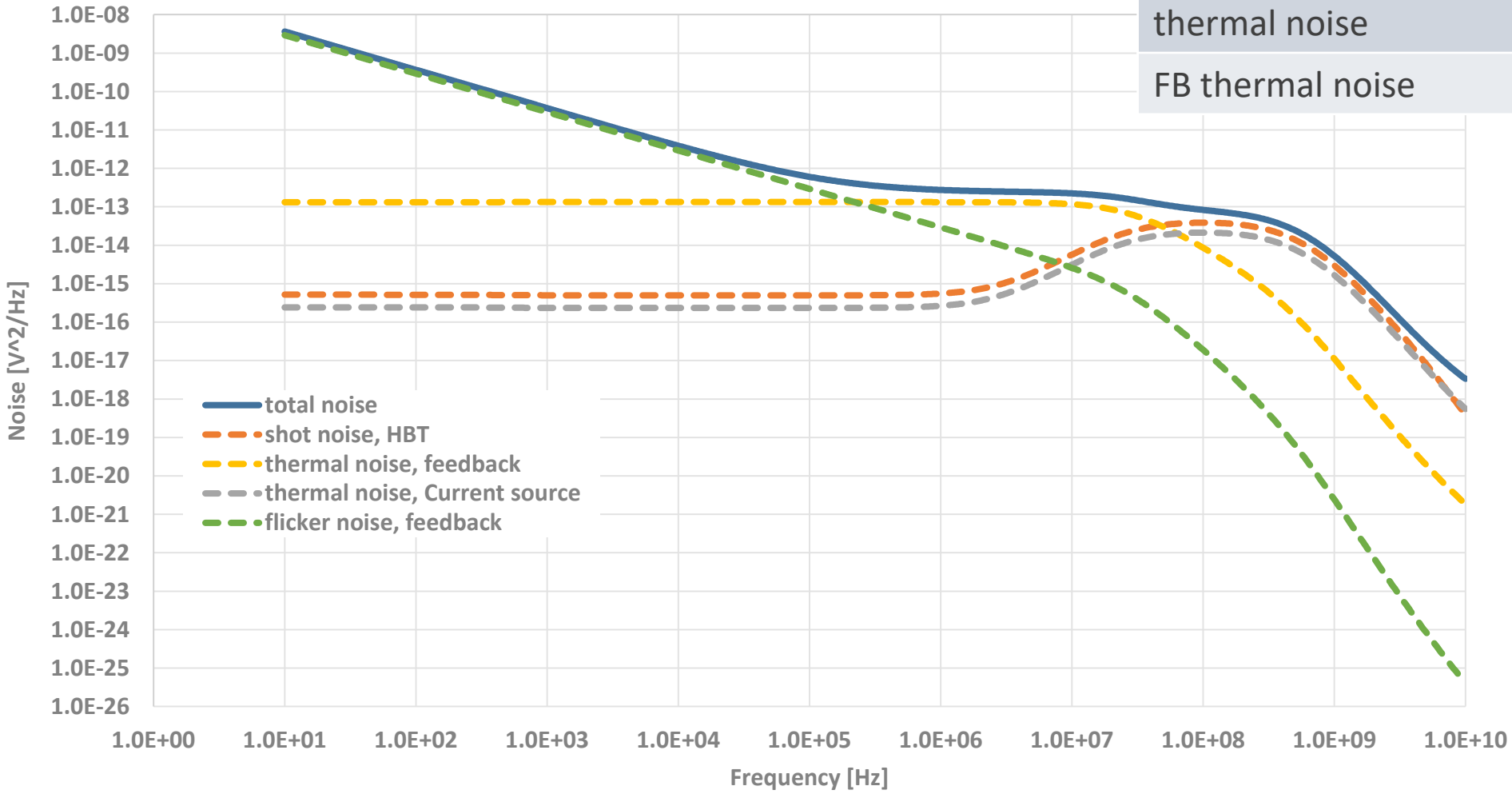
- transient simulation with noise is slow

→ dedicated noise simulation

- gives access to several different noise types for each part
- indicate larges noise contributors

Noise Simulation

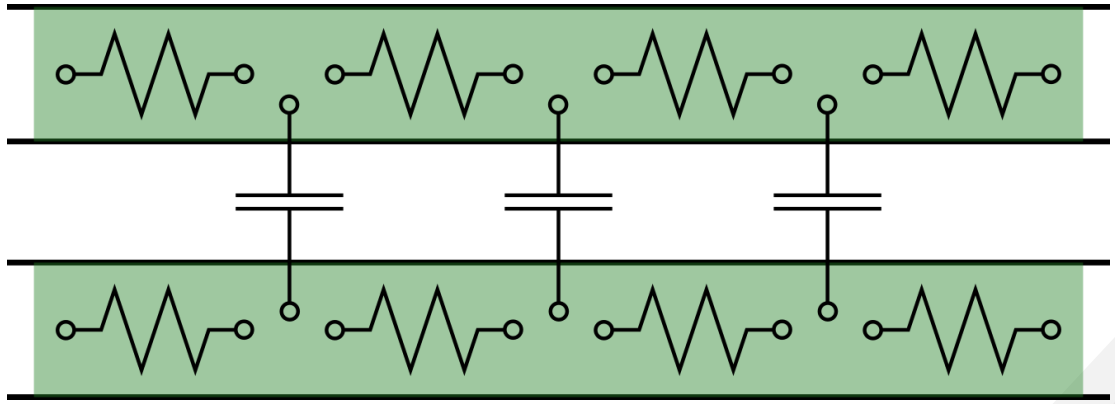
noise type	integrated noise
Total noise	$6.47\ mV$
HBT shot noise	$4.26\ mV$
Current source thermal noise	$3.18\ mV$
FB thermal noise	$2.30\ mV$



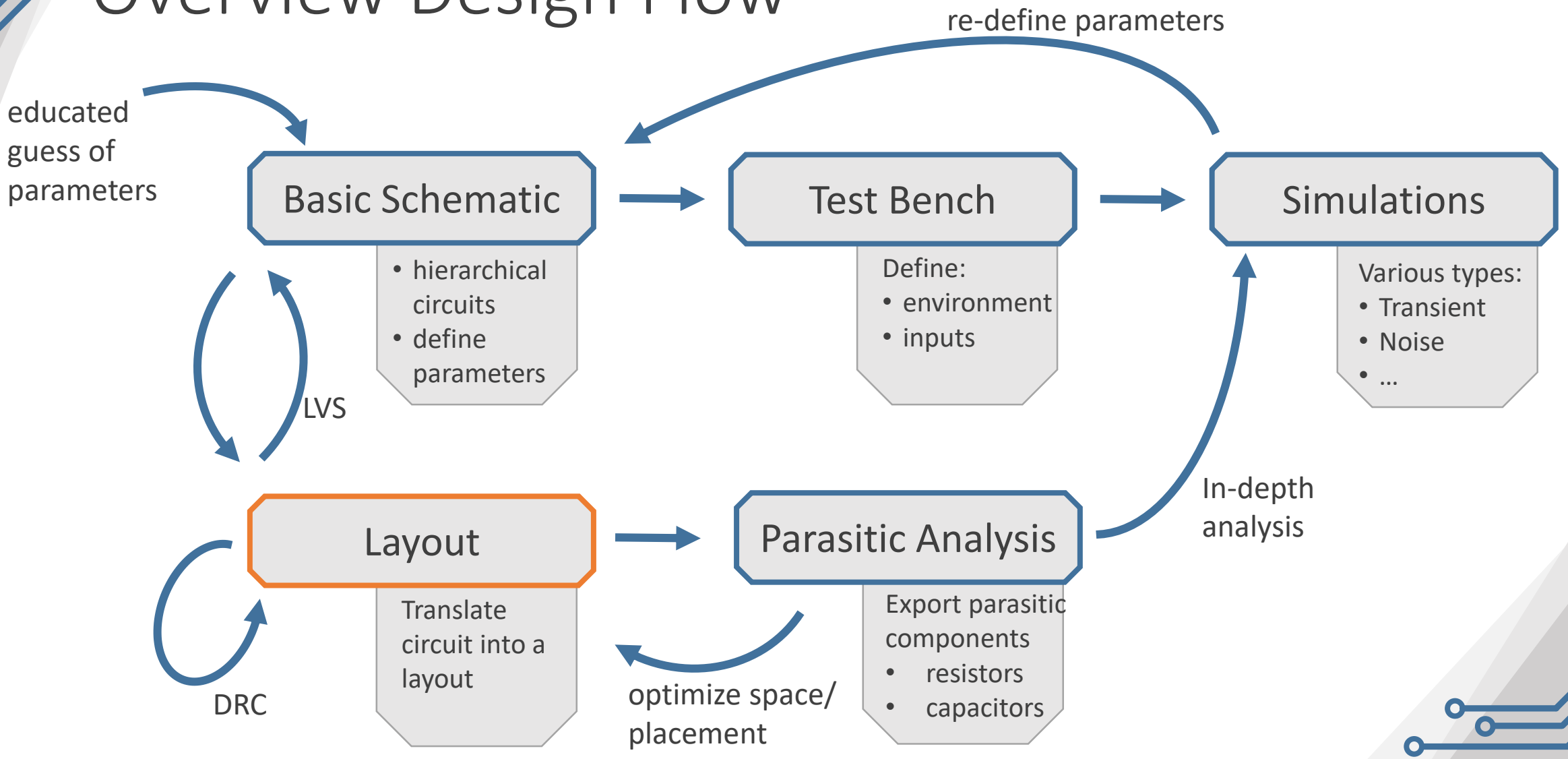
Parasitic Simulations

- till now: only transistor models are simulated
  - including internal capacities
- for the physical representation of the circuit non-ideal traces are needed
  - add parasitic resistance/ capacities
  - degrade circuit performance

→ layout is required

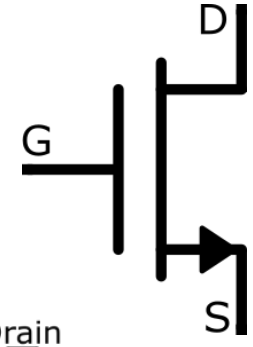


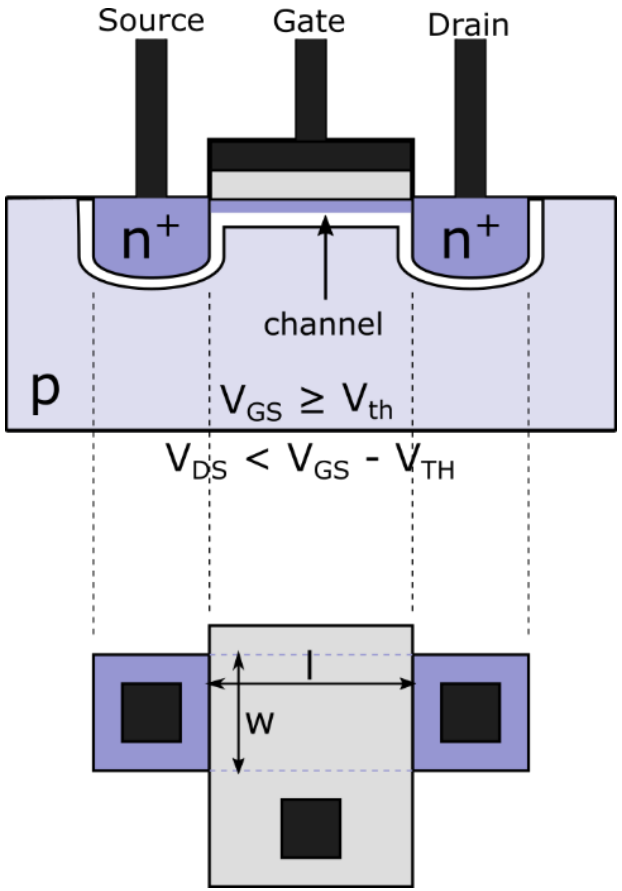
Overview Design Flow



NMOS

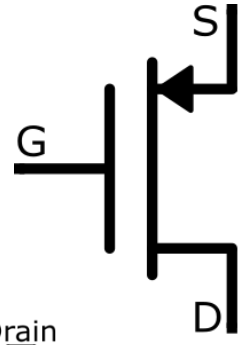
N-channel device

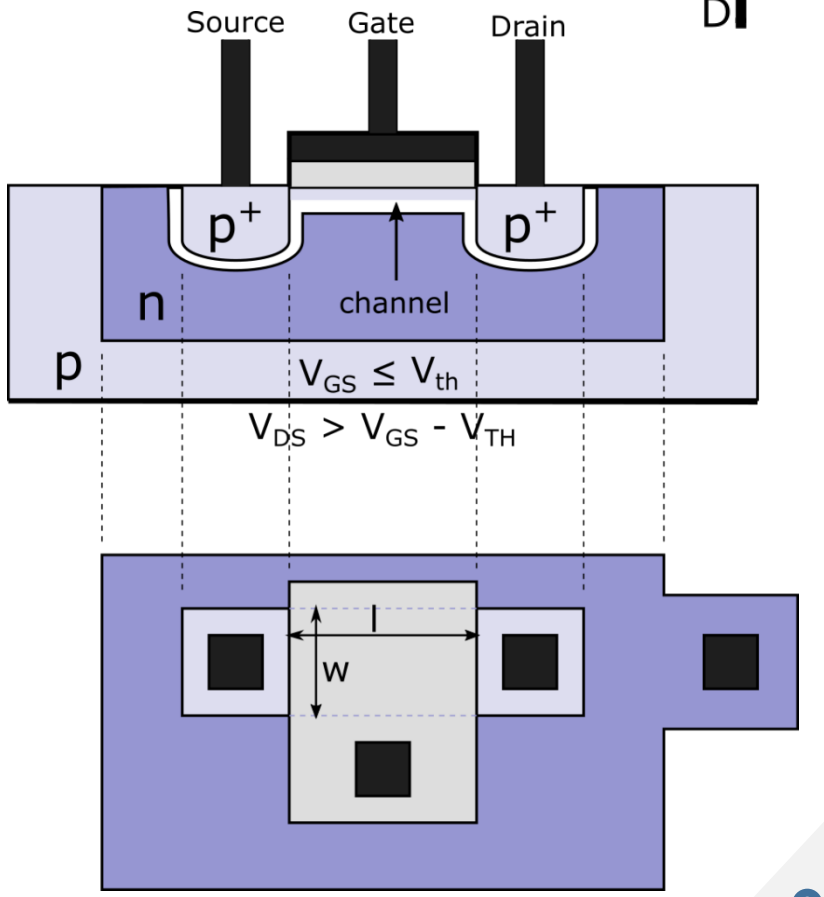




PMOS

P-channel device





Layout

- layers define physical layers on chip
  - shapes in  define n-doped area
- possible to use std. cells for transistors, …


n-well


p-well


buried n-well

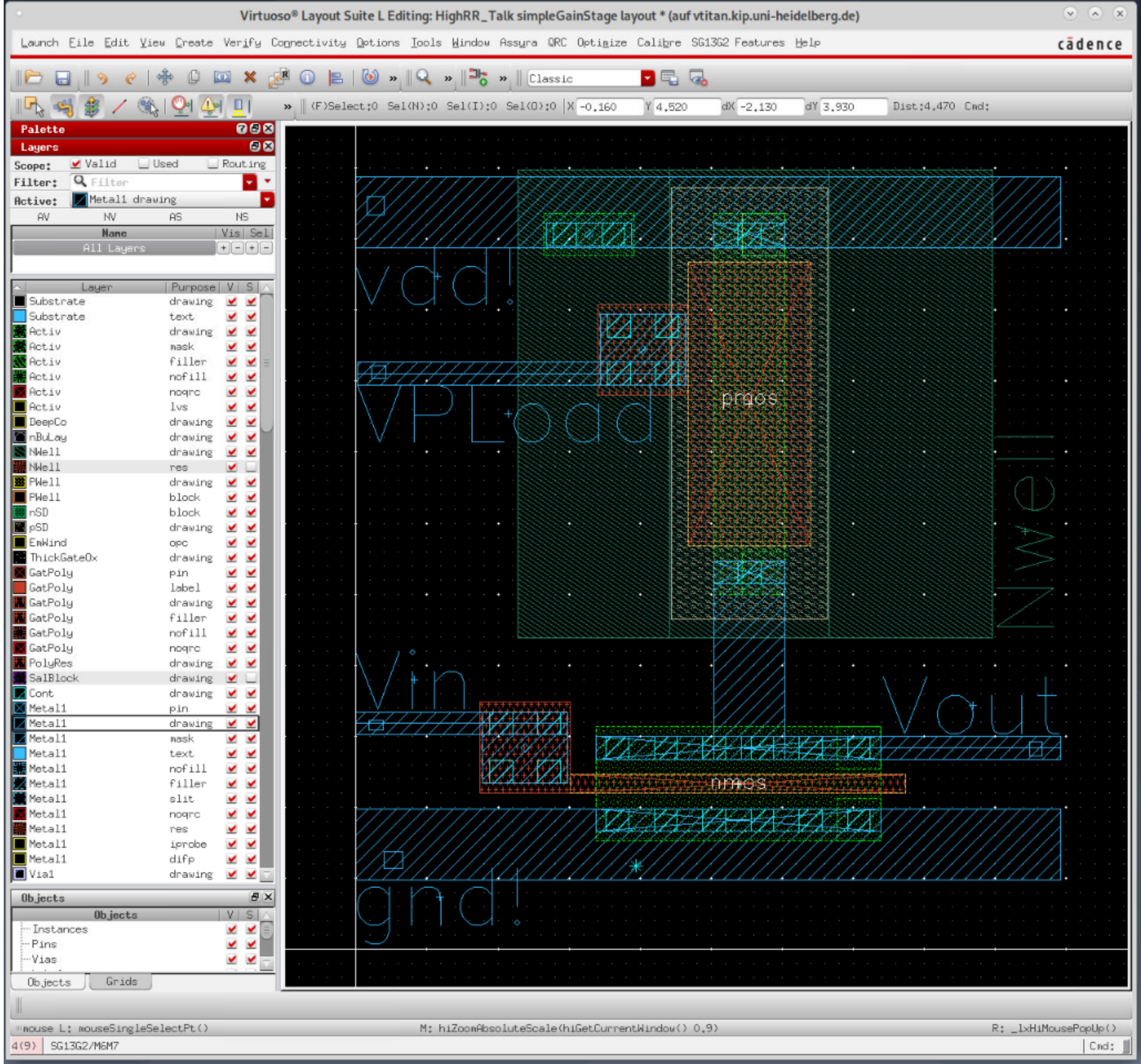

high doping area


gate poly silicon


metal 1

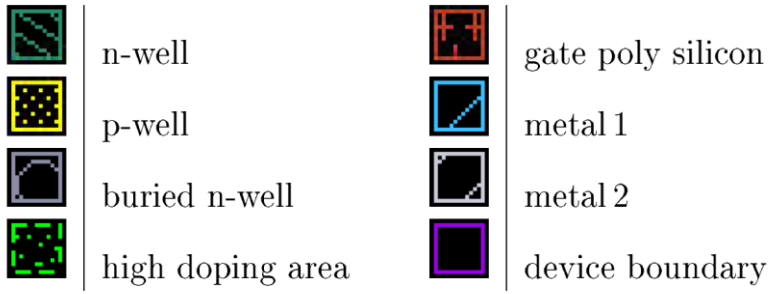

metal 2

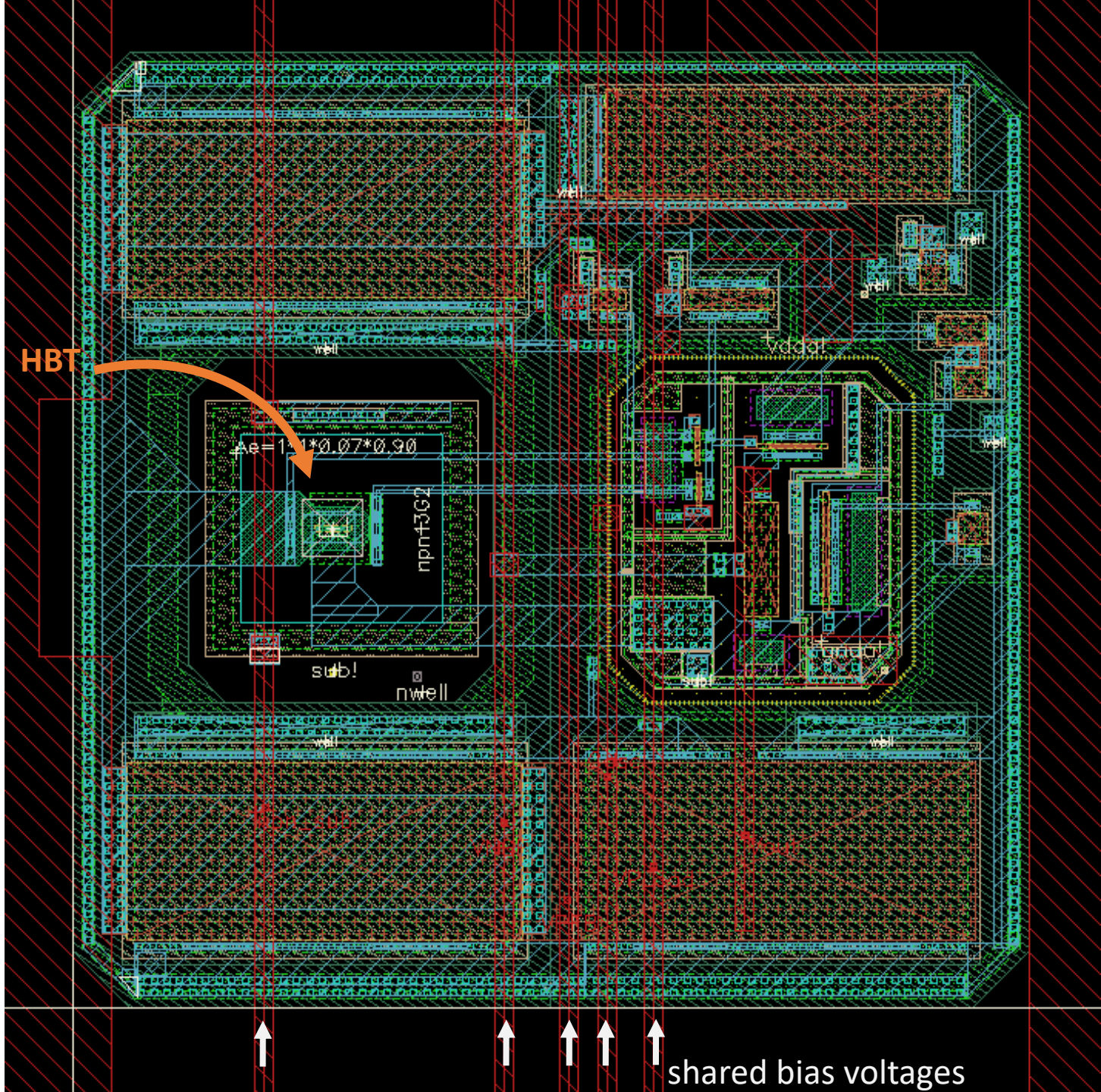

device boundary



Pixel Layout

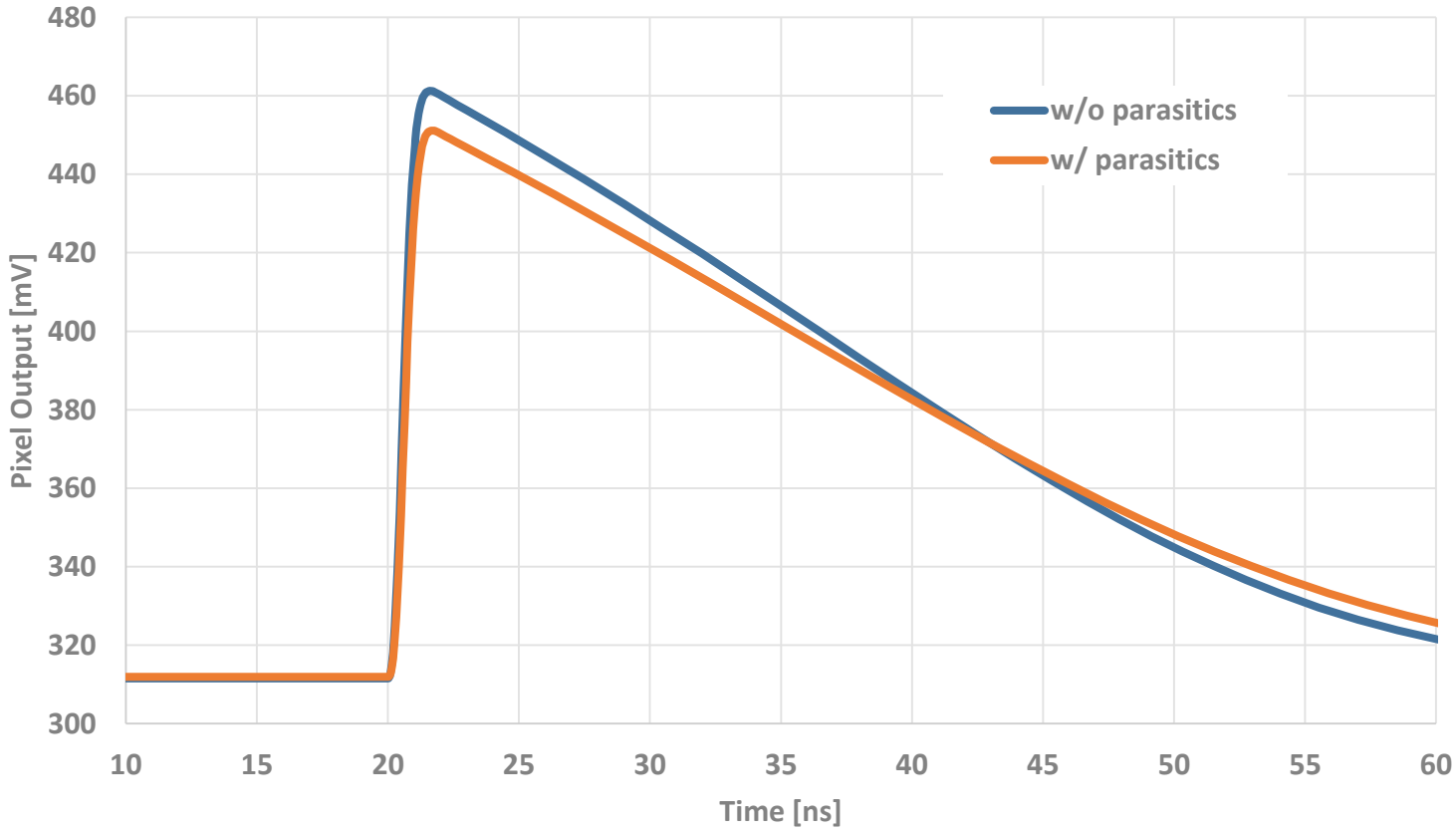
- implant size $26 \times 26\ \mu m^2$
  - pixel size $41 \times 41\ \mu m^2$
- HBT in separated p-well with double guard ring
- minimized parasitic capacities
  - avoid overlapping metal areas
- shared bias voltages for all pixels





Parasitic Simulation

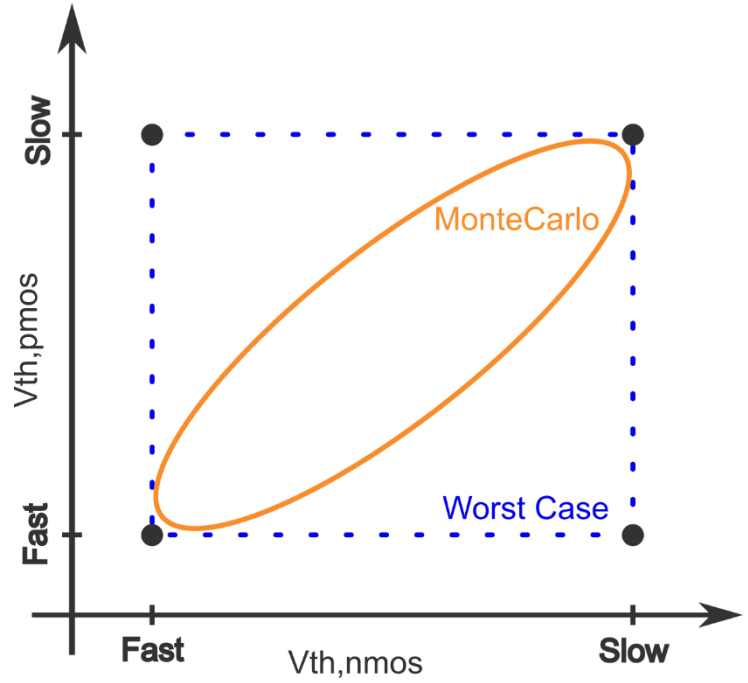
parameter	w/o parasitics	w/ parasitics
Amplitude	$149.8\ mV$	$139.2\ mV$
Rise Time	$741.2\ ps$	$789.4\ ps$
Slew Rate	$161.7\ mV/ns$	$141.1\ mV/ns$
ToA	$480\ ps$	$540\ ps$



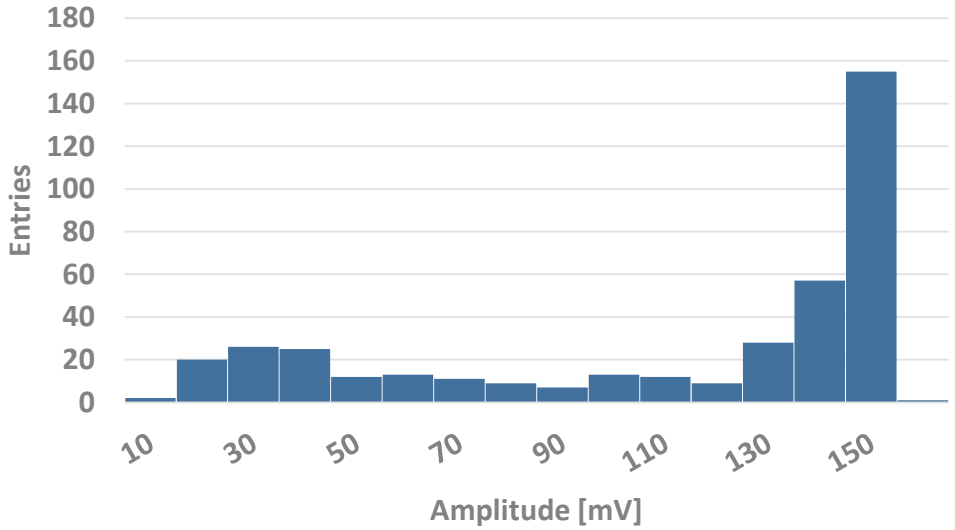
- not possible to extract parasitic from large layouts
- identify important parasitics and use an estimation
  - e.g. long lines between pixel and periphery

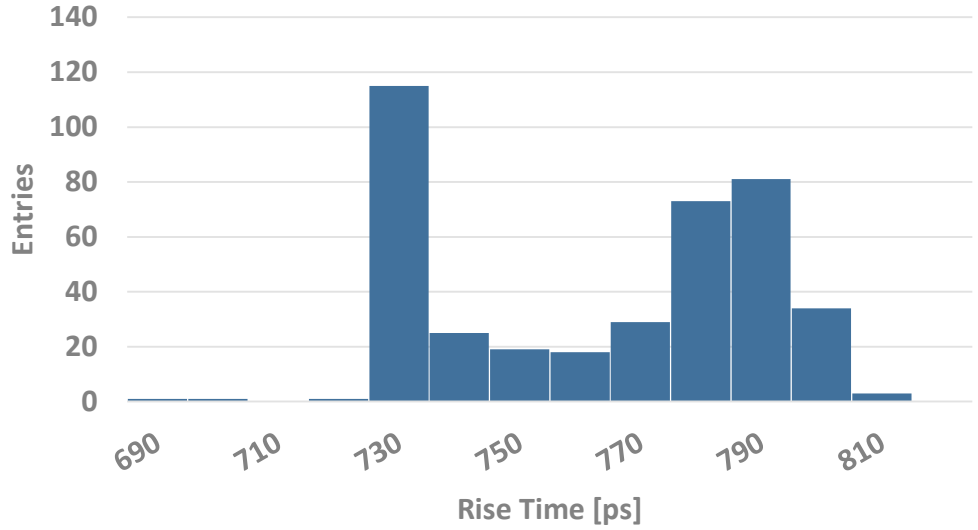
Monte Carlo Simulation

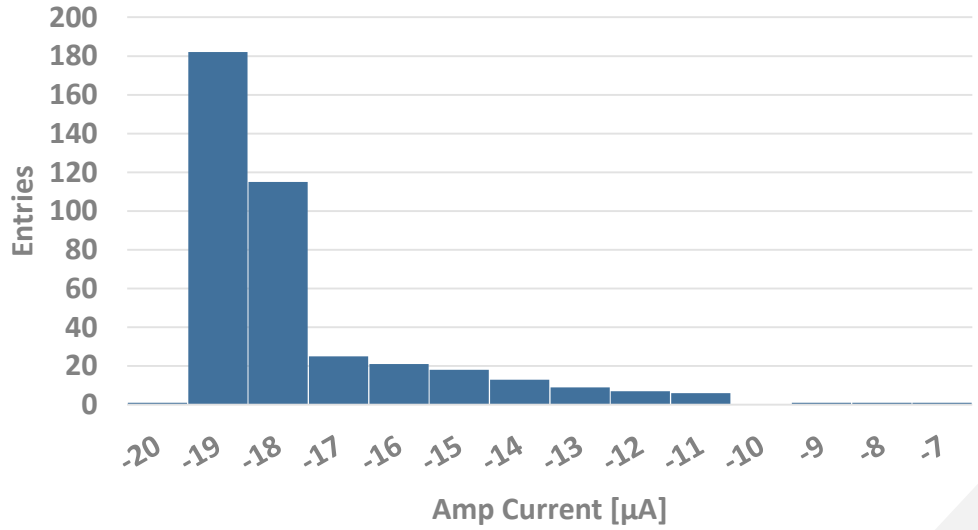
- Statistic analysis of the circuit performance
  - ..depending on global process parameters
  - ..depending on local device parameters (mismatch)



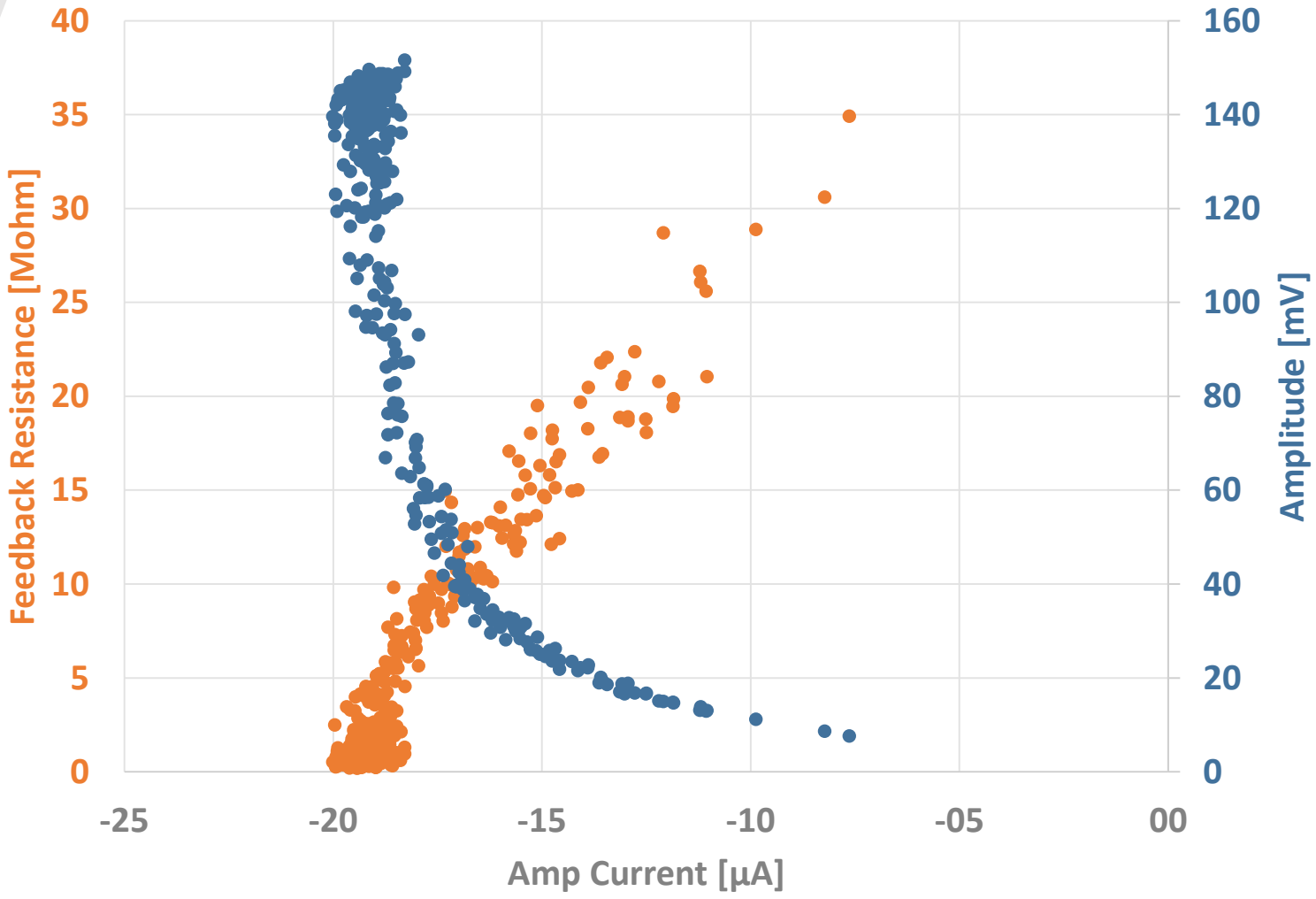
Monte Carlo Simulation – mismatch







Monte Carlo Simulation



- clear correlation between Amp/R_f – Current
- large values of R_f result in a higher output level -> decrease dynamic range
- change working point

Monte Carlo Simulation – Worst Point

- examine worst point in mismatch simulation
  - use bias voltages to optimize working point

	Old Working Point	New Working Point	Ideal Working Point
Amplitude	$7.63\ mV$	$115.0\ mV$	$149.8\ mV$
Rise Time	$734.5\ ps$	$1198\ ps$	$741.2\ ps$
Slew Rate	$8.31\ mV/ns$	$76.8\ mV/ns$	$161.7\ mV/ns$

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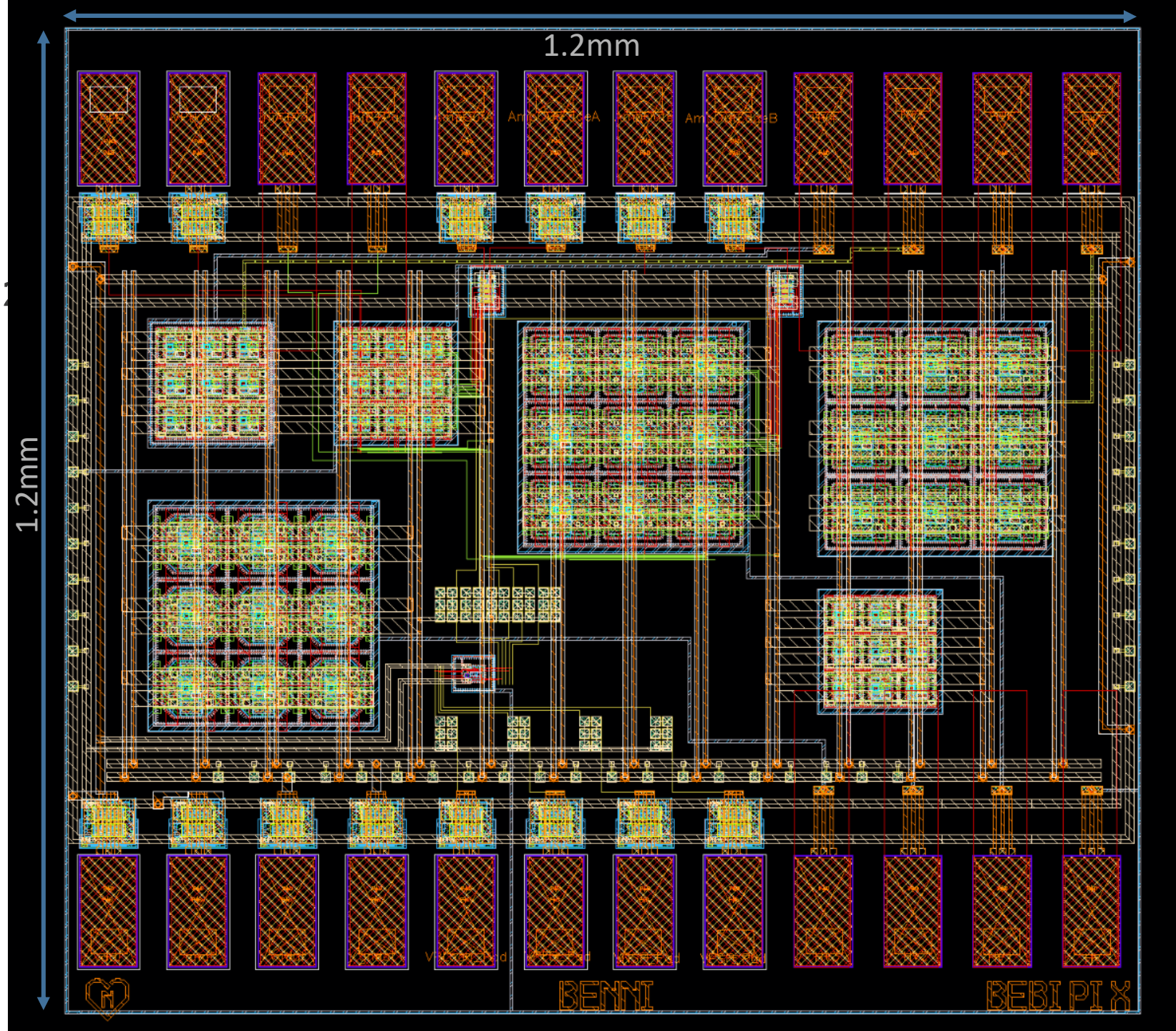
- Size:~1.2 × 1.2 mm^2
- 24 Pads
  - 4 supply voltages
  - 4 bias voltages
  - 2 sense wires
  - 2 injections
  - 4 outputs
  - 8 HV connections



BeBiPix

- featured structures:
  - 2 functional 3x3 matrices
  - 4 test structures
  - bias block
  - analogue output cell