



Cadence Virtuoso Design Flow

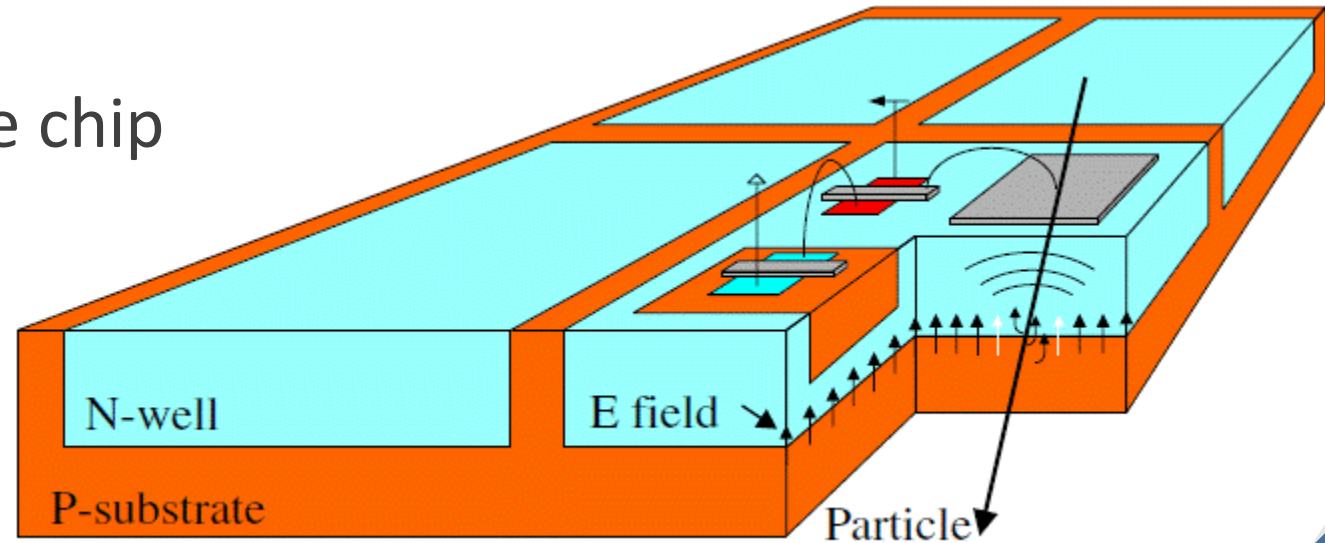
On the example of the test-structure BeBiPix

Benjamin Weinläder

08.06.2022

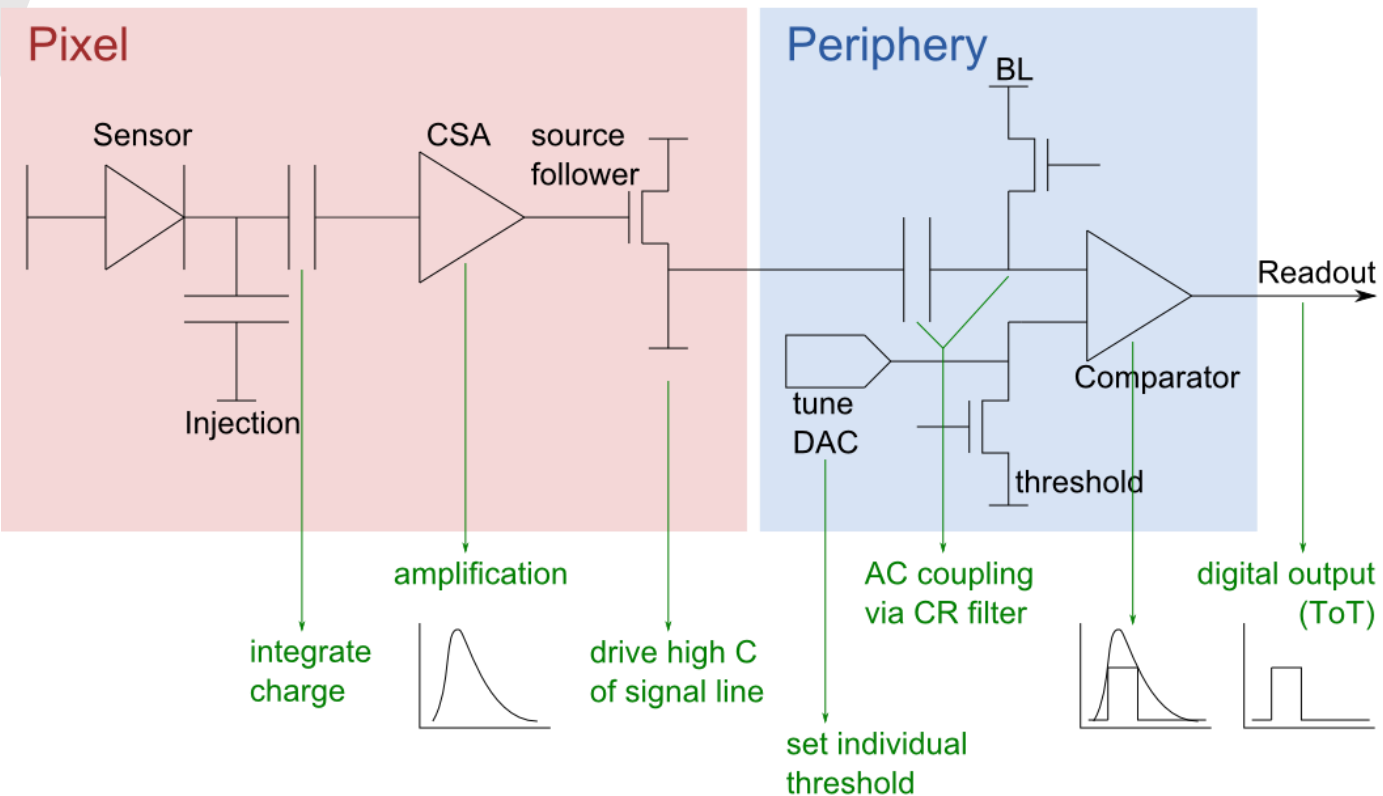
High Voltage – Monolithic Active Pixel Sensors

- detection and readout on one chip
- in-pixel electronics
- high voltage $\sim 100V$
- fast charge detection via drift
- large depletion area
- commercially available processes
- possibility to thin sensors to $\sim 50\mu m$



I. Peric, P. Fischer et al.:
NIM A 582 (2007) 87

High Voltage – Monolithic Active Pixel Sensors



typical readout schematics:

- in-pixel charge sensitive amplifier
- digitisation in-pixel is possible
- further processing in the periphery

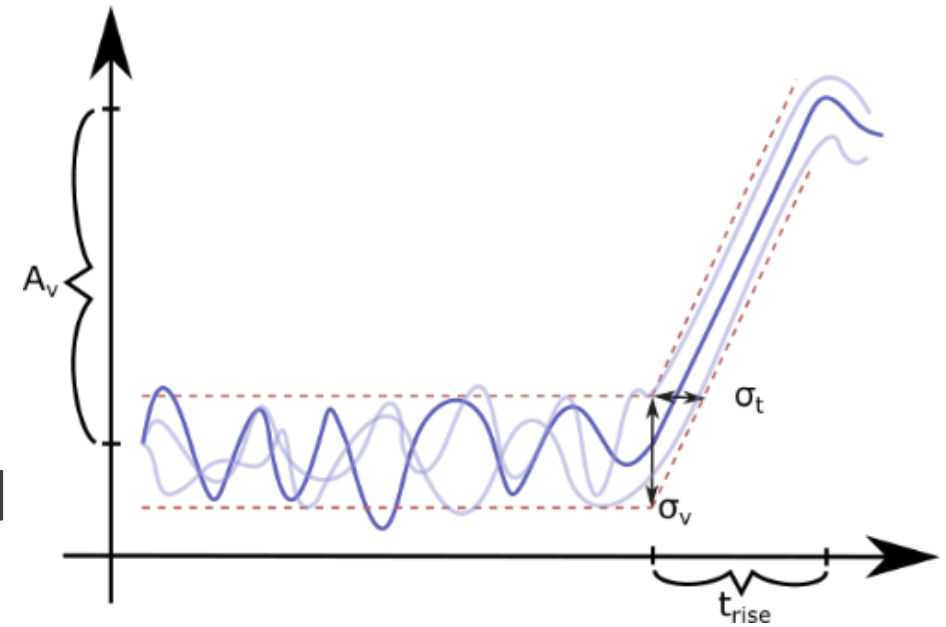
Starting Point: BeBiPix

Task:

- reduce time resolution to sub-nanosecond regime
- benefit from advantages of BiCMOS-Technology
 - combination of bipolar (HBT) and MOS transistors
- simplified model for the time resolution:

$$\frac{\sigma_t}{\sigma_v} \approx \frac{t_{rise}}{A_v} \rightarrow \sigma_t \approx \frac{t_{rise}}{SNR}$$

mostly influenced by the amplifier
→ use bipolar transistor here



Advantages of BiCMOS

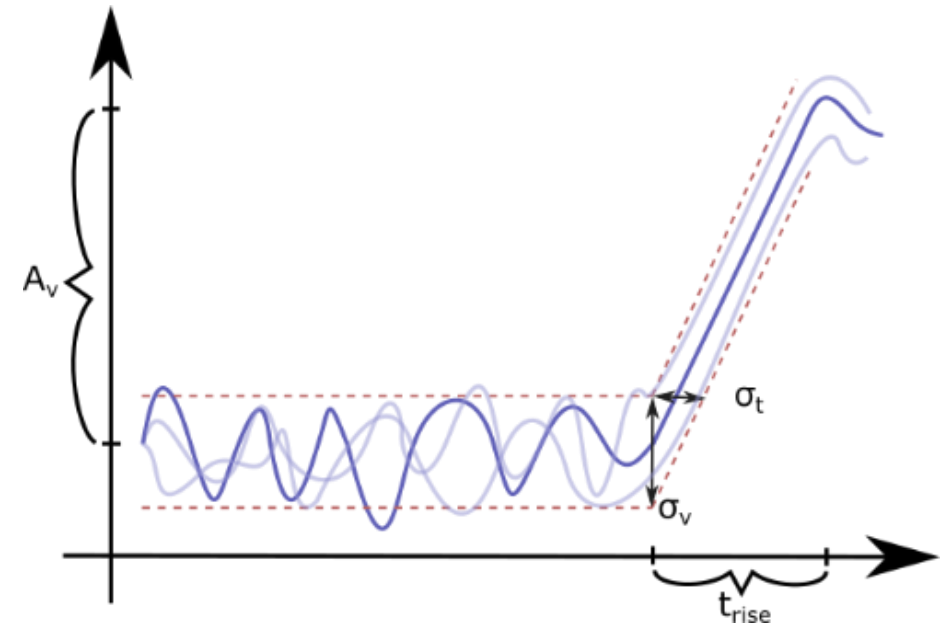
• $\frac{\sigma_t}{\sigma_v} \approx \frac{t_{rise}}{A_v} \rightarrow \sigma_t \approx \frac{t_{rise}}{SNR}$

• comparison MOSFET and BJT:

• τ = integration/measuring time

$$ENC^2 \sim \frac{a}{2\tau} C_{in}^2 + \frac{\tau}{2} b + 2c C_{in}^2$$

	MOSFET	BJT
a	therm. noise	shot noise
b	shot noise (leakage current)	shot noise (leakage current)
c	1/f-noise	-



Advantages of BiCMOS

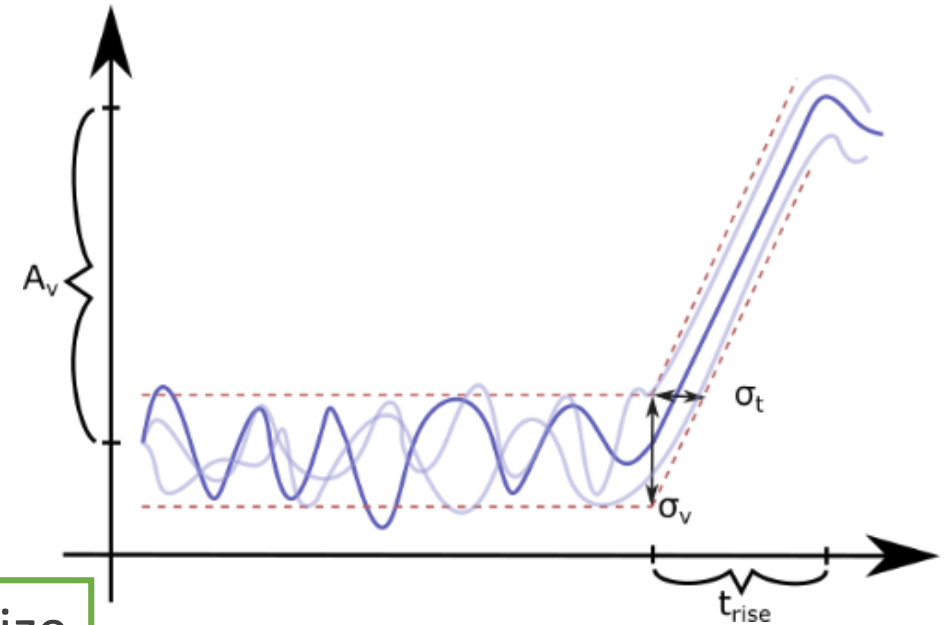
- $\frac{\sigma_t}{\sigma_v} \approx \frac{t_{rise}}{A_v} \rightarrow \sigma_t \approx \frac{t_{rise}}{SNR}$

- comparison MOSFET and BJT:

- τ = integration/measuring time

$\sim \tau \rightarrow$ minimize

$$ENC^2 \sim \frac{a}{2\tau} C_{in}^2 + \frac{\tau}{2} b + 2c C_{in}^2$$



	MOSFET	BJT
a	therm. noise	shot noise
b	shot noise (leakage current)	shot noise (leakage current)
c	1/f-noise	-

$\sim \frac{R_B}{\beta} \rightarrow$ minimize

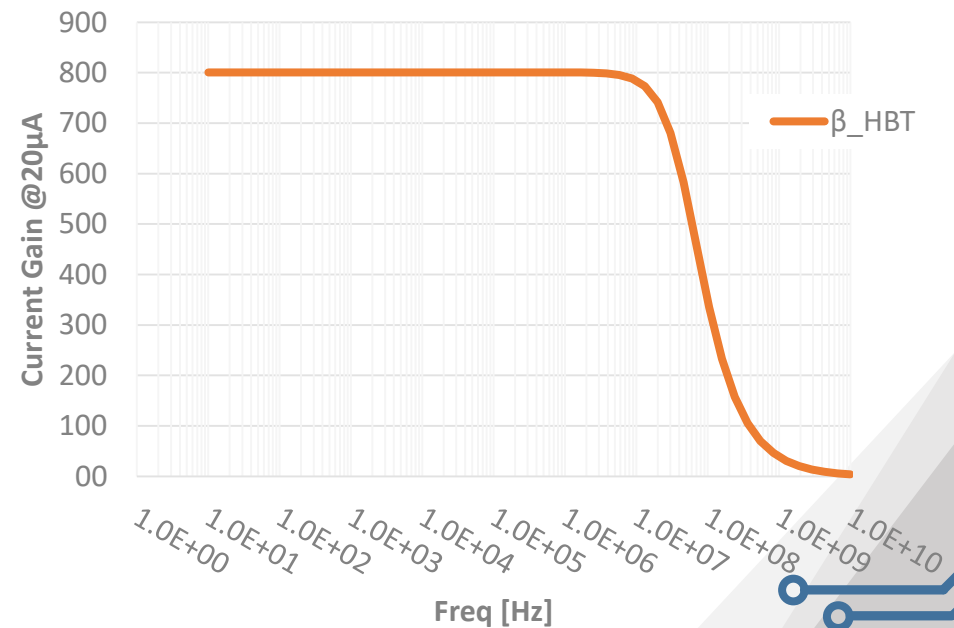
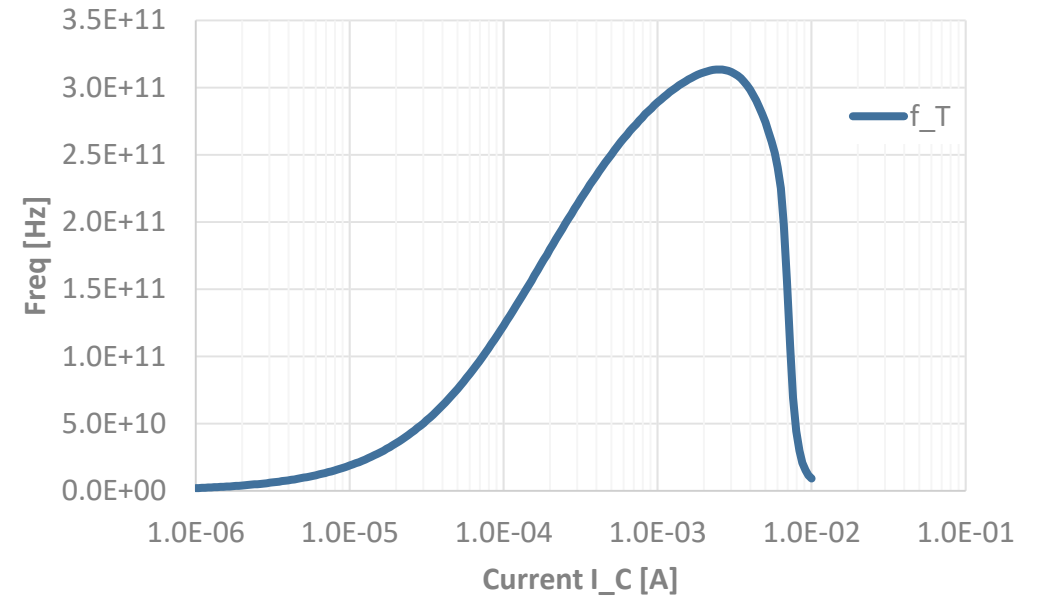
Advantages of BiCMOS

- transit frequency f_T :
 - max. Freq. with $\beta = 1$
 - depending on current I_C
- power influences performance

Noise

Trade off

Power



Advantages of BiCMOS

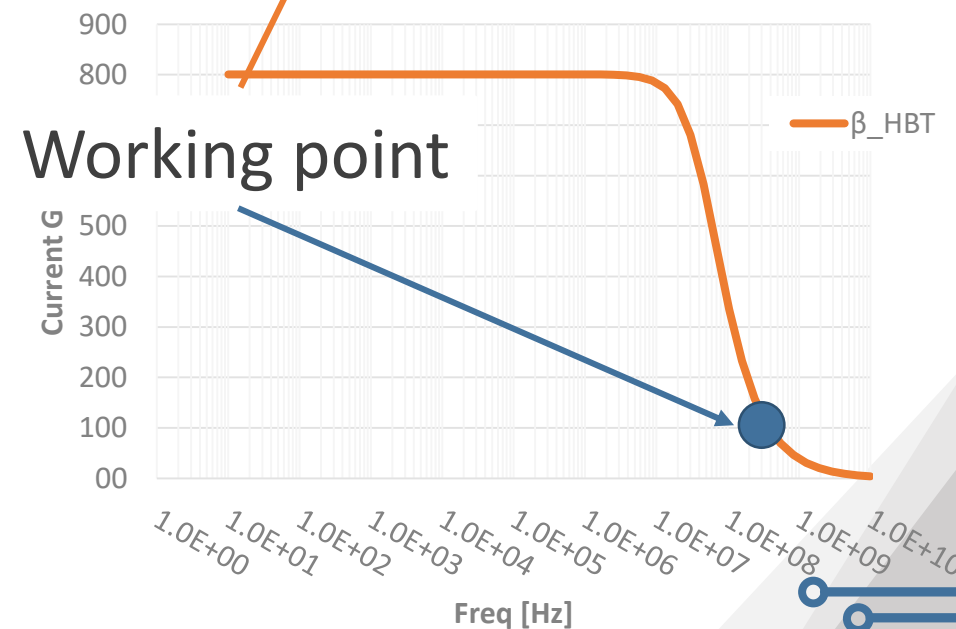
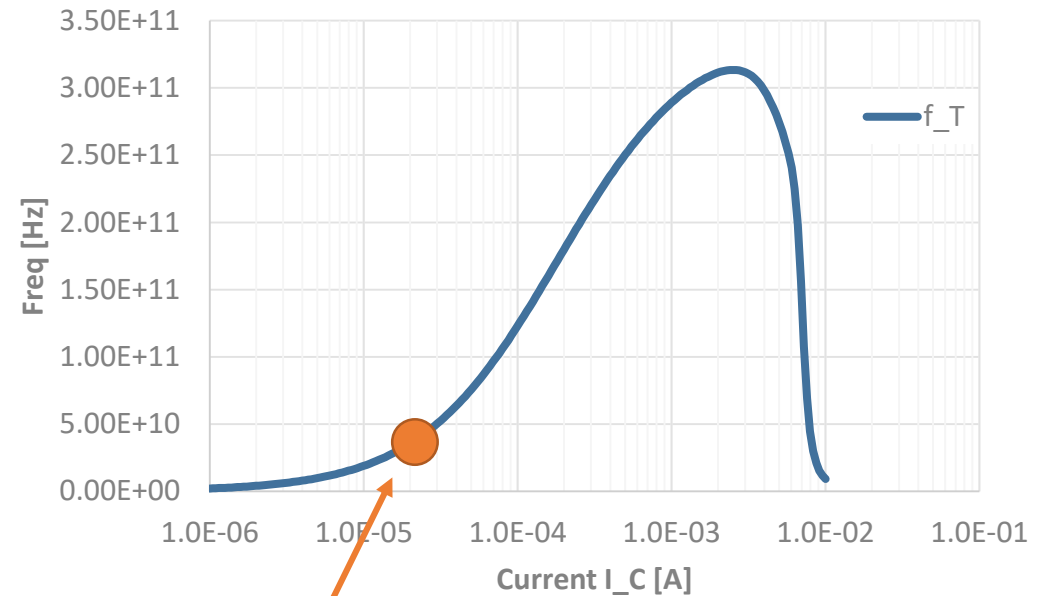
- transit frequency f_T :
 - max. Freq. with $\beta = 1$
 - depending on current I_C
- Power influences performance

Noise



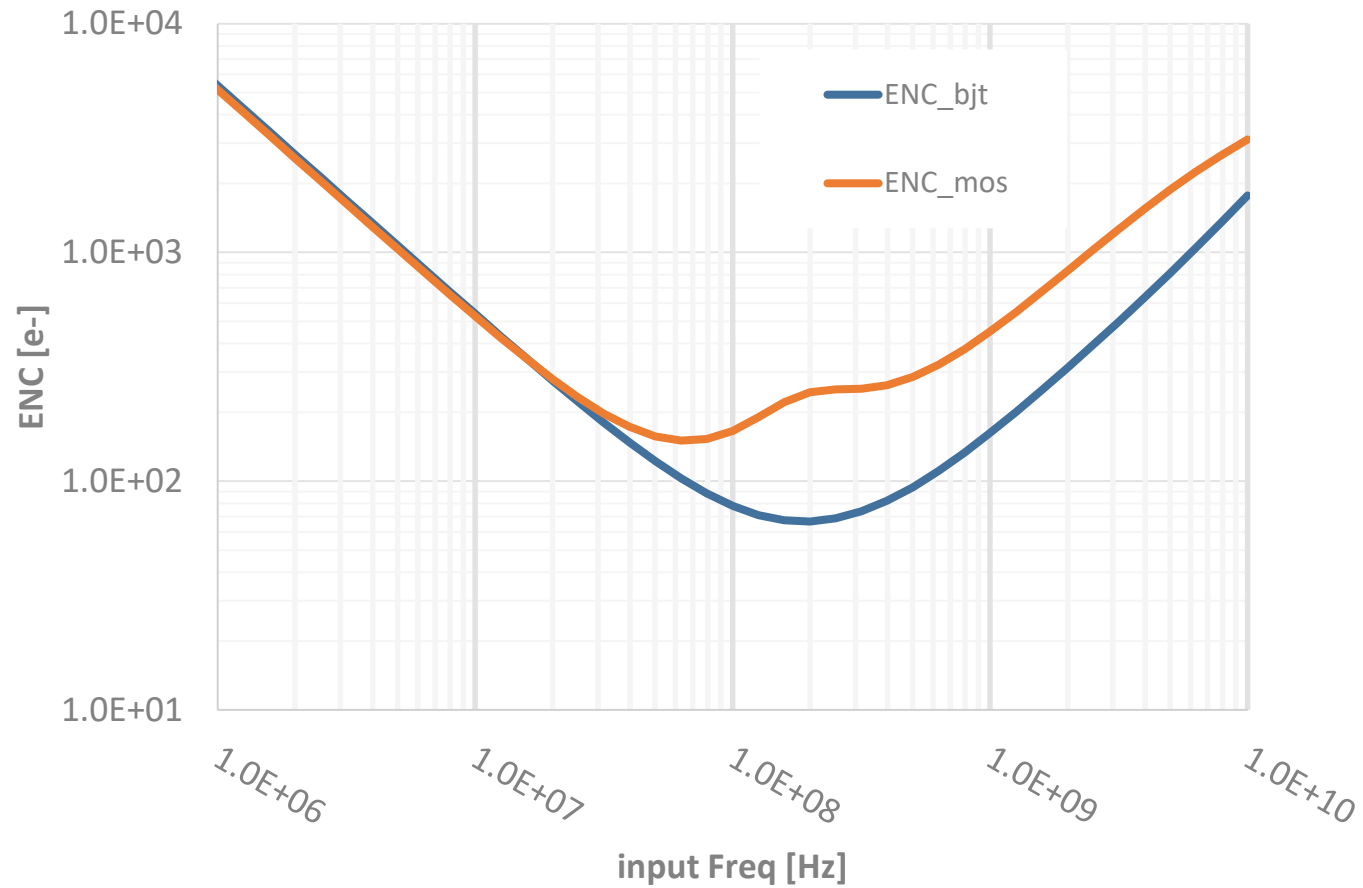
Power

Single pre-amplifier with **fast rising edge**, **low noise** and **low power consumption**

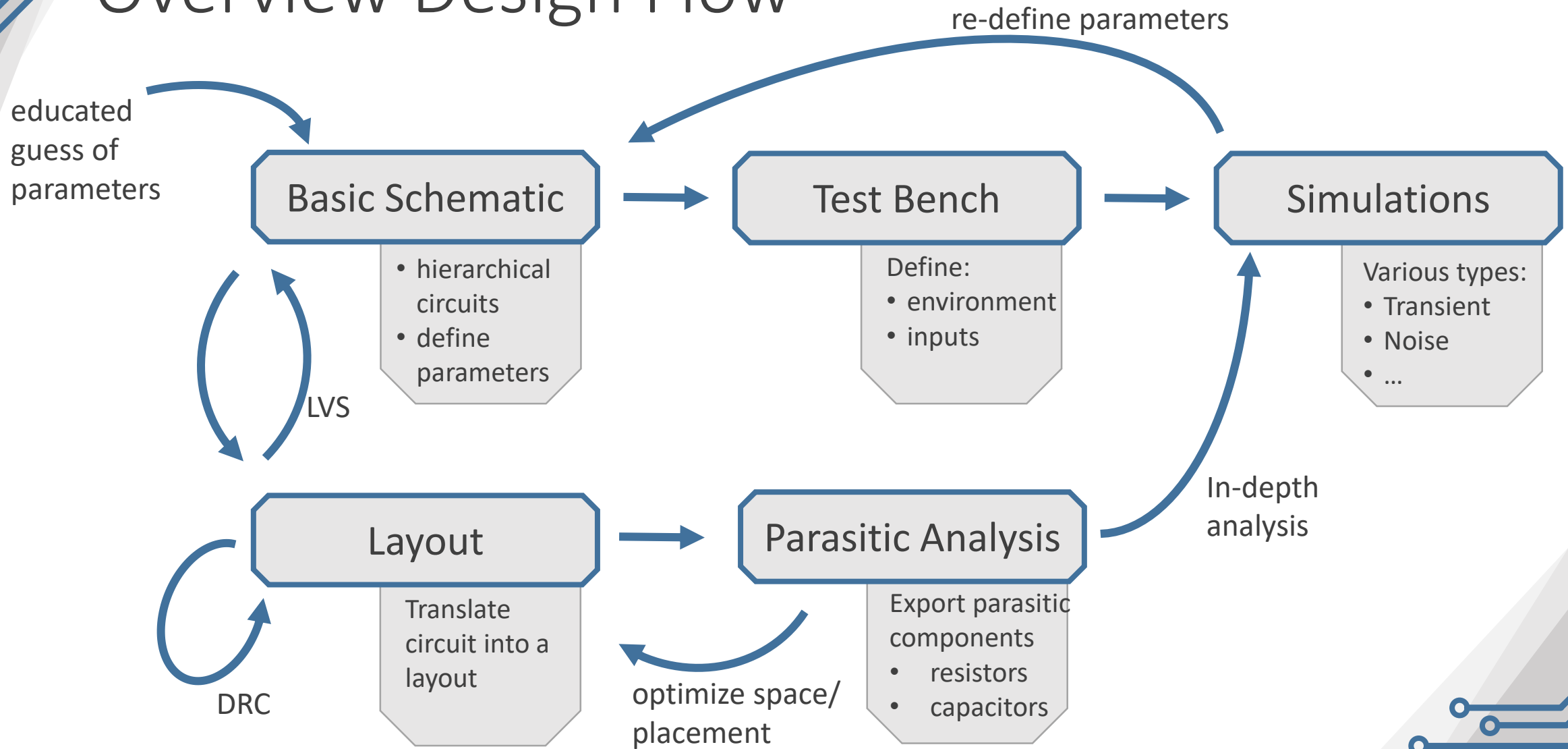


Working point

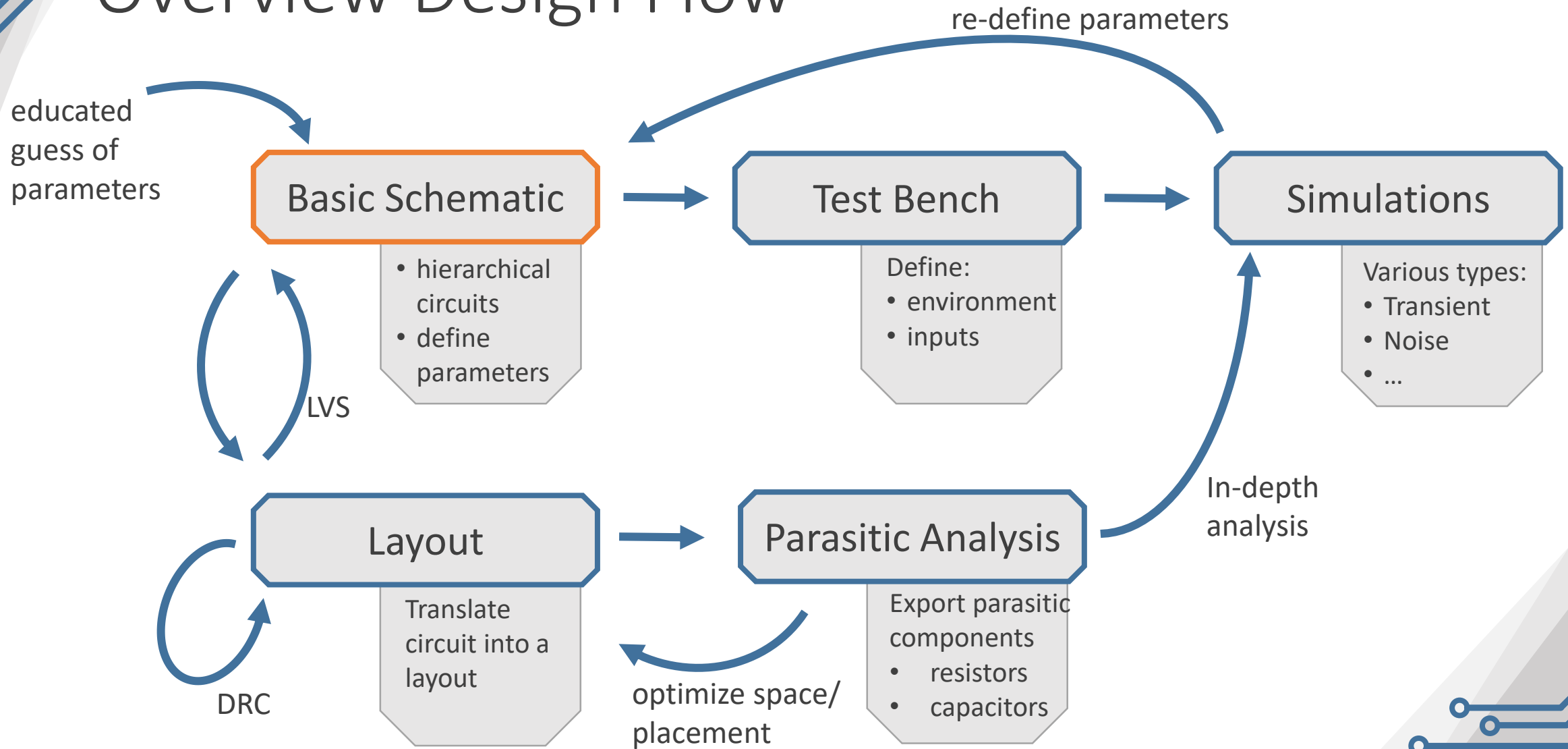
Advantages of BiCMOS



Overview Design Flow



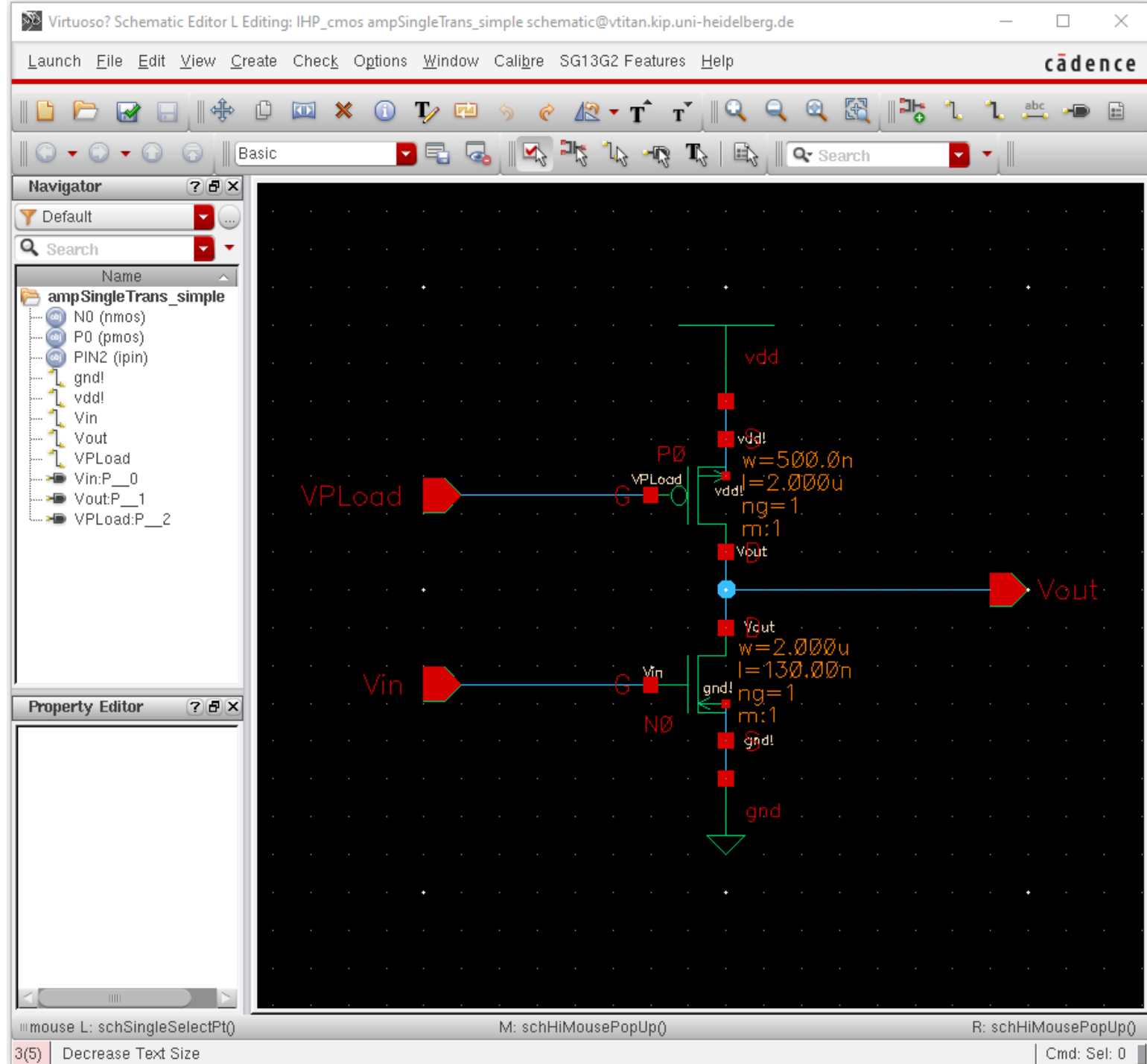
Overview Design Flow



Schematic Editor

simple gain stage:

- pmos current source
- nmos input transistor/switch



Schematic Editor

simple gain stage:

- pmos current source
- nmos input transistor/switch

circuit parameter:

- transistor width/length
- bias voltages

The screenshot displays the Cadence Virtuoso Schematic Editor interface. The title bar indicates the file name: "Virtuoso? Schematic Editor: IHP_cmos ampSingleTrans_simple schematic@vtitan.kip.uni-heidelberg.de". The menu bar includes "Launch", "File", "Edit", "View", "Create", "Check", "Options", "Window", "Calibre", "SG13G2", "Features", and "Help". The toolbar contains various icons for file operations, navigation, and editing. The Navigator panel on the left shows a project tree for "ampSingleTrans_simple" with components like "N0 (nmos)", "P0 (pmos)", and "PIN2 (ipin)". The Property Editor at the bottom is currently empty. The main workspace shows a schematic diagram of a simple gain stage. The circuit consists of a PMOS transistor (P0) and an NMOS transistor (N0). The PMOS transistor is connected to a "global net" labeled "vdd" and its gate is connected to "VPLoad". The NMOS transistor's gate is connected to "Vin". The NMOS transistor's source is connected to "gnd!". The output of the NMOS transistor is labeled "Vout" and is also connected to the "global net" labeled "vdd". The PMOS transistor's drain is connected to "Vout". The NMOS transistor's drain is connected to "gnd!". The circuit is annotated with "transistor parameters" for both transistors. For the PMOS transistor (P0), the parameters are: $w=500.0n$, $l=2.000u$, $ng=1$, and $m:1$. For the NMOS transistor (N0), the parameters are: $w=2.000u$, $l=130.00n$, $ng=1$, and $m:1$. The input port is labeled "Vin" and the output port is labeled "Vout". The bias voltages are "vdd" and "gnd!".

Schematic Editor

simple gain stage:

- pmos current source
- nmos input transistor/switch

$$\begin{aligned} V_{N,gs} &\rightarrow vdd \Rightarrow \\ I_{N,ds} &\rightarrow I_{sat} \end{aligned}$$

$$\begin{aligned} V_{N,gs} &\rightarrow 0 \Rightarrow \\ I_{N,ds} &\rightarrow 0 \end{aligned}$$

The screenshot displays the Cadence Virtuoso Schematic Editor interface. The main window shows a schematic of a simple gain stage. The circuit consists of a PMOS current source (P0) and an NMOS input transistor (N0). The PMOS source is connected to VDD, and the NMOS source is connected to GND. The gates of both transistors are connected to a common node labeled P0. The input of the NMOS transistor is connected to Vin, and the output is connected to Vout. The PMOS transistor has parameters: w=500.0n, l=2.000u, ng=1, m:1. The NMOS transistor has parameters: w=2.000u, l=130.00n, ng=1, m:1. The schematic is annotated with the following conditions:

- $V_{P,gs} = const.$ (indicated by a blue arrow pointing to the P0 node)
- $I_{P,ds} = const.$ (indicated by a blue arrow pointing to the PMOS transistor)

The Navigator panel on the left shows the hierarchy of the schematic, including components like N0 (nmos), P0 (pmos), PIN2 (ipin), gnd!, vdd!, Vin, Vout, VPLoad, and their respective ports. The Property Editor at the bottom is empty.

Schematic Editor

Virtuoso? Schematic Editor L Editing: IHP_cmos ampSingleTrans_simple schematic@vtitan.kip.uni-heidelberg.de

Launch File Edit View Create Check Options Window Calibre SG13G2 Features Help

Basic

Navigator

- Default
- Search
- Name
- ampSingleTrans_simple
 - N0 (nmos)
 - P0 (pmos)
 - PIN2 (ipin)
 - gnd!
 - vdd!
 - Vin
 - Vout
 - VPLoad
 - Vin:P__0
 - Vout:P__1
 - VPLoad:P__2

Property Editor

mouse L: schSingleSelectPt() M: schHiMousePopUp() R: schHiMousePopUp()

3(5) Decrease Text Size Cmd: Sel: 0

Detailed description: This window shows a detailed schematic of a common-source amplifier. The input node is labeled 'Vin' and is connected to the gate of an NMOS transistor (N0). The gate of the PMOS transistor (P0) is connected to 'vdd'. The gates of both transistors are tied together. The drain of the PMOS is connected to 'vdd' through a load resistor 'VPLoad'. The drain of the NMOS is connected to the output node 'Vout'. The source of the NMOS is connected to ground 'gnd!'. The schematic includes device parameters: for N0, $w=2.000\mu$, $l=130.00n$, $ng=1$, $m:1$; for P0, $w=500.0n$, $l=2.000\mu$, $ng=1$, $m:1$. The layout includes a grid and various connection points labeled 'Vdd!', 'gnd!', and 'VPLoad'.

Virtuoso? Schematic Editor L Editing: HighRR_Talk simpleGainStage_sim schematic *@vtitan.kip.uni-heidelberg.de

Launch File Edit View Create Check Options Window Calibre SG13G2 Features Help

Basic

Navigator

sim (Stage)

simpleGainStage

Vin

Vout

VPLoad

I0

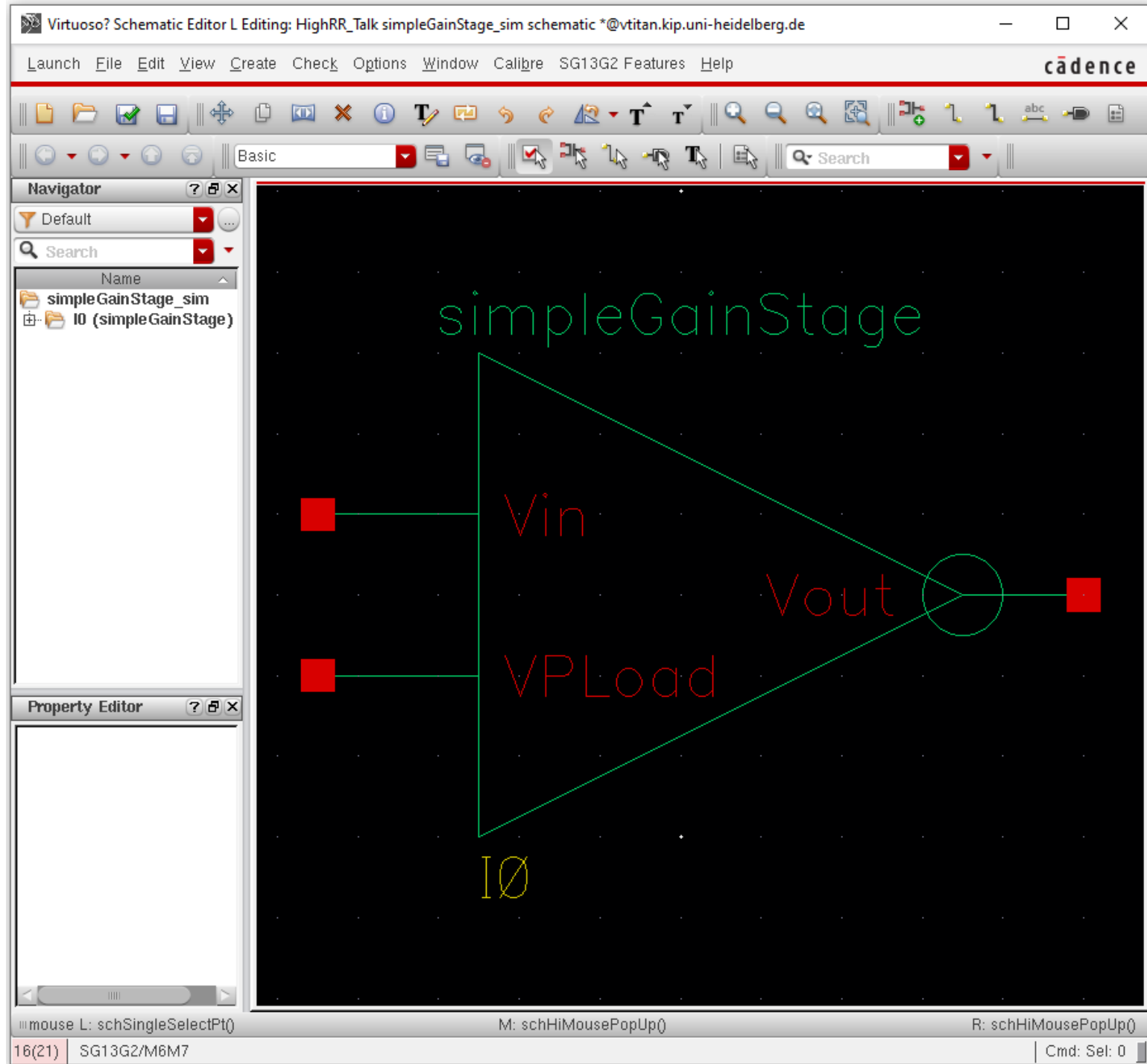
electPt() M: schHiMousePopUp() R: schHiMousePopUp()

17 Cmd: Sel: 0

Detailed description: This window shows a simplified block diagram of the 'simpleGainStage'. The block is represented by a large triangle with three input ports on the left: 'Vin' (top), 'VPLoad' (middle), and 'I0' (bottom). The output port on the right is labeled 'Vout'. The diagram is overlaid with green lines and red squares at the ports. Blue arrows from the detailed schematic in the left window point to the corresponding ports in this block diagram. The layout includes a grid and various connection points.

Schematic Editor

- ↳ hierarchical structure
 - ↳ circuits are divided into smaller blocks
 - ↳ ports are used to interconnect nets
 - ↳ transistors are also just symbols



Schematic Editor

Library



Cell



view

- schematic
- layout
- simulation
- ...

Library Manager: Directory ...perfast/home/bl415/cadence/cds@vtitan.kip.uni-heidelberg.de

File Edit View Design Manager Help

Show Categories Show Files

Library

- HighRR_Talk
- AssuraOutLib
- BeBiPix
- BeBiPixAntenna
- BeBiPixV0
- Cadence_IC
- HighRR_Talk
- IHP_KIT
- IHP_bipolar
- IHP_cmos
- IHP_sg13g2
- LFoundry_KIT
- PADS
- SG13G2
- SG13_Modules
- TestIHP
- Test_1.2V
- Test_3.3V

Category

- Amplifier
- Everything
- Uncategorized
- Amplifier
- Simulations

Cell

simpleGainStage

simpleGainStage

View

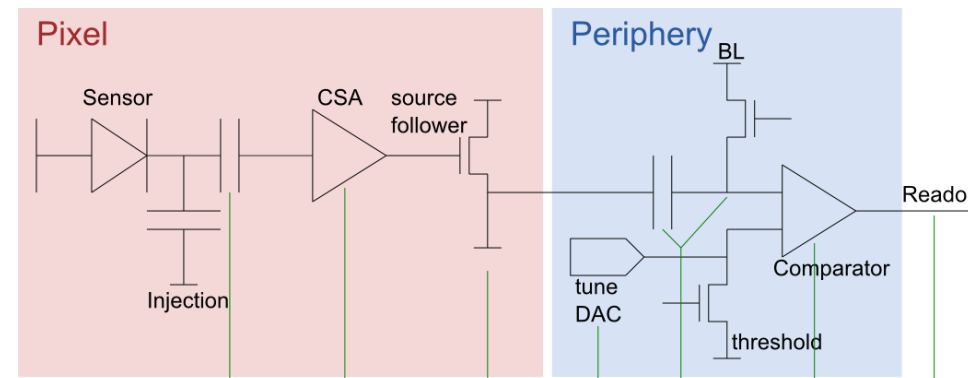
View	Lock	Size
layout		19k
schematic		36k
symbol		23k

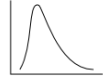
Messages

Warning: The directory: '/superfast/home/bl415/cadence/cds/%/superfast/home/bl415/cadence/cds/amplifier_bipolar' does not exist but was defined in libFile '/superfast/home/bl415/cadence/cds/cds.lib' for Lib 'amplifier_bipolar'.

Lib: HighRR_Talk | Free: 5.91 G

BeBiPix Pixel Schematics



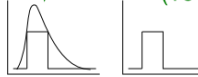
integrate charge 

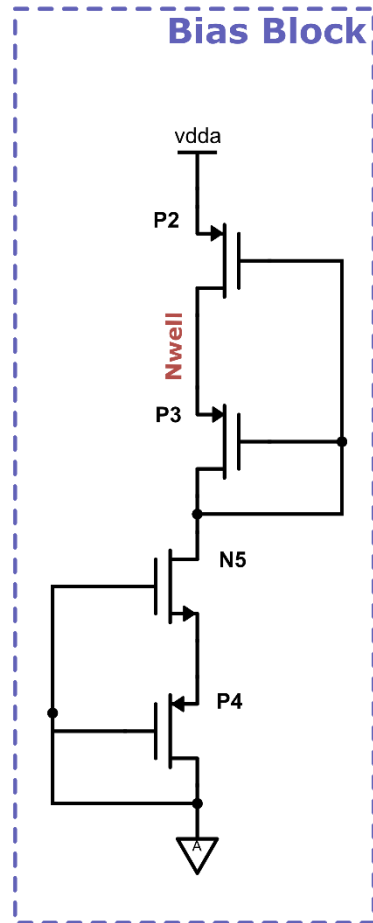
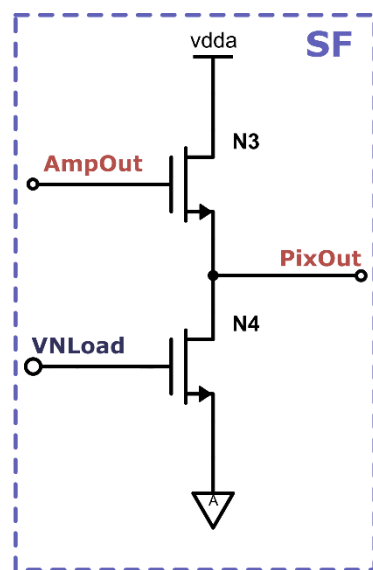
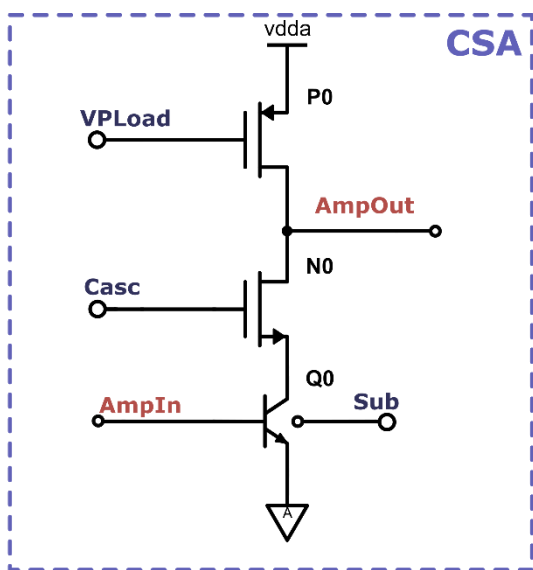
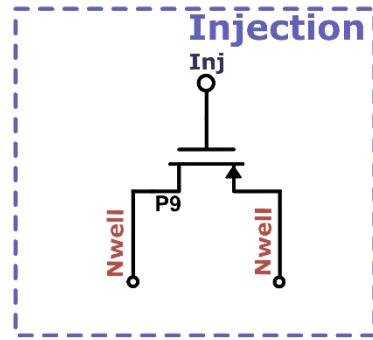
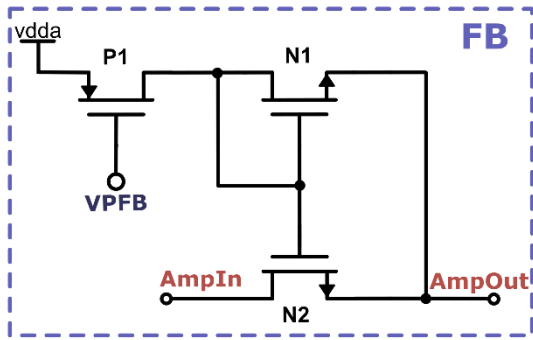
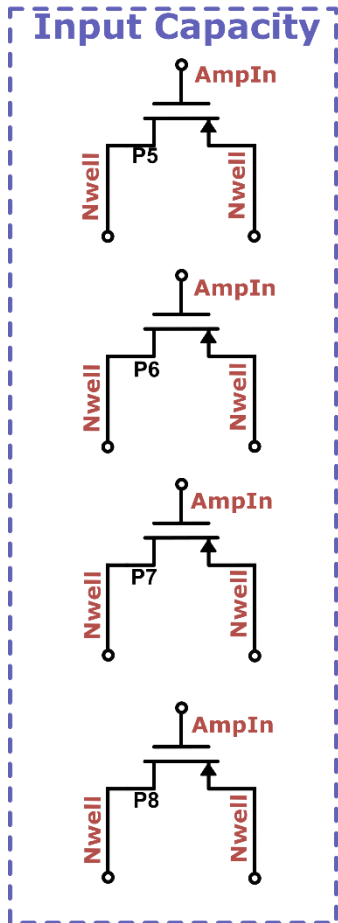
amplification

drive high C of signal line

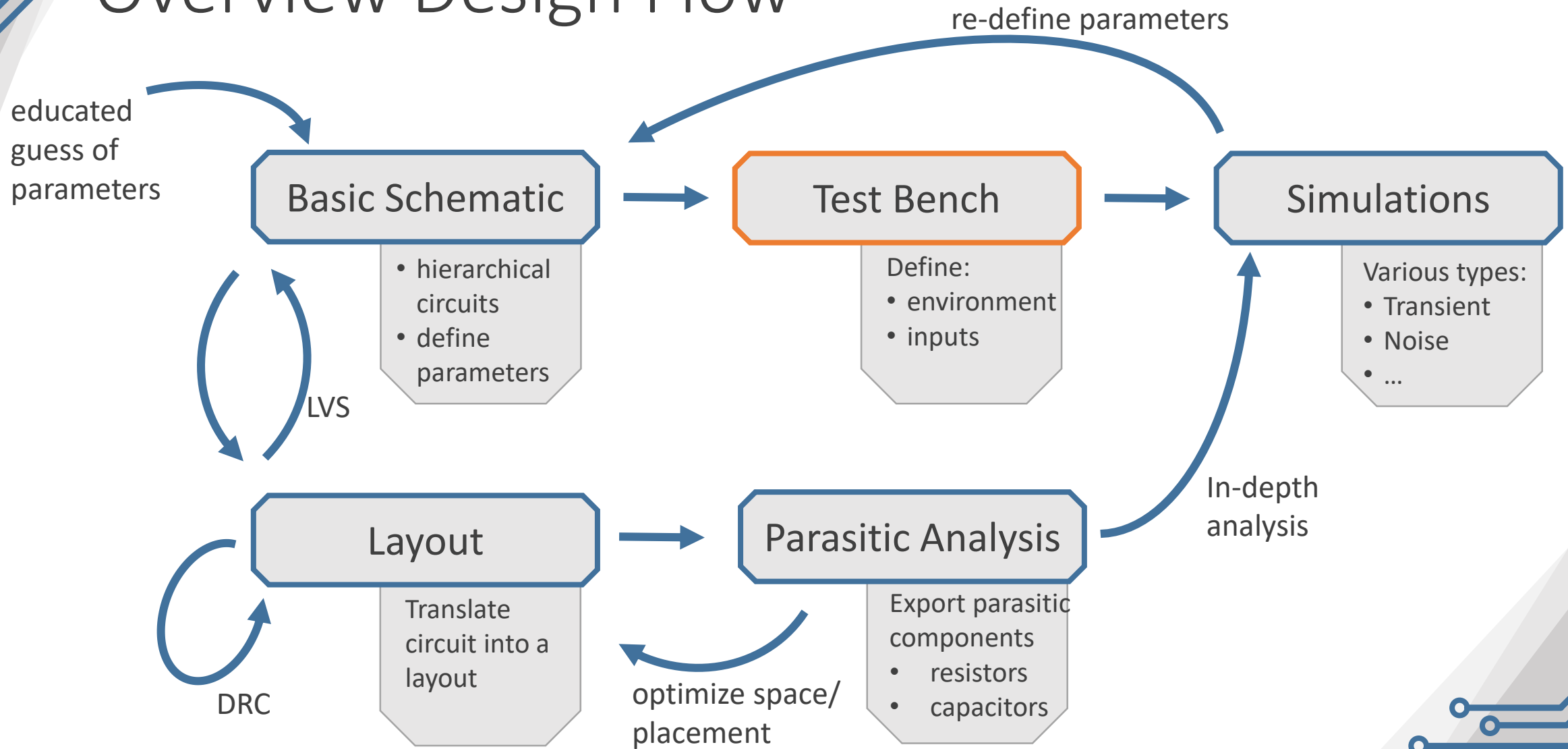
AC coupling via CR filter

set individual threshold

digital output (ToT) 



Overview Design Flow



Test Bench

define environment:

- ideal current/voltage sources
- use variables
- detector capacity:
 $C_{det} = 100fF$
- load capacity:
 $C_{load} = 10fF \rightarrow$
(large transistor gate)

Virtuoso? Schematic Editor L Editing: HighRR_Talk PixelBipolar_sim schematic *@vtitan.kip.uni-heidelberg.de

Launch File Edit View Create Check Options Window Calibre SG13G2 Features Help

Navigator

Default

Search

Name

- PixelBipolar_sim
 - C0 (cap)
 - C1 (cap)
 - I0 (amp..._SF_v4)
 - I5 (ipulse)
 - R0 (res)
 - R1 (res)
 - V0 (vdc)
 - V1 (vdc)
 - V2 (vdc)
 - V4 (vdc)
 - V5 (vdc)
 - Casc
 - gnd!
 - gndal
 - net08
 - net09
 - nwell!
 - vdd!
 - vddal

Property Editor

Powering

Bias Voltages

Input Signal

1(3) SG13G2/M6M7

Cmd: Sel: 0

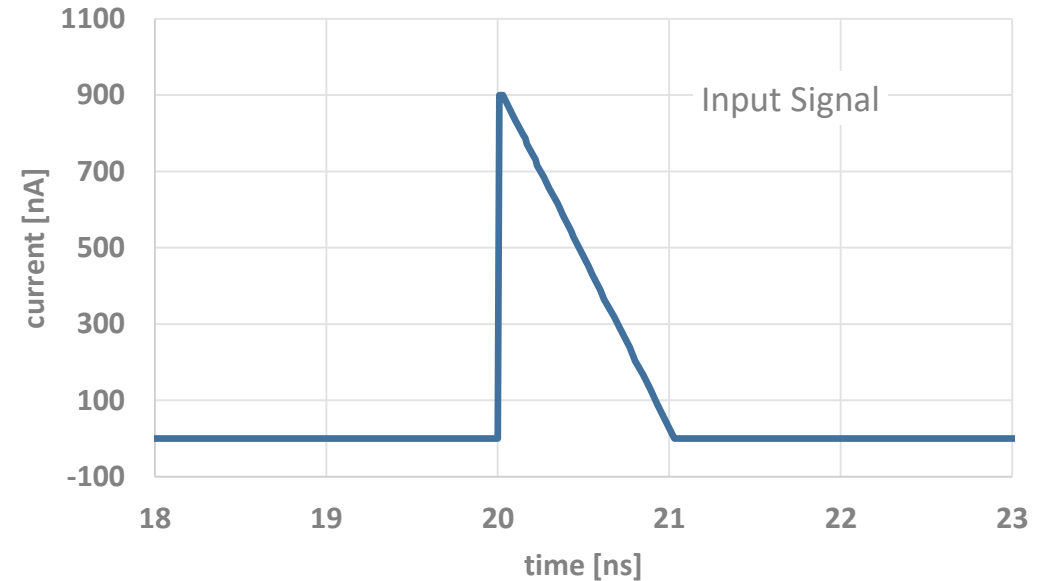
Test Bench

input signal:

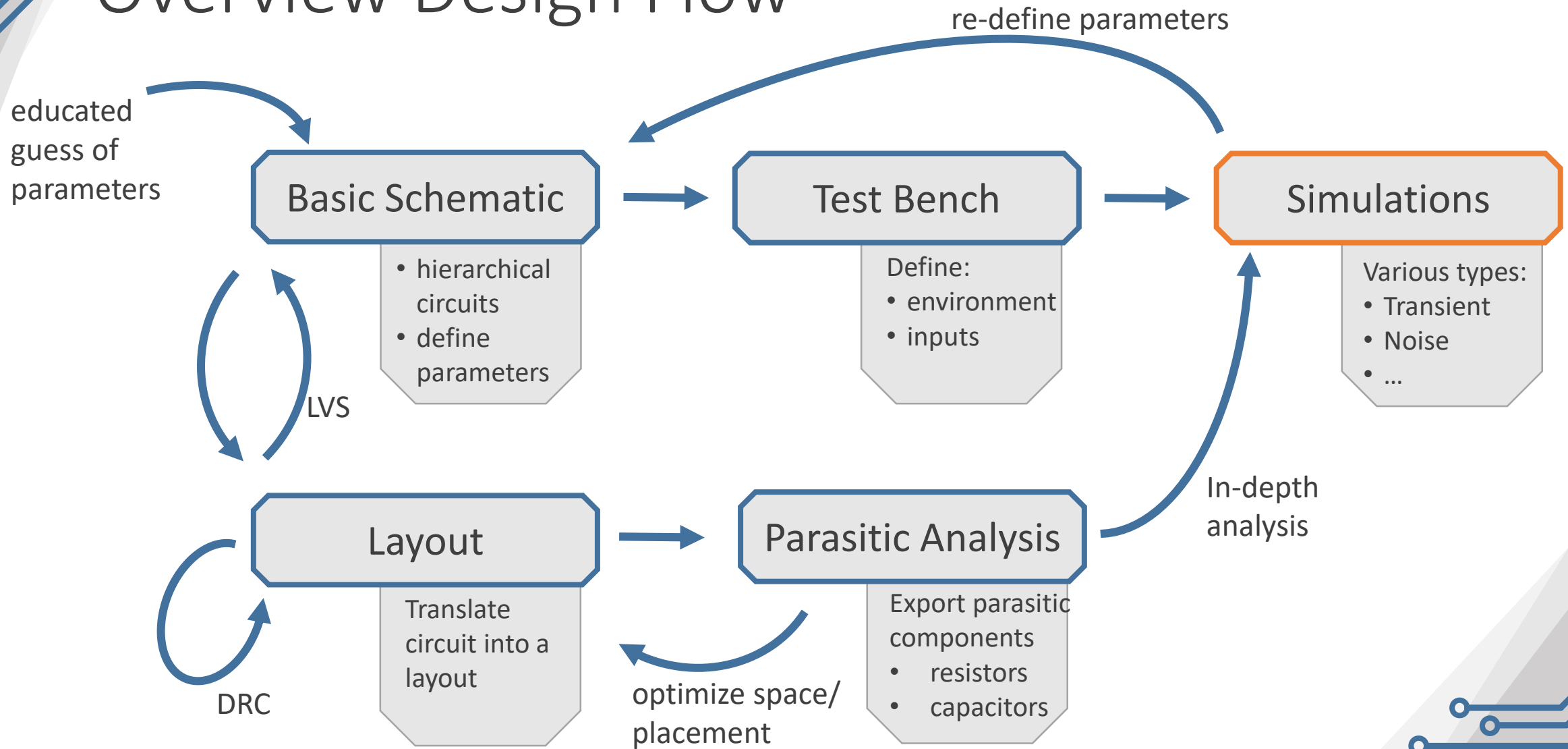
- corresponding to a MIP
- Parameter:
 - $Q_{sig} \approx 0.45fC \approx 2800 e^-$
 - $t_{rise} = 10ps, t_{fall} = 1ns$

power specification:

- limit power consumption to $\sim 20\mu A$



Overview Design Flow



Simulations

define **variables** from the test bench – also useful to simulate circuit parameters

The screenshot shows the Cadence Spectre simulation environment. The title bar reads "ADE L (2) - HighRR_Talk PixelBipolar_sim schematic@vtitan.kip.uni-heidelberg.de". The menu bar includes "Launch", "Session", "Setup", "Analyses", "Variables", "Outputs", "Simulation", "Results", "Tools", "Configure", and "Help". The "Design Variables" panel on the left contains a table with the following data:

Name	Value
1 C_out	10f
2 C_det	100f
3 Isig	900n
4 vdd	1.2
5 VPLoad	465m
6 Casc	1
7 VNFB	600m
8 VNSF	600m
9 ToA	400m

The "Analyses" panel in the center shows a table of simulation types:

Type	Enable	Arguments
1 tran	<input type="checkbox"/>	0 70n conservative
2 noise	<input type="checkbox"/>	10 10G 100 Logarithmic Points Per Decade Start...
3 dc	<input type="checkbox"/>	t
4 ac	<input checked="" type="checkbox"/>	10 10G 10 Logarithmic Points Per Decade Start...

The "Outputs" panel at the bottom shows a table of output signals:

Name/Signal/Expr	Value	Plot	Save	Save Optio
1 Vout		<input checked="" type="checkbox"/>	<input type="checkbox"/>	all
2 I0/Vin		<input checked="" type="checkbox"/>	<input type="checkbox"/>	all
3 I0/AmpOut		<input checked="" type="checkbox"/>	<input type="checkbox"/>	all
4 nwell!		<input type="checkbox"/>	<input type="checkbox"/>	all
5 I0/P0/D		<input type="checkbox"/>	<input type="checkbox"/>	all
6 I_0/amp		<input checked="" type="checkbox"/>	<input type="checkbox"/>	all

At the bottom of the interface, the status bar shows "6(12) Environment ...", "Status: Ready", "T=27 C", "Simulator: spectre", and "State: spectre_state1".

define **type** of simulation

select **outputs** or define **expressions**

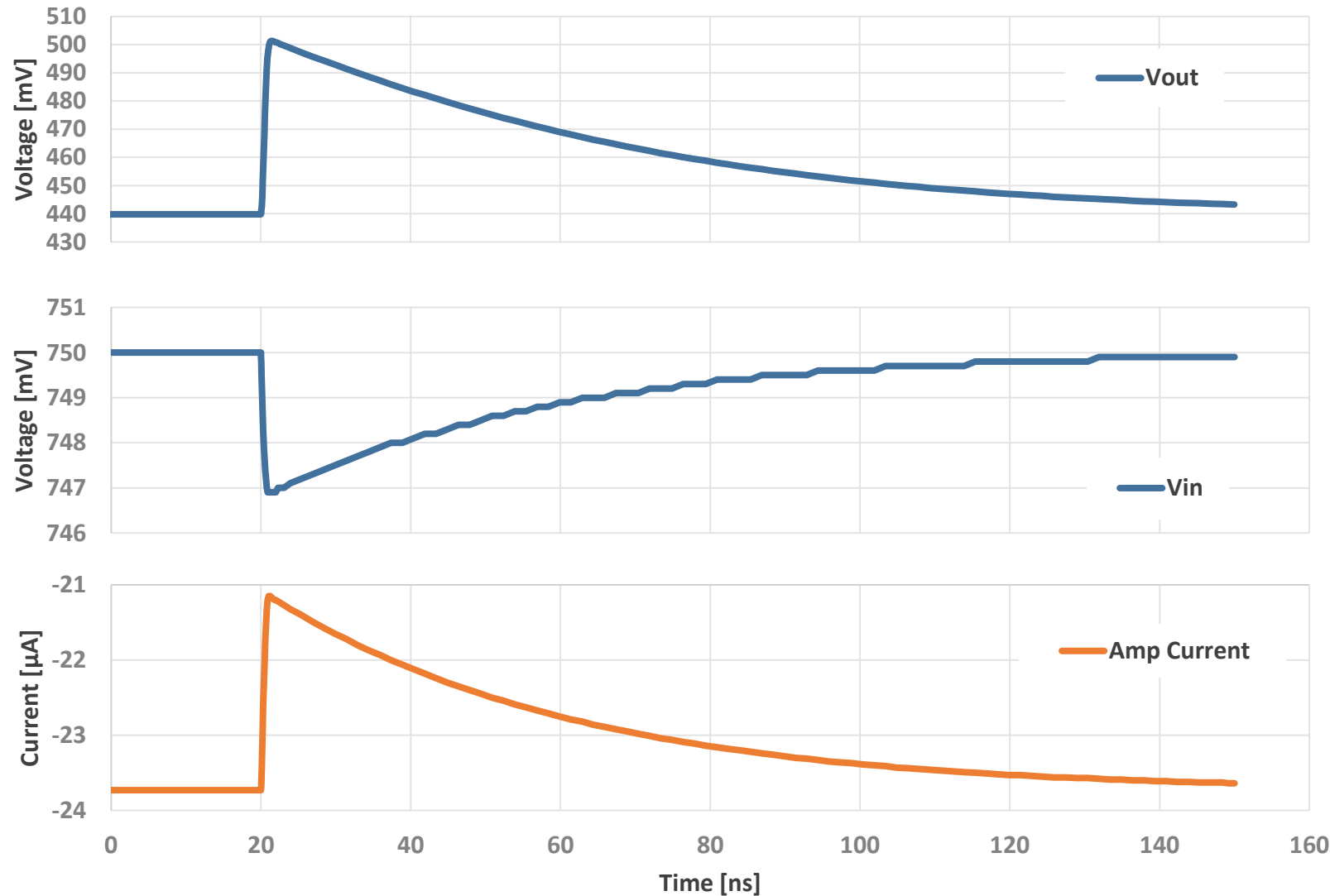
Transient Simulation

shows circuit response to an input signal:

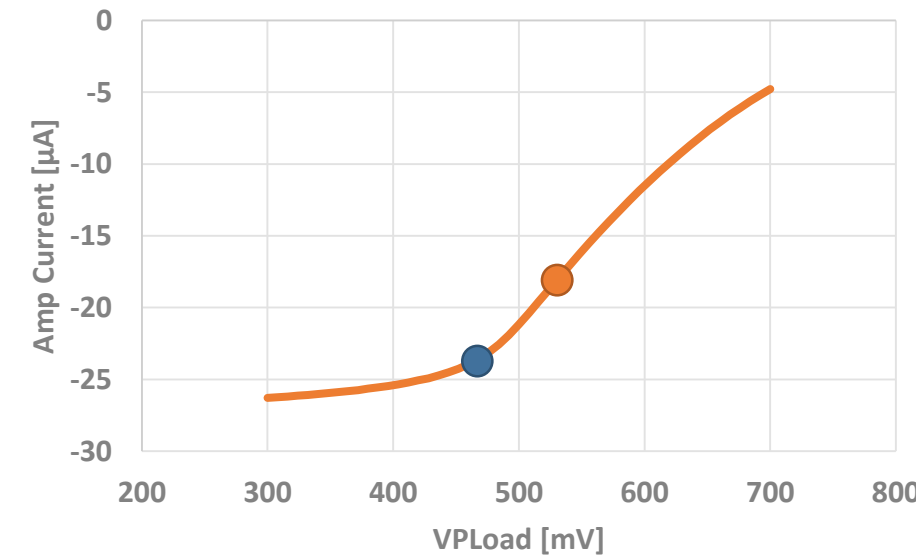
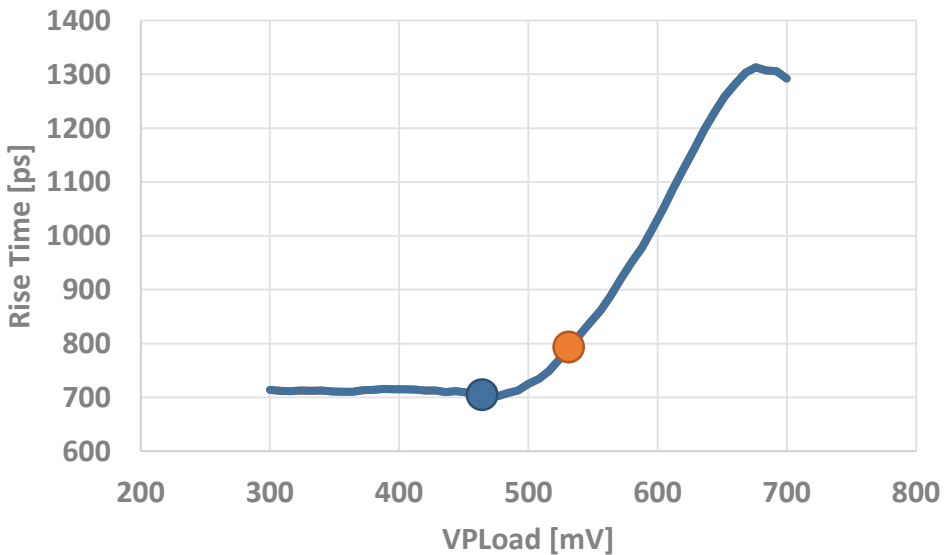
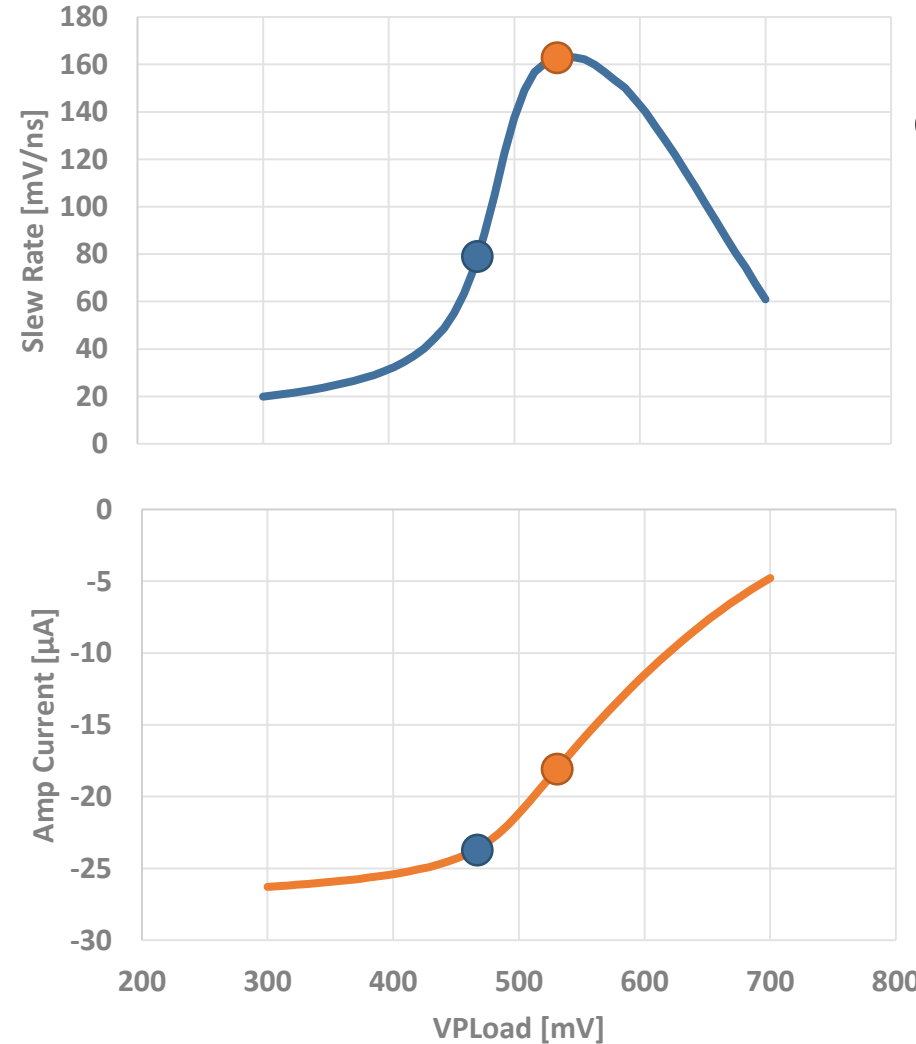
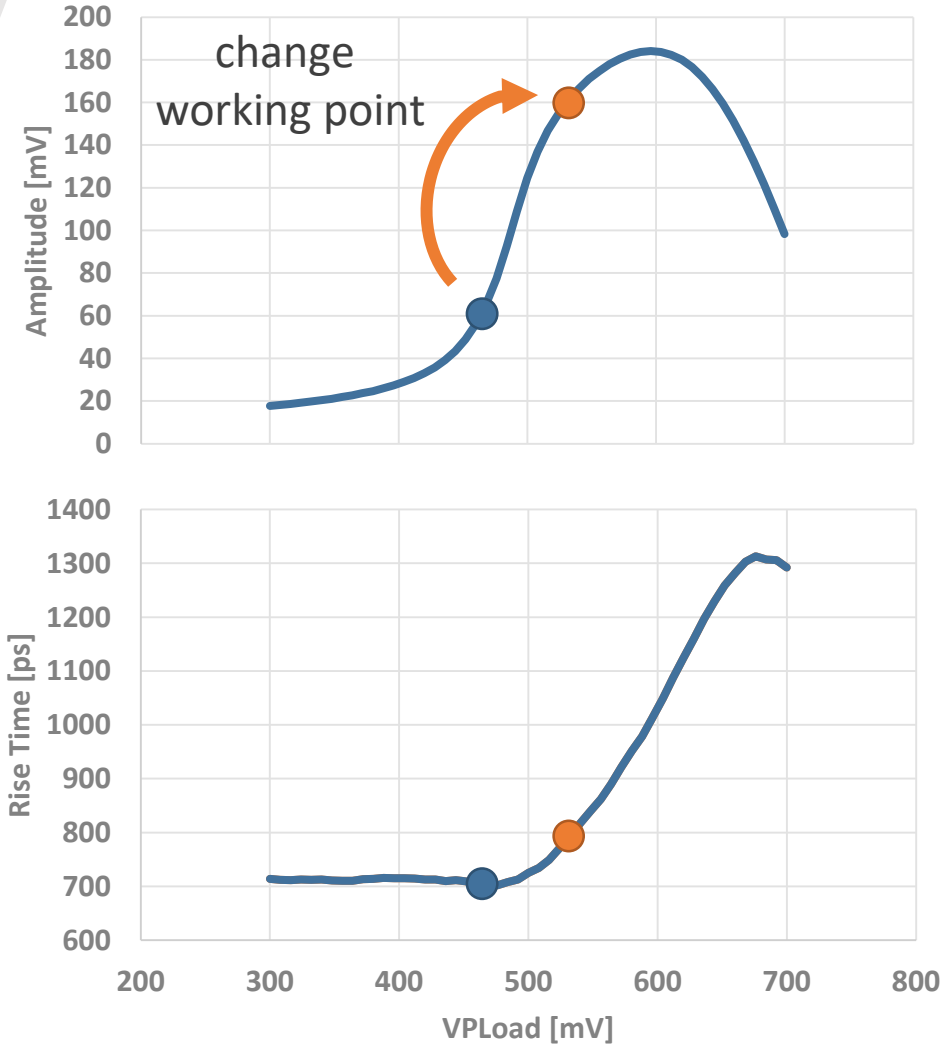
signal results in a $\sim 60\text{mV}$ voltage peak at the output

current signal defined in test bench results in a $\sim 3\text{mV}$ voltage drop at the input

amplifier current is not constant but only varies a few μA

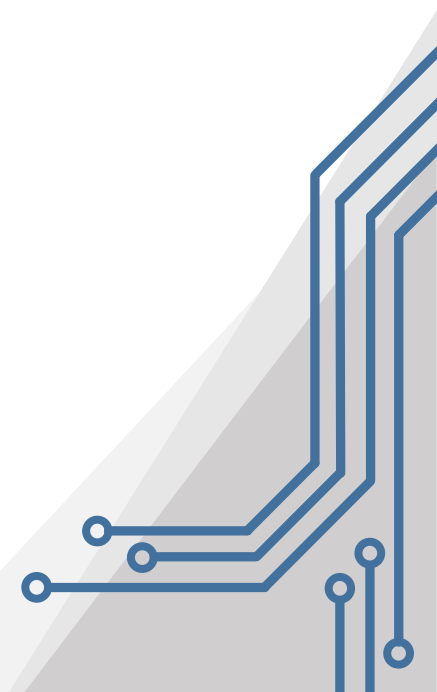


Transient Simulation – Parametric Sweep

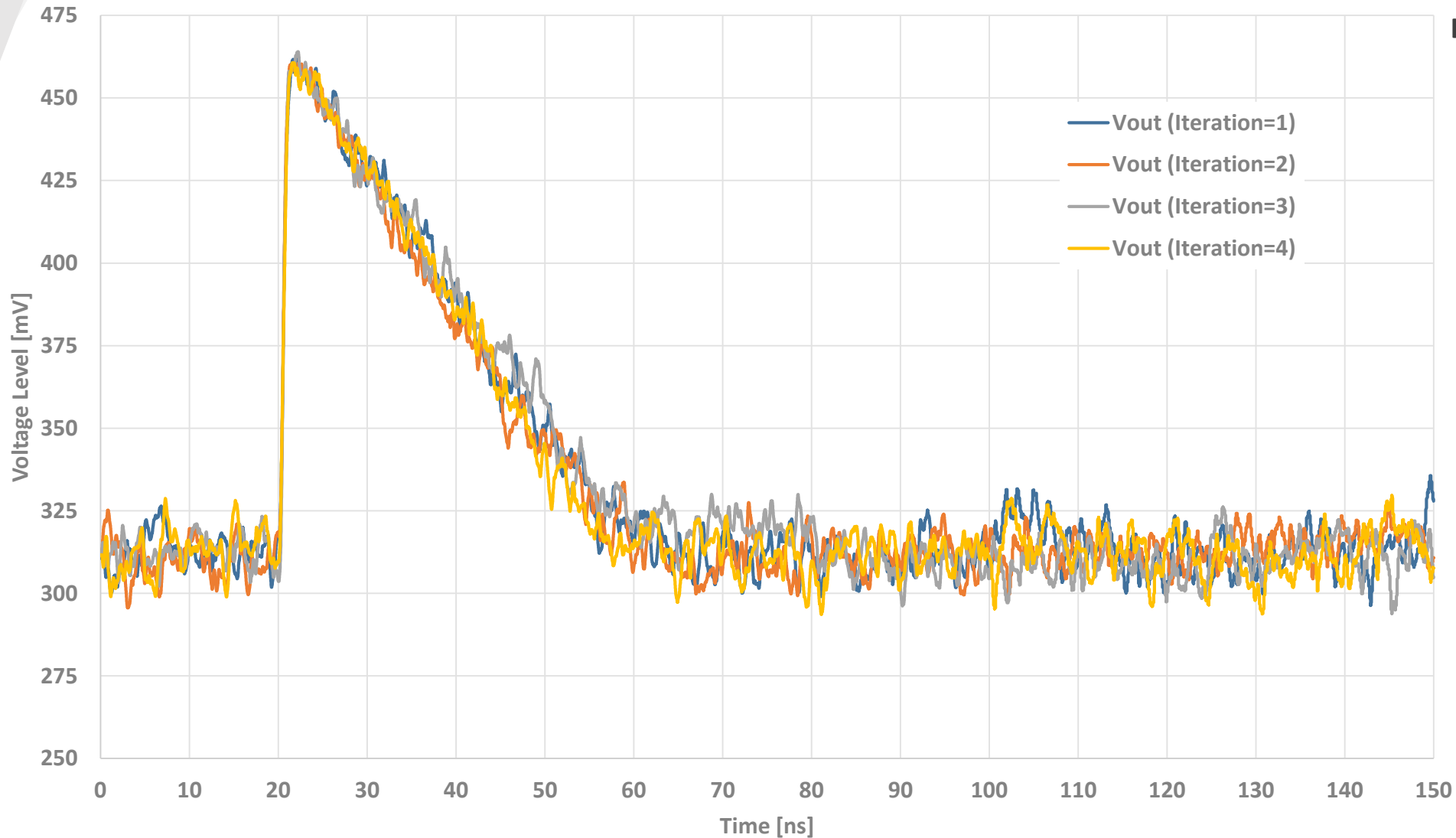


useful to find good operation points:

combine with expressions to observe important parameter



Transient Simulation – influence of noise

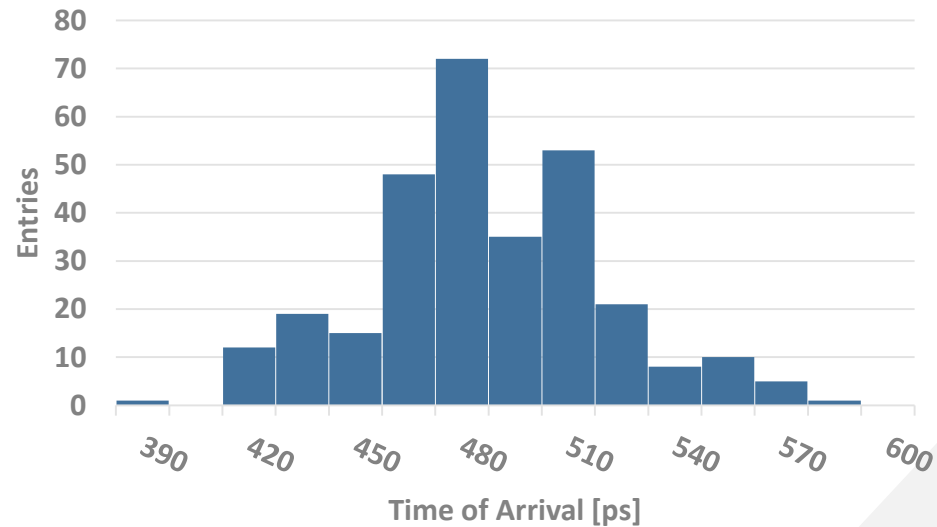
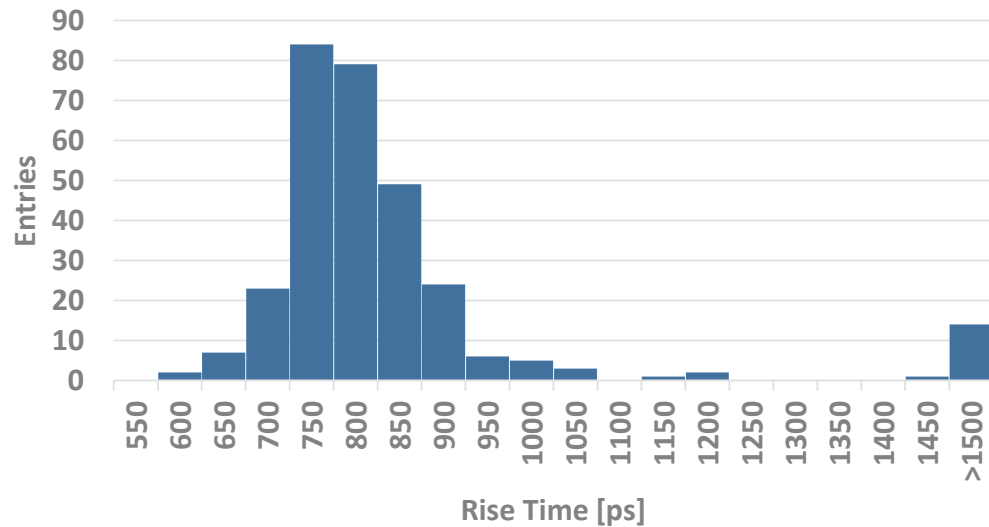
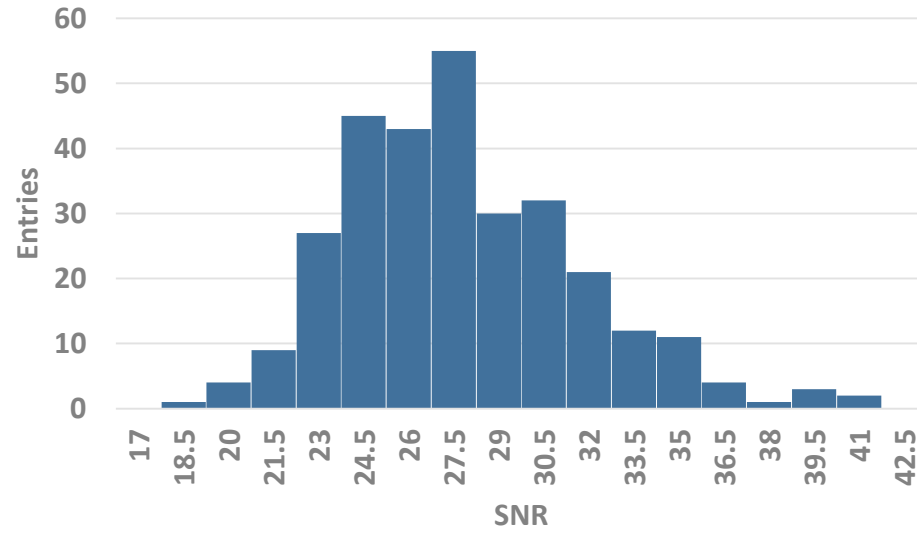
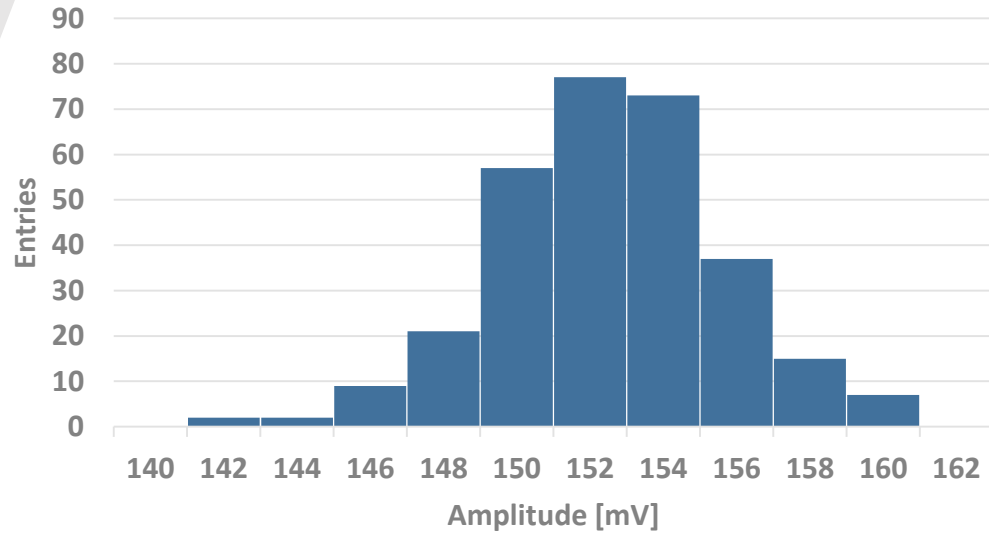


possibility to introduce noise into the simulation:

requires significantly more time

opens up the possibility to investigate various important parameters

Transient Simulation – influence of noise





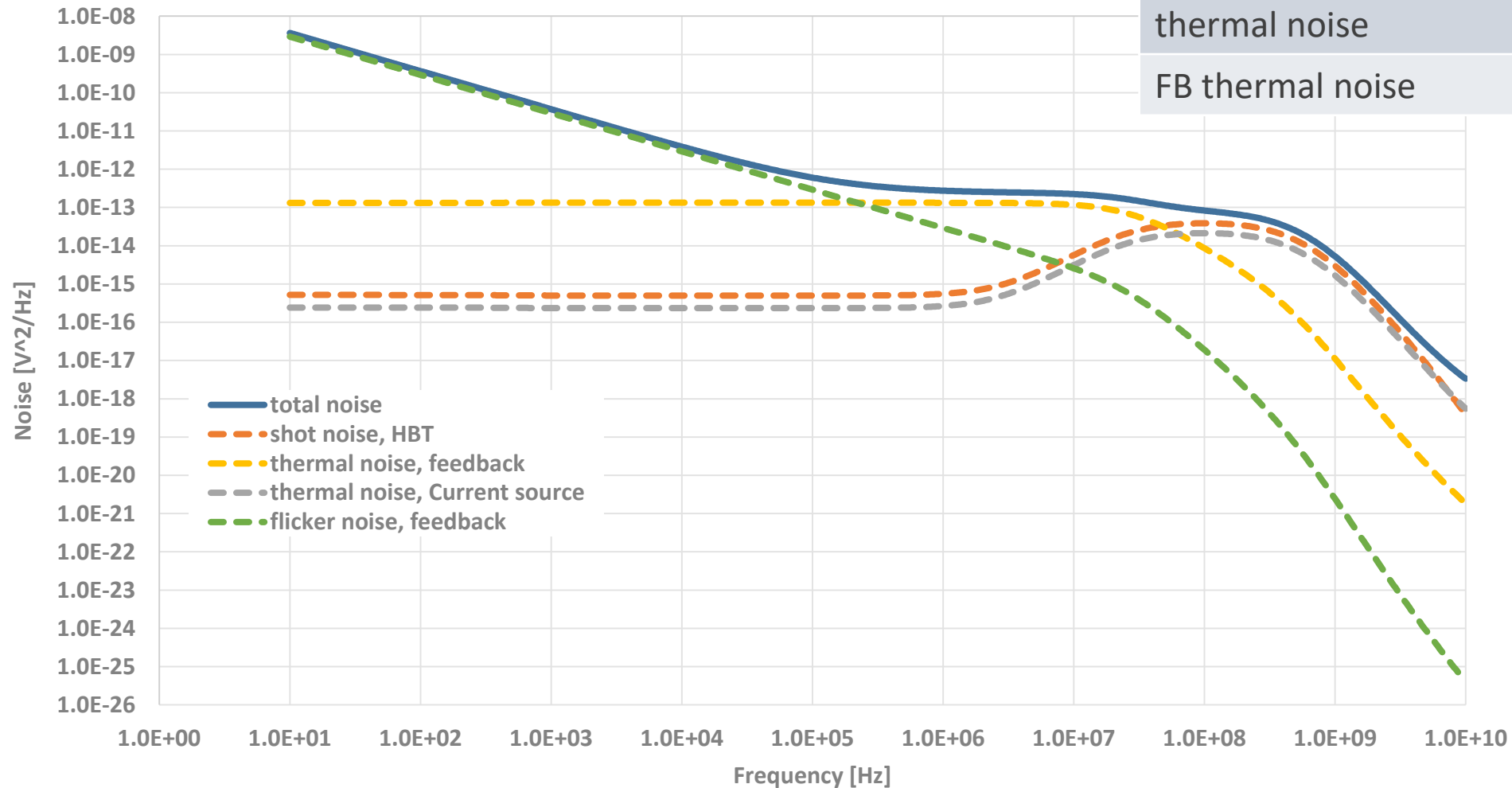
Noise Simulation

- ↳ transient simulation with noise is slow

→ dedicated noise simulation

- ↳ gives access to several different noise types for each part
 - ↳ indicate large noise contributors
- 

Noise Simulation

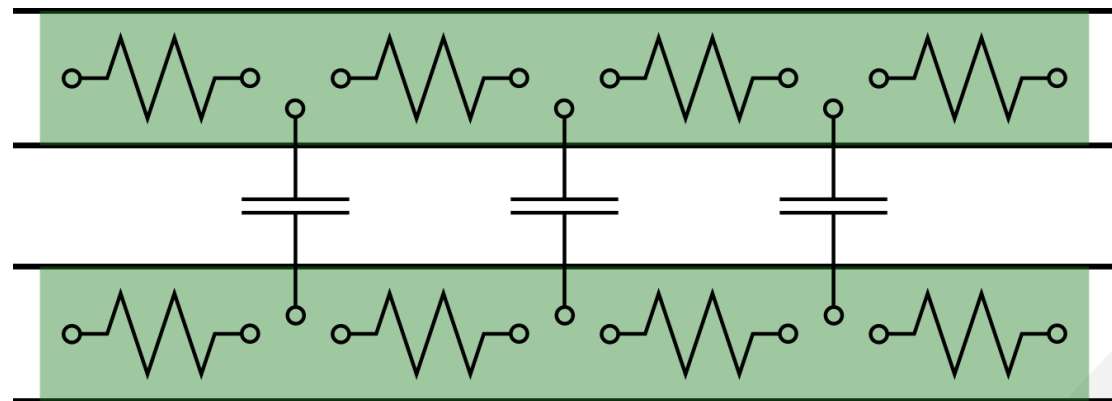


noise type	integrated noise
Total noise	6.47 mV
HBT shot noise	4.26 mV
Current source thermal noise	3.18 mV
FB thermal noise	2.30 mV

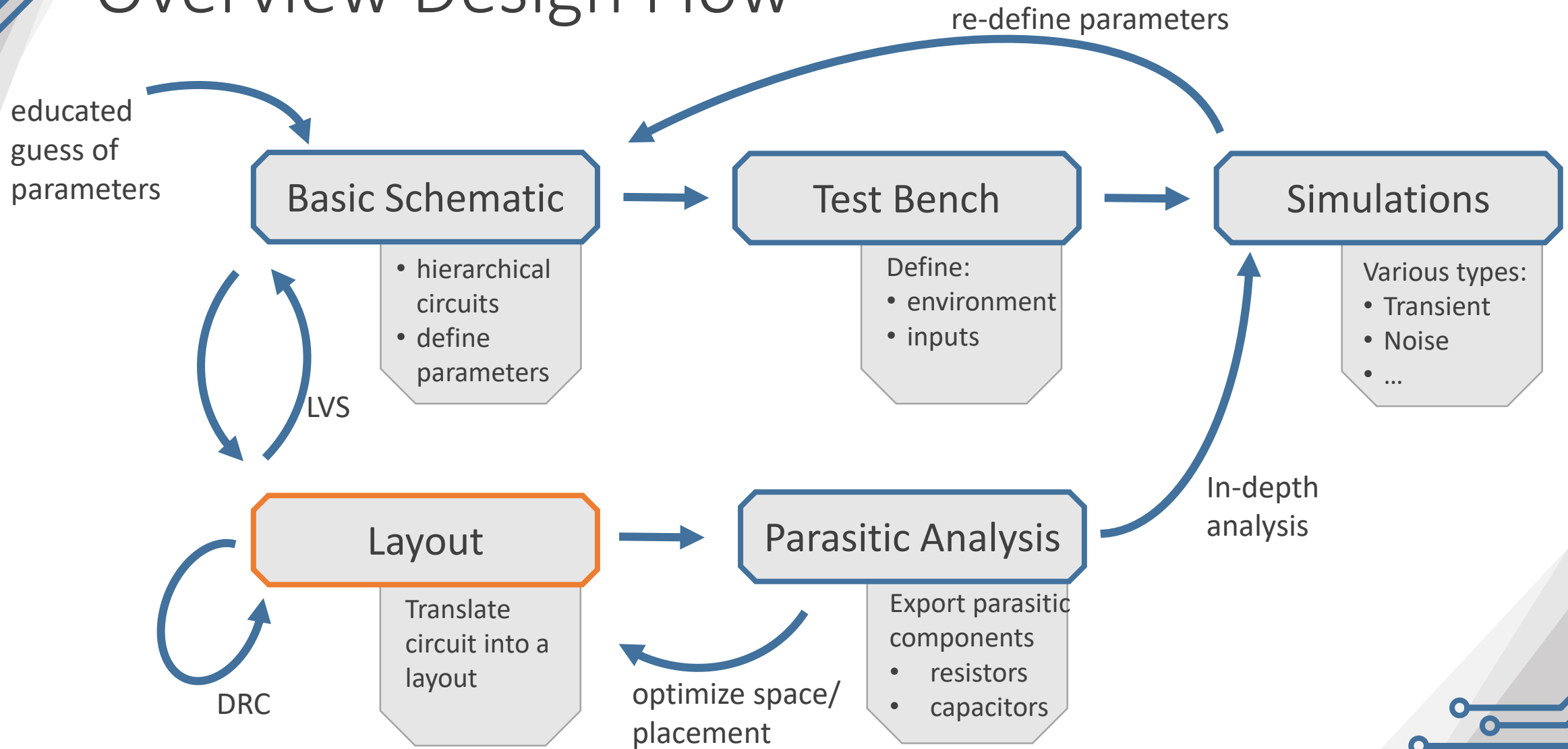
Parasitic Simulations

- till now: only transistor models are simulated
 - including internal capacities
- for the physical representation of the circuit non-ideal traces are needed
 - add parasitic resistance/ capacities
 - degrade circuit performance

→ layout is required

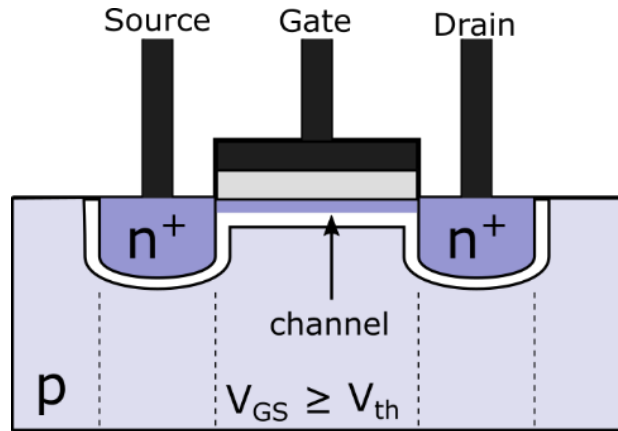
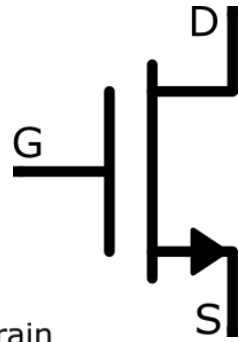


Overview Design Flow

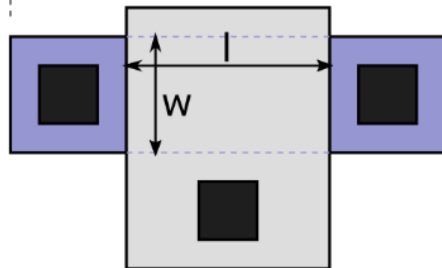


NMOS

N-channel device

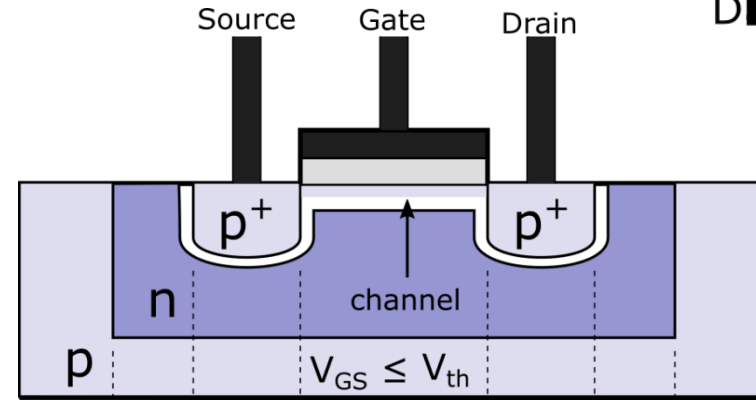
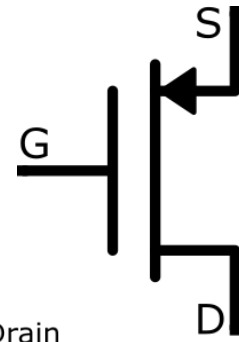


$$V_{DS} < V_{GS} - V_{TH}$$

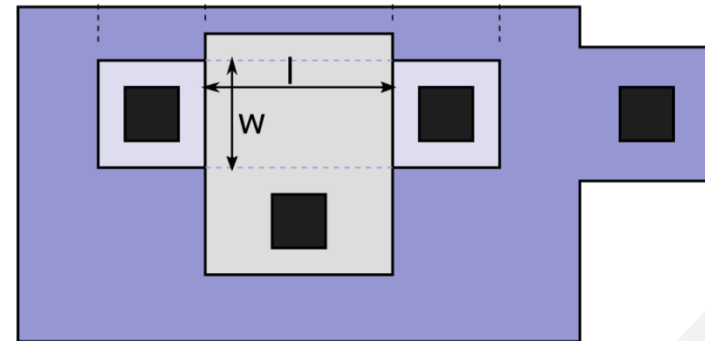


PMOS


P-channel device



$$V_{DS} > V_{GS} - V_{TH}$$



Layout

- layers define physical layers on chip
 - shapes in  define n-doped area
- possible to use std. cells for transistors, ...



n-well



p-well



buried n-well



high doping area



gate poly silicon



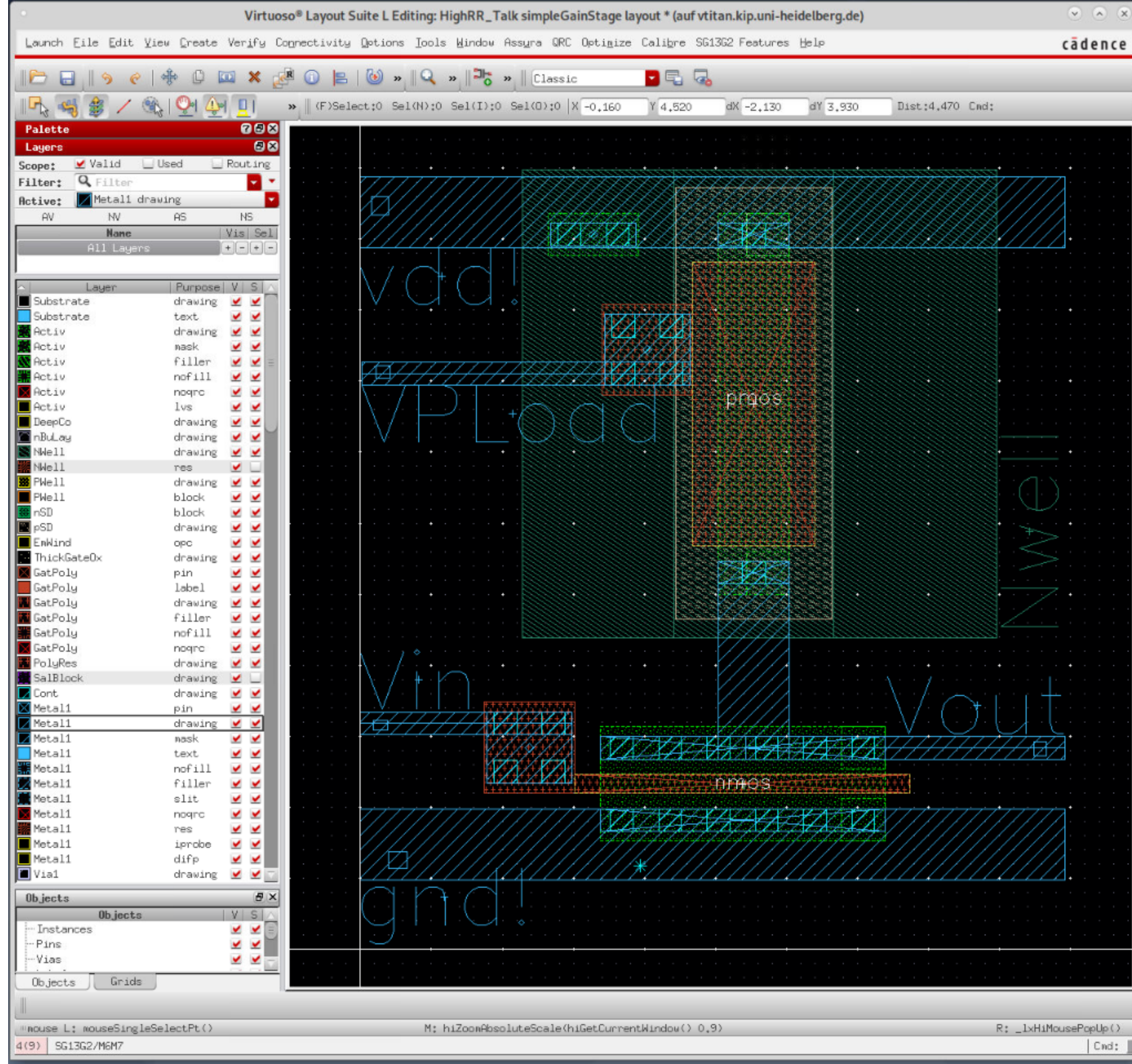
metal 1



metal 2











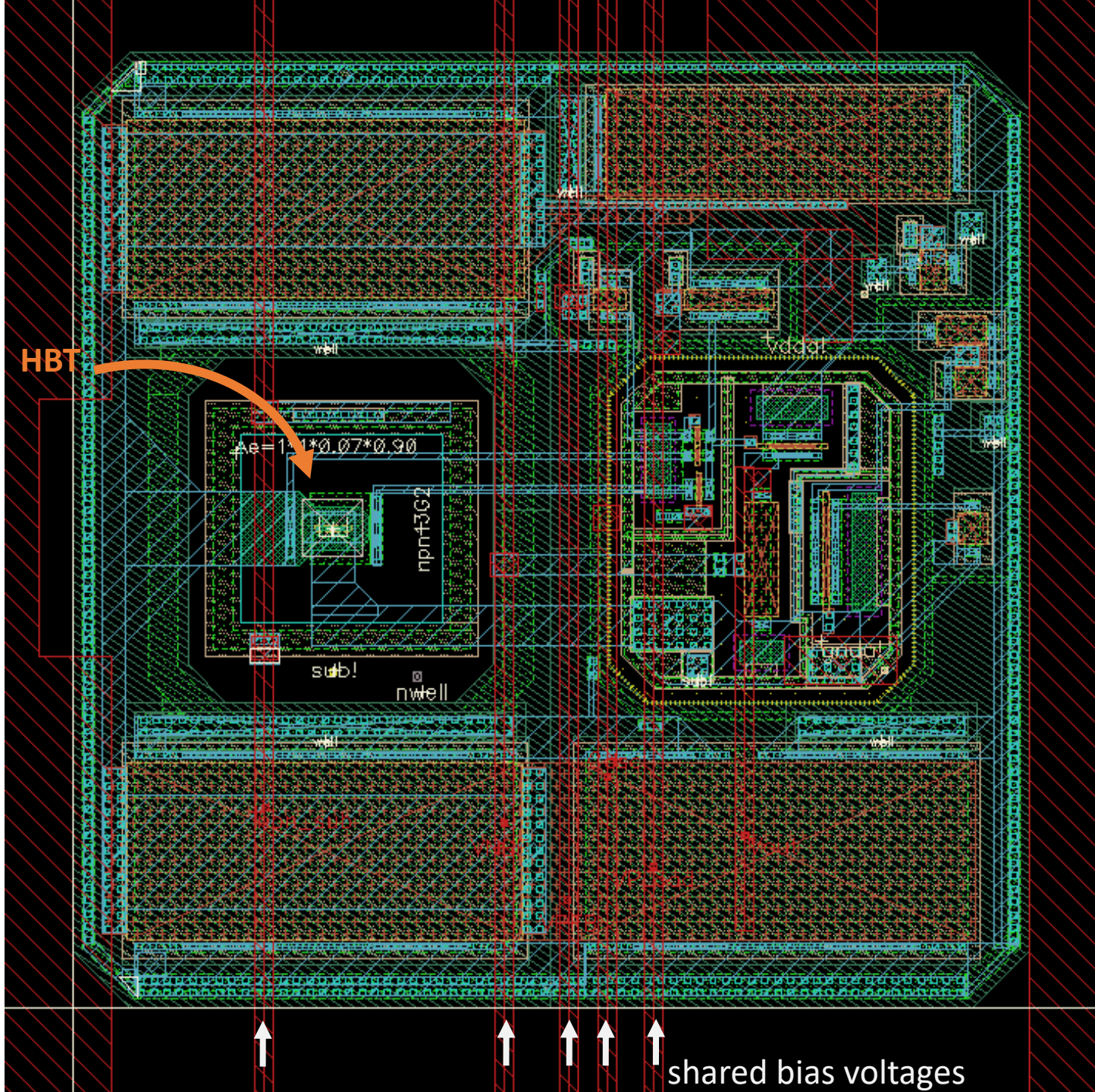
device boundary



Pixel Layout

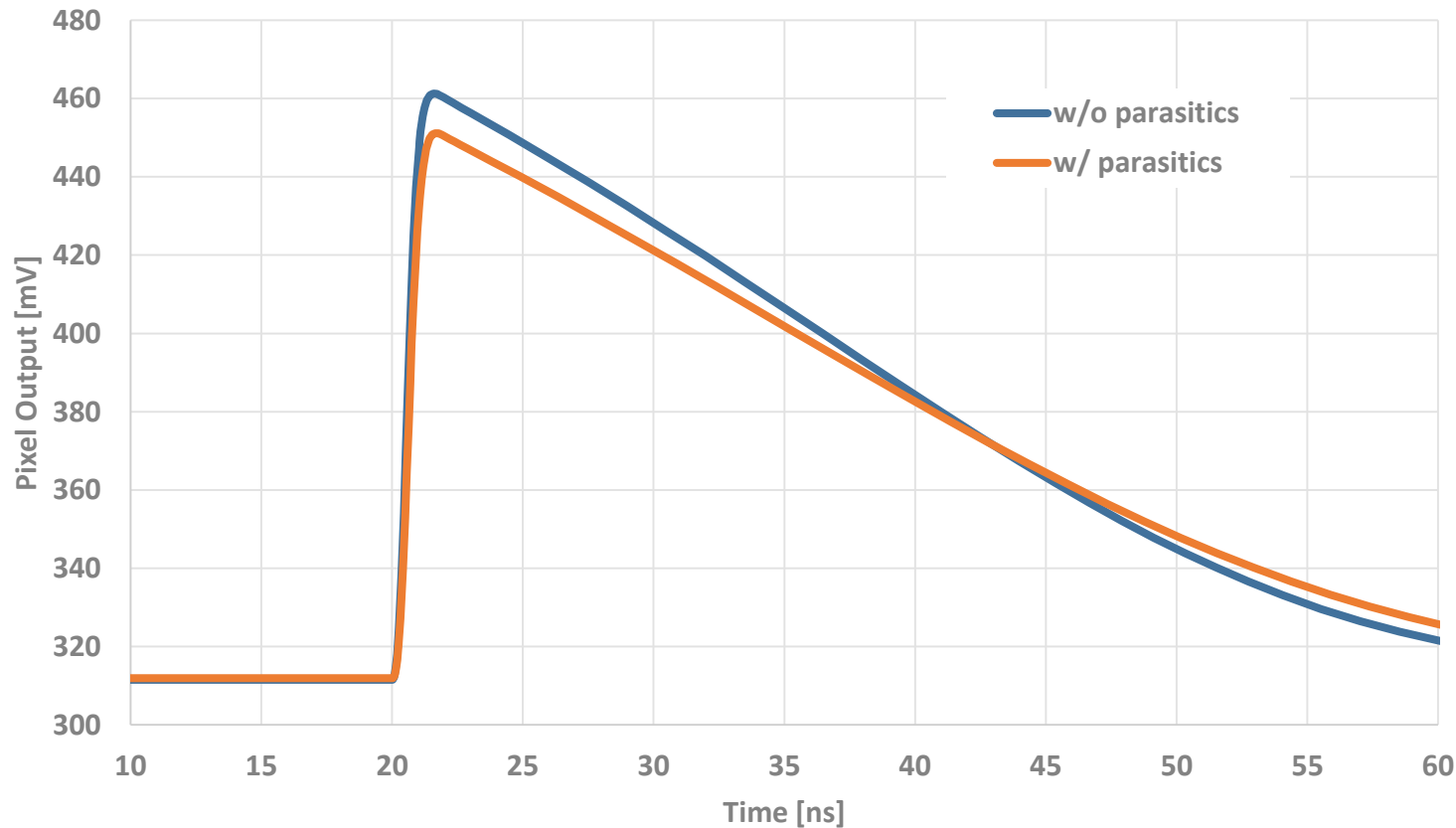
- implant size $26 \times 26 \mu\text{m}^2$
- pixel size $41 \times 41 \mu\text{m}^2$
- HBT in separated p-well with double guard ring
- minimized parasitic capacities
 - avoid overlapping metal areas
- shared bias voltages for all pixels

	n-well		gate poly silicon
	p-well		metal 1
	buried n-well		metal 2
	high doping area		device boundary



Parasitic Simulation

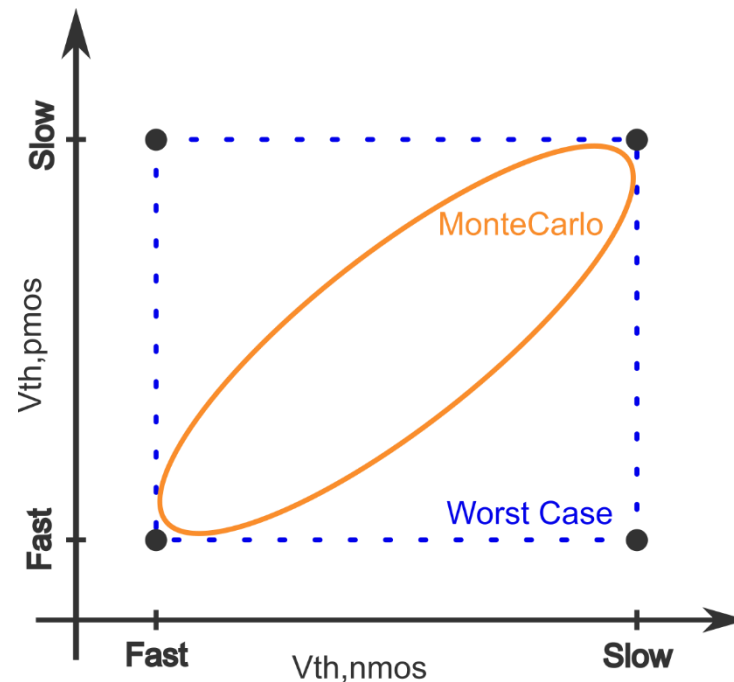
parameter	w/o parasitics	w/ parasitics
Amplitude	149.8 mV	139.2 mV
Rise Time	741.2 ps	789.4 ps
Slew Rate	161.7 mV/ns	141.1 mV/ns
ToA	480 ps	540 ps



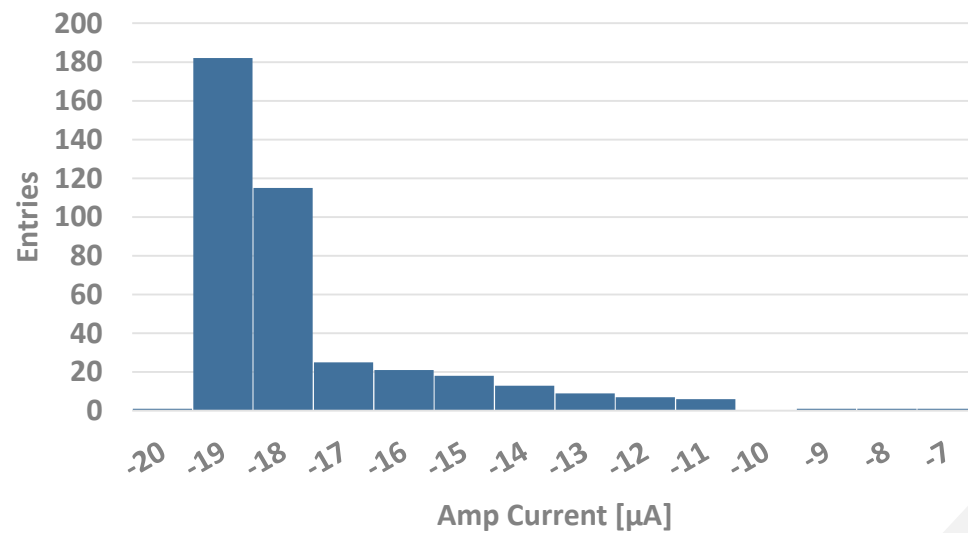
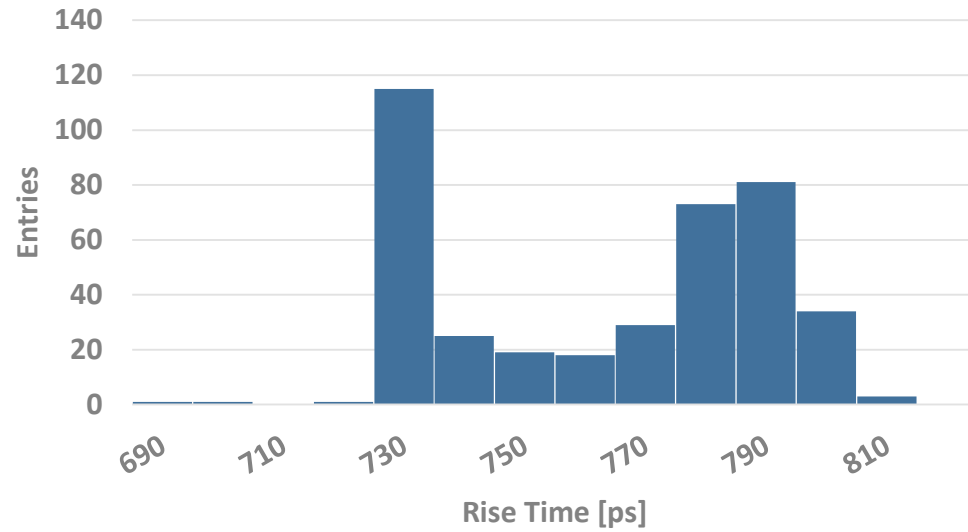
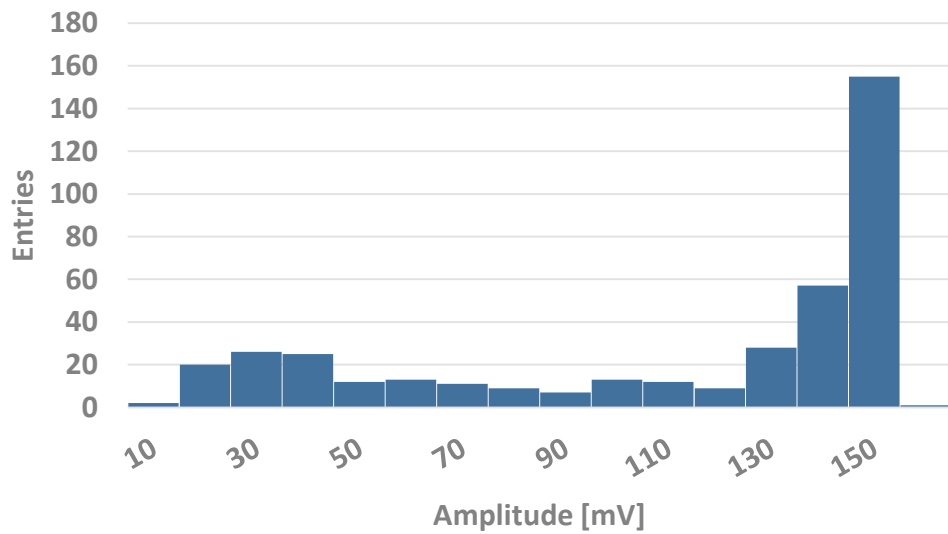
- not possible to extract parasitic from large layouts
- identify important parasitics and use an estimation
 - e.g. long lines between pixel and periphery

Monte Carlo Simulation

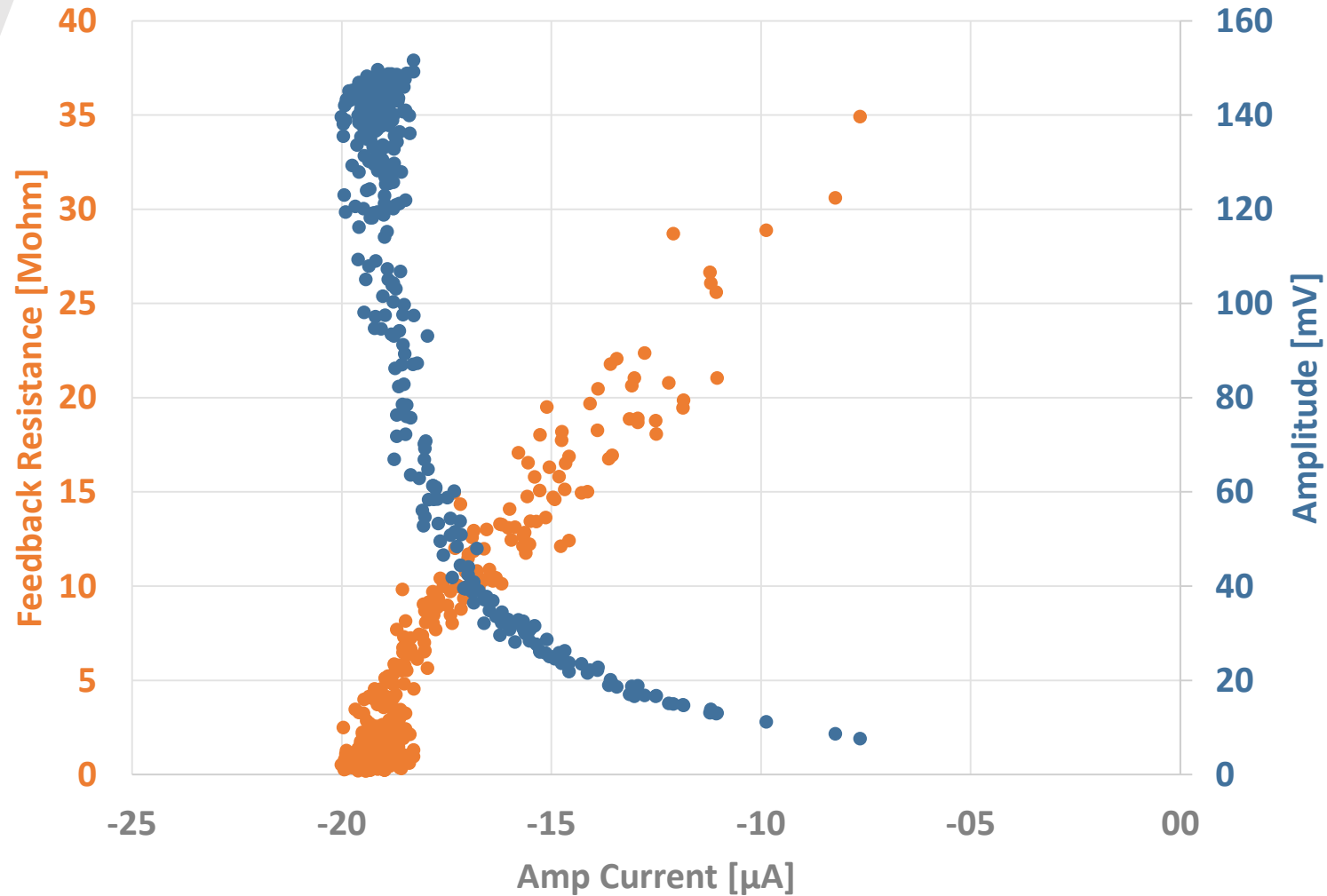
- Statistic analysis of the circuit performance
 - ..depending on global process parameters
 - ..depending on local device parameters (mismatch)



Monte Carlo Simulation – mismatch



Monte Carlo Simulation



- clear correlation between Amp/R_f – Current
- large values of R_f result in a higher output level -> decrease dynamic range
- change working point

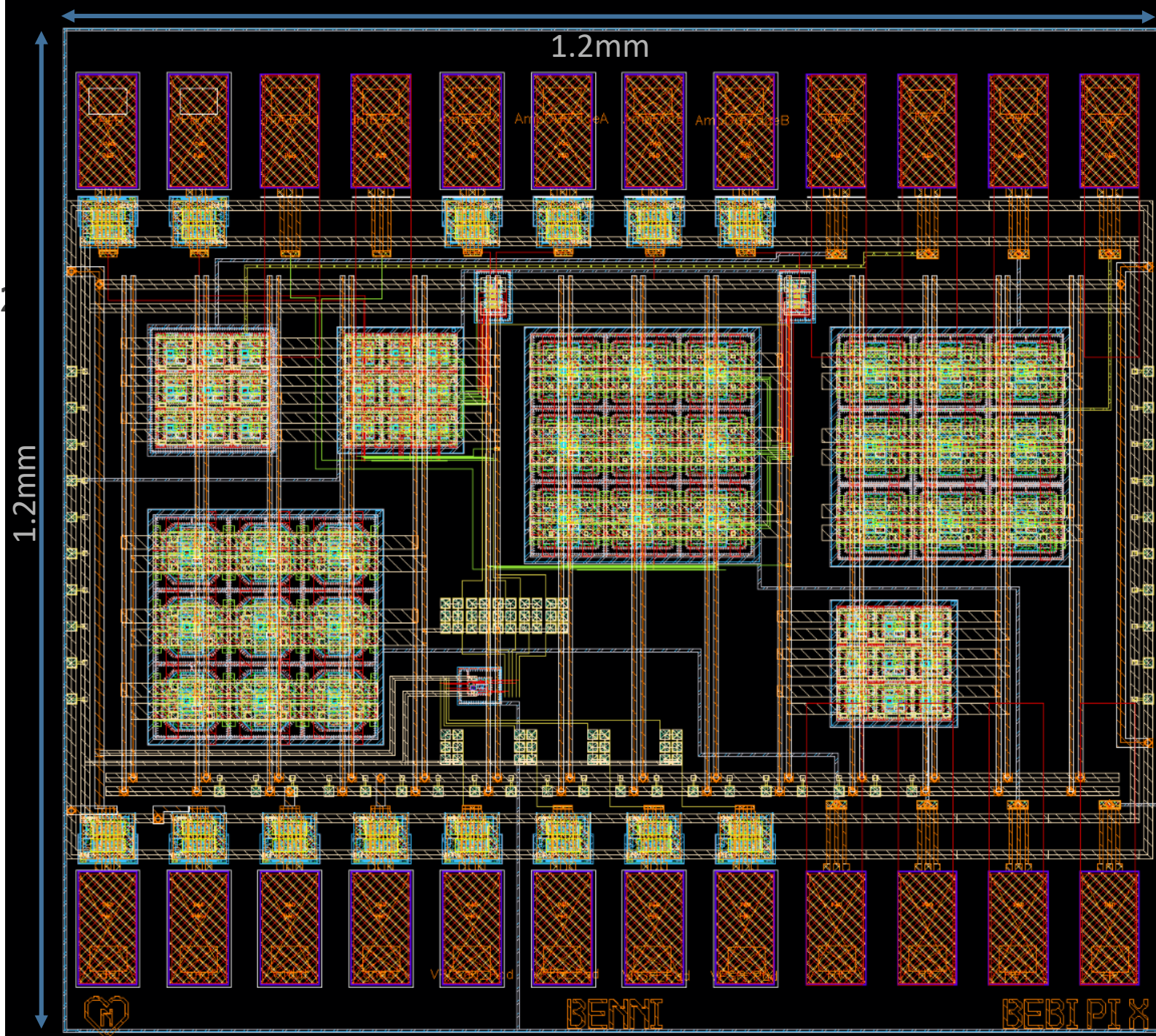
Monte Carlo Simulation – Worst Point

- examine worst point in mismatch simulation
 - use bias voltages to optimize working point

	Old Working Point	New Working Point	Ideal Working Point
Amplitude	7.63 mV	115.0 mV	149.8 mV
Rise Time	734.5 ps	1198 ps	741.2 ps
Slew Rate	8.31 mV/ns	76.8 mV/ns	161.7 mV/ns

BeBiPix

- Size: $\sim 1.2 \times 1.2 \text{ mm}^2$
- 24 Pads
 - 4 supply voltages
 - 4 bias voltages
 - 2 sense wires
 - 2 injections
 - 4 outputs
 - 8 HV connections



BeBiPix

- featured structures:
 - 2 functional 3x3 matrices
 - 4 test structures
 - bias block
 - analogue output cell

