# **Evaluating Portable Parallelization Strategies for Heterogeneous Architectures**

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Portable	Paralle	elizatio	on APIs	and Lar	nguages			Metrics	Perfo
<ul> <li>Kokkos: A execution of accelerator</li> <li>SYCL: A s Implementa different are execution of alpaka: Ha control of h</li> <li>std::execut parallel task full integrat</li> </ul>	A C++ of the co archited specifica ations an chitectu Compi on differe eader or hardware <b>ition::p</b> ks. Still	abstraction and addition for a provision for a	tion layer data mai r a cross- ded by dif ctive-base t and acc allel abstra ting CPU lel C++ s developme	(library) nagement platform fferent ve d progran elerator a action lib s, GPUs standards	that sup t for diffe C++ ab endors/or mming m architectu rary that and FPG s based a	oports par erent host straction ganizatio nodel for ures. provides SAs opproach t	t and layer. ns to support parallel low level	<ul> <li>Ease of Learning <ul> <li>novices, C++ developers, GPU experts</li> </ul> </li> <li>Code conversion <ul> <li>CPU → GPU, API → API</li> </ul> </li> <li>Extent of modifications to existing code <ul> <li>Control of main, threading/execution model</li> </ul> </li> <li>Extent of modifications to EDM / Data</li> </ul> <li>Extent of modifications to build rules / system</li> <li>Hardware Mapping <ul> <li>current and promised future support of hardware</li> </ul> </li> <li>Feature Availability <ul> <li>reductions, kernel chaining, callbacks, concurrency</li> </ul> </li> <li>Address needs of large and small workflows</li> <li>Long term sustainability and code stability</li>	Fa 4 4 4 4 4 4 4 4 4 4 4 4 4
NVidia GPU AMD GPU Intel GPU Multicore CPU FPGA Experime	ent Tes			feature complete for select GPUs native and via OpenMP target offload	codeplay and intel/llvm	via SYCL	nvc++ oneAPI::dpI g++ & tbb	<ul> <li>backward/forward compatibility of API and eg CUDA</li> <li>Compilation time</li> <li>Run time <ul> <li>what happens to original CPU code</li> </ul> </li> <li>Ease of Debugging</li> <li>Aesthetics <ul> <li>beauty is in the eye of the beholder</li> </ul> </li> <li>Interoperability <ul> <li>interaction with externals, thread pools, c++ standards</li> </ul> </li> </ul>	
<ul> <li>FCS – Fast</li> <li>Patatrack (</li> <li>p2r (CMS):</li> <li>ACTS track</li> </ul>	CaloSin (CMS): Propag king wor	n (ATL/ Silicon gate to	AS): Para pixel trac R track f	metrized ker recon ollower	LAr Cal Instruction e track fi	orimeter S	Simulation	needs explicit init/finalize though recor	m same sourd npilation or npiler versions

	Kokkos	SYCL	OpenMP	std::par	a
WireCell			WIP	desired	s
FastCaloSim			WIP		
Patatrack		WIP	WIP	WIP	
p2R					
ACTS	partial	partial		partial	

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- stretch
- NIP

Iong templates make

need to explicitly define

backends at compilation

no generic use of concurrent

strong developer community

and prompt backend support

debugging hard

well established

kernels

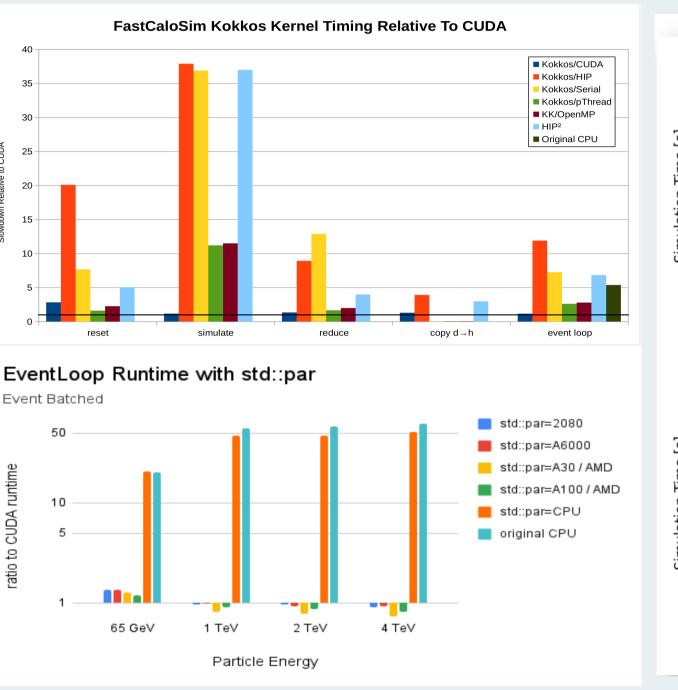


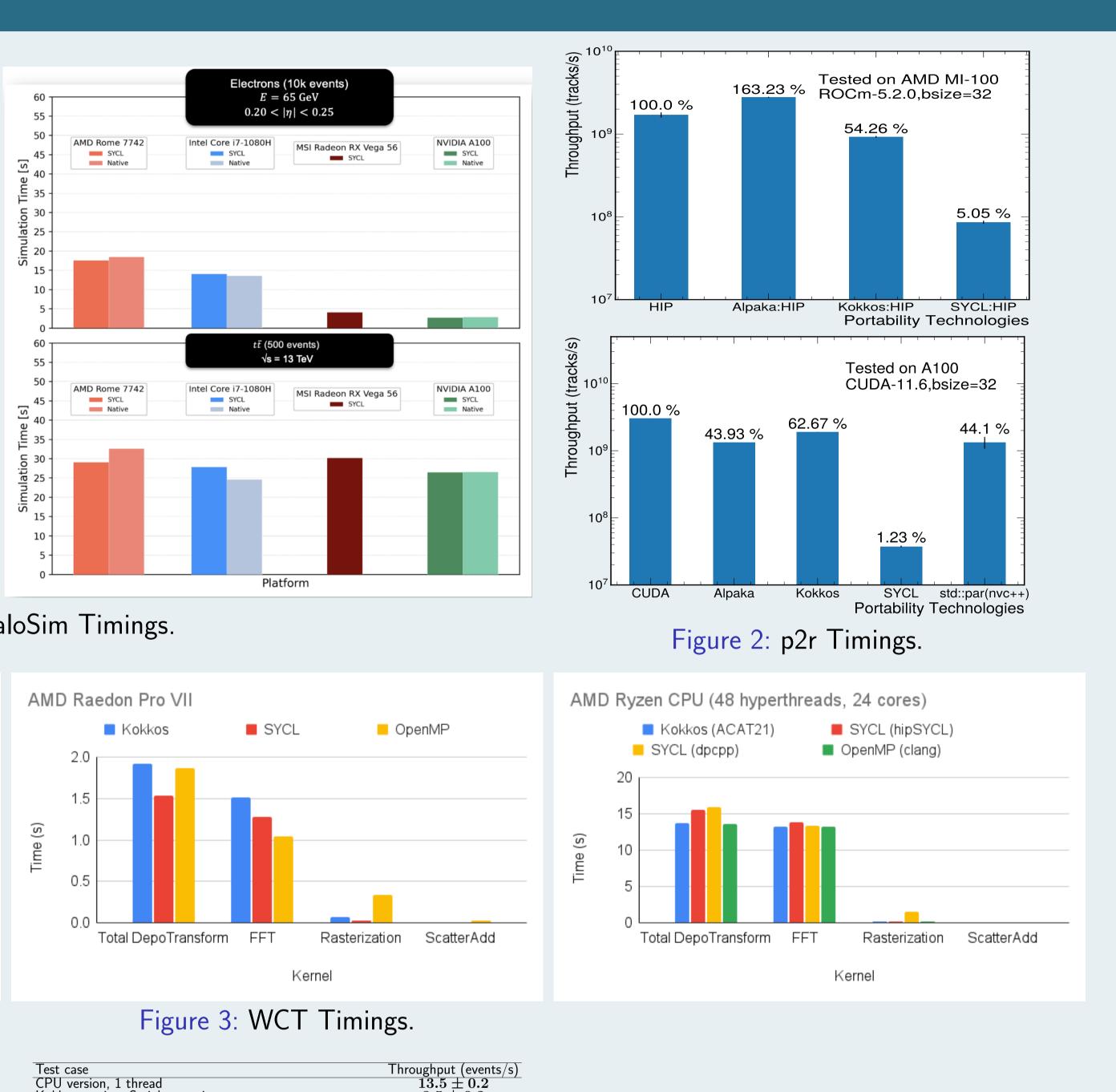
C++ standards

buffers

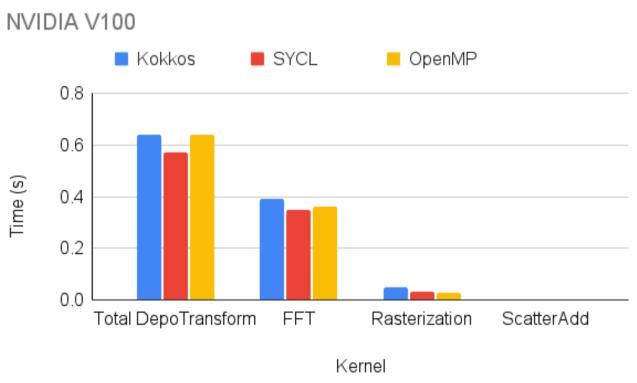


## **Performance Studies**





## Figure 1: FastCaloSim Timings.



Test case	Throughpu
CPU version, 1 thread Kokkos version, Serial execution space	13.5
Kokkos version, Serial execution space	<b>8.5</b>
CPU version, 40 threads	539
Kokkos version, Threads execution space, peak (18 threads)	<b>28</b>
CUDA version, peak (9 concurrent events and CPU threads)	1840
CUDA version, 1 concurrent event	720
CUDA version, 1 concurrent event, memory pool disabled	159
Kokkos version, CUDA execution space	115.7
Table 1: Patatrack Tim	ings

ware ne source, ion or versions

more verbose than CUDA, but similar to Kokkos for memory management when using

callbacks may not be supported in future, no concurrent kernels

good cmake integration strong support by Intel, pushing towards integration in

# **OpenMP**

- easy to implement, does not require major changes to the C++ code
- performance varies from compiler to compiler
- specialized operations (e.g. atomic) less performant than CUDA
- does not support GPU scan operation
- under active development
- architecture agnostic compiler directives can offload to multiple GPUs, FPGAs

# std::par

- plain C++ low developers
- cannot access low features
- memory transfers USM
- unless kernels have thrust counterpar performant as CL
- no asynchronous
- no ability to spec execution parame (block/grid size)
- compilers still und
- development, can
- $\blacksquare C++$  standards c



 $\begin{array}{c} \mathsf{put}\;(\mathsf{events/s})\\ 5\pm0.2\\ 5\pm0.2\\ 39\pm9\\ 28\pm1\\ 40\pm20\\ 20\pm20\\ 59\pm1\\ ..7\pm0.3\end{array}$ 

	alpaka
entry bar for w level GPU s restricted to ve a direct rt, not as UDA operations cify kernel eters	<ul> <li>Header-only C++ library</li> <li>Single-source programming model (kernels are embedded in application code)</li> <li>At compilation alpaka kernels are transformed into native kernels. Achieves compatibility with the vendor ecosystem (e.g., debugging tools)</li> <li>Low-level and powerful API. Not always super-intuitive</li> <li>Heavy usage of C++ template meta-programming. The application code tends to be quite verbose</li> </ul>

