Contribution ID: **226** Type: **Poster**

Implementation of the Cluster Counting and Timing realtime algorithm on FPGA to improve the impact parameter estimates of the Drift Chamber and particle identification.

Thursday, 27 October 2022 11:00 (30 minutes)

Ultra-low mass and high granularity Drift Chambers fulfill the requirements for tracking systems of modern High Energy Physics experiments at the future high luminosity facilities (FCC-ee or CEPC).
\indent We present how, in Helium based gas mixtures, by measuring the arrival times of each individual ionization cluster and by using proper statistical tools, it is possible to perform a bias free estimate of the impact parameter and a precise PID. Typically, in a helium-based drift chamber, consecutive ionization clusters are separated in time by a few ns, at small impact parameters up to a few tens of ns, at large impact parameters. For an efficient application of the cluster timing technique, consisting in isolating pulses due to different ionization cluster, it is, therefore, necessary to have read-out interfaces capable of processing high speed signals. We present a full front-end chain, able to treat the low amplitude sense wire signals (a $\sim$few mV), converted from analog to digital with the use of FADCs, with a high bandwidth ($\sim$1 GHz). The requirement of high sampling frequency, together with long drift times, usually of the order of several hundreds of ns, and large number of readout channels, typically of the order of tens of thousand, impose a sizable data reduction, meanwhile preserving all relevant information. Measuring both the amplitude and the arrival time of each peak in the signal associated to each ionization cluster is the minimum requirement on the data transfer for storage to prevent any significant data loss. An electronic board including a Fast ADC and an FPGA for a real-time processing of the drift chamber signals is presented. Various peak finding algorithms, implemented and tested in real time with VHDL code, are also compared.

Significance

This project, by immediately digitizing the signals of the drift chamber, respecting the performance requirements, imposes conversions at high sampling rates with high resolution. These constraints, together with maximum drift times and with a large number of readout channels, impose some sizable data reduction, preserving all relevant information. Measuring both the amplitude and the arrival time of each peak in the signal associated to each ionization cluster is the minimum requirement on the data transfer for storage to prevent any data loss.

References

-The use of FPGA in drift chambers for data transfer rate reduction", Journal of Instrumentation 15 (2020) C09058 , doi:10.1088/1748-0221/15/09/C09058;
-https://agenda.infn.it/event/22092/contributions/166648/

Experiment context, if any

it will be used in the IDEA drift chamber and it is WP of AidaINNOVA

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Session Classification: Poster session with coffee break

Track Classification: Track 2: Data Analysis - Algorithms and Tools