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The European Processor Initiative (EPI), an status update

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The European Processor Initiative (EPI) is an EU-funded project that aims to develop and implement a new family of European processors for high performance computing, artificial intelligence, and a range of emerging application domains. A variety of processor technologies are being implemented as part of EPI. They are divided into two main development lines: the General Purpose Processor (GPP) and the European Processor Accelerator (EPAC).
The first CPU from the GPP line – Rhea1, a multi-core processor using the Arm Neoverse V1 architecture –, will be commercialised by SiPEARL SAS. The Rhea1 architectural specifications have been determined via co-design using typical HPC applications and benchmarks. Rhea1 will integrate core technologies from several EPI partners and offers unique features in terms of memory architecture, memory bandwidth optimisation, security and power management. Amongst others, it includes High Bandwidth Memory (HBM2) and a scalable network-on-chip (NoC) that enables high-frequency, high-bandwidth data transfers between cores, accelerators, input/output (IO) and shared memory resources.
The EPI accelerator line uses the open-source RISC-V Instruction Set Architecture (ISA) to deliver energy-efficient acceleration for HPC and AI workloads. The EPAC v1.0 test chip is the first proof-of-concept of the EPI accelerator stream, which has fully embraced the open-source philosophy by contributing to the expansion of the RISC-V ecosystem, extending the LLVM compiler codebase and providing new patches, drivers and features for the Linux operating system, OpenMP and MPI. In addition, parts of the accelerator hardware such as the STX (Stencil/Tensor accelerator) have been developed using an open source approach with free licensing on the PULP platform.
The GPP and EPAC streams are complemented by a number of joint activities, including a co-design process to design the EPI processors. Simulations and models of varying levels of detail and precision have been produced to determine the impact of design decisions on the performance of future applications. A benchmark suite containing over 40 applications is used in support of co-design and subsequent evaluation of the EPI processors. The applications are also prepared for use on future EPI systems by adapting and testing them on comparable hardware platforms and emulators.
This talk will describe the main developments of the EPI project and present their current status and roadmap.

Experiment context, if any

References

Significance

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