Contribution ID: **300** Type: **Poster**

A FPGA Implementation of the Hough Transform tracking algorithm for the Phase-II upgrade of ATLAS

Monday 24 October 2022 16:10 (30 minutes)

The High Energy Physics world will face challenging trigger requests in the next decade. In particular the luminosity increase to 5-7.5 x 1034 cm-2 s-1 at LHC will push the major experiments as ATLAS to exploit the online tracking for their inner detector to reach 10 kHz of events from 1 MHz of Calorimeter and Muon Spectrometer trigger. The project described here is a proposal for a tuned Hough Transform algorithm implementation on FPGA high-end technology, versatile to adapt different tracking situations. The platform developed allows to study different dataset from a software "emulating"the firmware and consequently to the hardware performance and to generate input dataset from ATLAS simulation. Xilinx FPGA have been destined to this implementation, exploiting up to now the VC709 commercial board and its PCI Express Generation 3 technology. The system provides the features to possibly process a 200 pile up event of ATLAS Run4 in the order of 10 μs averagely, with the possibility to run two events at a time. Best efficiency reached are simulated to be > 95 % for single muon tracking. The project plans to be proposed for the Event Filter TDAQ ATLAS Upgrade of Phase-II.

Experiment context, if any

The ATLAS experiment.

References

https://www.mdpi.com/2079-9292/10/20/2546
https://www.mdpi.com/2079-9292/11/4/517

Significance

These results are the updates of a FPGA tracking algorithm implementation forwarded
by the INFN Bologna group and stated in the ATLAS TDAQ Phase-II upgrade reports related to the Hardware Tracking for Trigger project.

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Session Classification: Poster session with coffee break