ACAT 2022



Contribution ID: 301

Type: Poster

Fast track seed selection for track following in the Inner Detector Trigger track reconstruction

Monday 24 October 2022 16:10 (30 minutes)

During ATLAS Run 2, in the online track reconstruction algorithm of the Inner Detector (ID), a large proportion of the CPU time was dedicated to the fast track finding. With the proposed HL-LHC upgrade, where the event pile-up is predicted to reach $\langle 1/_4 \rangle = 200$, track finding will see a further large increase in CPU usage. Moreover, only a small subset of Pixel-only seeds is accepted after the fast track finding procedure, essentially discarding the CPU time used on rejected seeds. Therefore, a computationally cheap track candidate seed preselection procedure based on approximate track following was designed, which is described in this report. The algorithm uses a parabolic track approximation in the plane perpendicular to the beamline, a combinatorial Kalman filter simplified by a reference-related coordinate system to find the best track candidates. For such candidates, a set of numerical features are created to classify seeds using machine learning techniques, such as Support Vector Machines (SVM) or kernel-based methods. The algorithm was tuned for high identification and rejection of bad seeds, while ensuring no significant loss of track finding efficiency. Current studies focus on implementing the algorithm into the Athena framework for online seed pre-selection, which could be used during Run 3 or potentially be adapted for the ITK geometry for Run 4 of the HL-LHC.

Experiment context, if any

The ATLAS experiment.

References

Significance

The presentation covers a new approach that could greatly reduce the overall CPU time consumption for the full-scan and large RoI tracking in the ATLAS Inner Detector. A separate algorithm is designed to be used for pre-filtering of track seeds before the combinatorial track following, so it could be used simultaneously with any other optimisation techniques used within the fast track finding algorithm. Reducing the CPU timing of the track finding is especially important for higher pile-up levels, and this algorithm is flexible and can be adapted to Run 4 ITk geometry.

Primary authors: VAITKUS, Andrius (University of London (GB)); HIGUCHI, Yu Nakahama (High Energy Accelerator Research Organization (JP))

Presenter: VAITKUS, Andrius (University of London (GB))

Session Classification: Poster session with coffee break