Implementation of the Cluster Counting and Timing realtime algorithm on FPGA to improve the impact parameter estimates of the Drift Chamber and particle identification.

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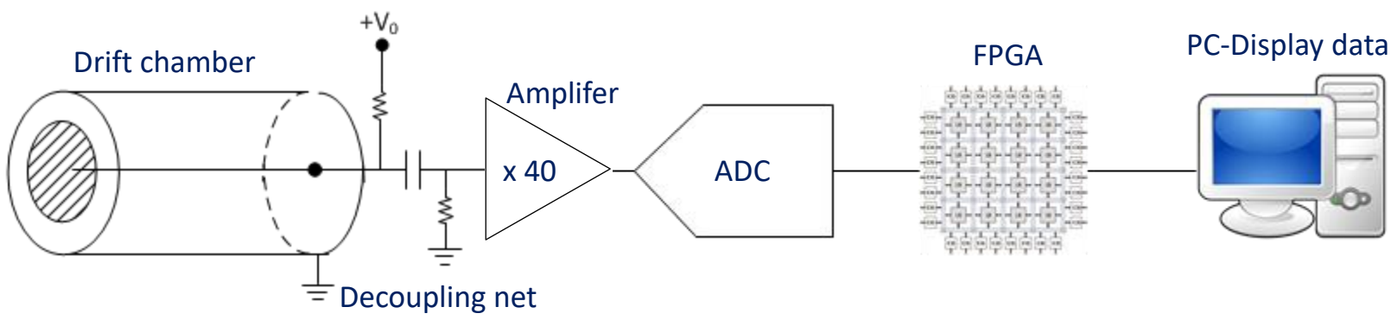
Abstract

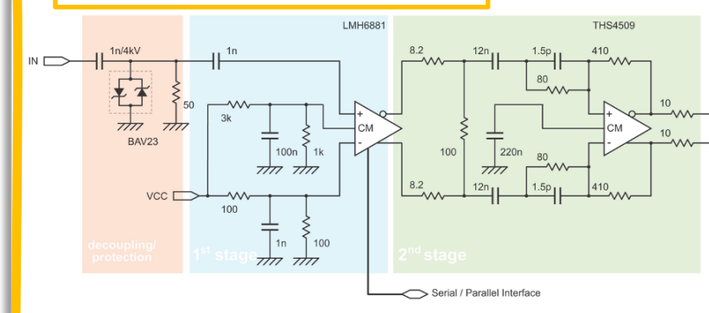
Ultra-low mass and high granularity Drift Chambers fulfill the requirements for tracking systems of modern High Energy Physics experiments at the future high luminosity facilities (FCC-ee or CEPC). We present how, in Helium based gas mixtures, by measuring the arrival times of each individual ionization cluster and by using proper statistical tools, it is possible to perform a bias free estimate of the impact parameter and precise particle identification. Typically, in a helium-based drift chamber, consecutive ionization clusters are separated in time by a few ns, at small impact parameters up to a few tens of ns, at large impact parameters. For an efficient application of the cluster timing technique, consisting in isolating pulses due to different ionization cluster, it is, therefore, necessary to have read-out interfaces capable of processing high speed signals. We present a full front-end chain, able to treat the low amplitude sense wire signals (a ~few mV), converted from analog to digital with the use of high bandwidth (~1 GHz) FADCs and an electronic board including an FPGA for a real-time processing of the signals.

Cluster counting/timing operation

The Cluster Timing Technique (CTT), which consists in measuring the arrival times on the sense wires of each individual ionization electron, overcomes a substantial bias in the impact parameter estimate (normally in drift chambers, only the time of the first cluster is used to estimate the track impact parameter) and offers the possibility of greatly improving the particle identification capabilities (Cluster Counting Technique, CCT). This technique uses statistical tools to reduce the biased estimate, by exploiting the information of all clusters detected with a peak finding algorithm. An on-line algorithm (in VHDL/Verilog languages) identifies, in the digitized signals after a pre-amplification, in real time, the peaks due to the single ionization electrons, records their times and amplitudes and sends the data stored to an external device when a specific trigger signals occurs.

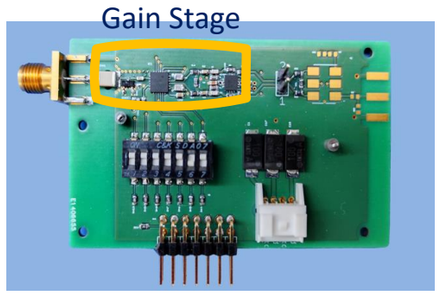


A possible amplifier



- 2 stage amplifiers based on commercial devices:
  - Variable gain LMH6881 is a high-speed, high-performance fully differential programmable amplifier
  - THS4509 (wideband low noise fully differential amplifier
- The gain stage supports gain settings up to about 50 dB with small accurate 0.25dB gain steps, although the VGA can also be parallel programmed.
- Bandwidth about 1GHz

Gain Stage

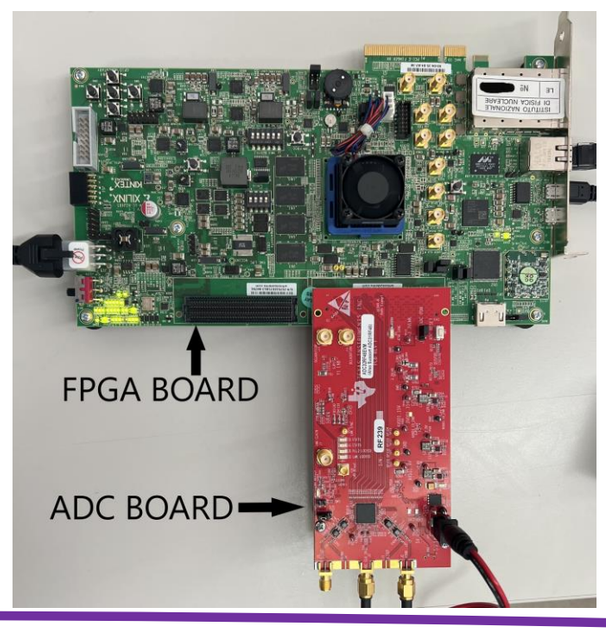


Mode/Gain programming.
with dip switches it is possible to select the gain of the first stage.

FPGA and ADC

A fast read-out CTT algorithm has been developed with success as VHDL code implemented on a Virtex 6 FPGA (maximum input/output clock switching frequency of 710 MHz). The hardware setup includes also a 12-bit monolithic pipeline sampling ADC at conversion rates up to 2.0 GSPS. To improve the performance of the algorithms used (and try others with better performance) it was decided to focus on more performing hardware. The new hardware, for this reason, uses an FPGA with better performances (in terms of time and power) and allows us to reduce the processing time and to manage multichannel ADCs:

- **KIT EVAL ULTRASCALE FPGA KCU105**
  - UltraScale™ XCKU040-2FFVA1156E
  - Transceiver 20 GTH
  - 2 moduli SFP+ da 10Gbps
- **ADC ADC32RF45**
  - 14-Bit, Dual-Channel, 3.0-GSPS ADC
  - Noise Floor: –155 dBFS/Hz
  - RF Input Supports Up to 4.0 GHz
  - Aperture Jitter: 90 fS
  - Channel Isolation: 95 dB at f_{IN} = 1.8 GHz

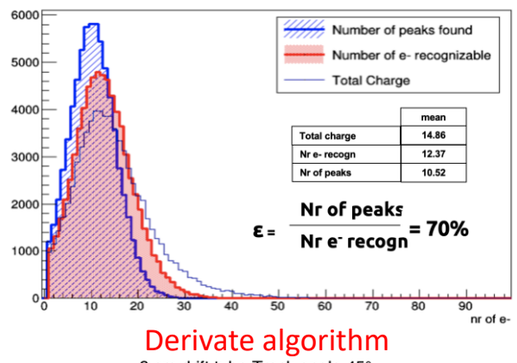


CTT algorithms

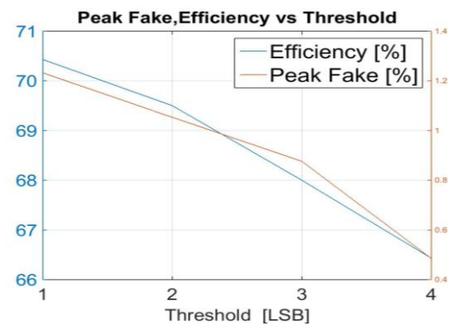
A first simple tested peak finder algorithm is based on the first and second derivative of the digitized signal function f, defined for each time bin i, Δb being the number of bins over which the average value of f is calculated:

$$f'(i) = \frac{f(i) - \bar{f}(i - \Delta b)}{\Delta b} \qquad f''(i) = f'(i) - f'(i-1)$$

A peak is found when Δf, f' and f'' are above a pre-defined threshold level.

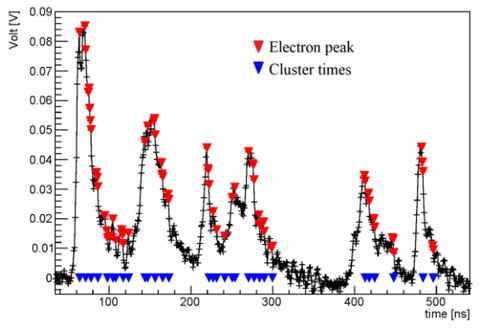


Derivate algorithm

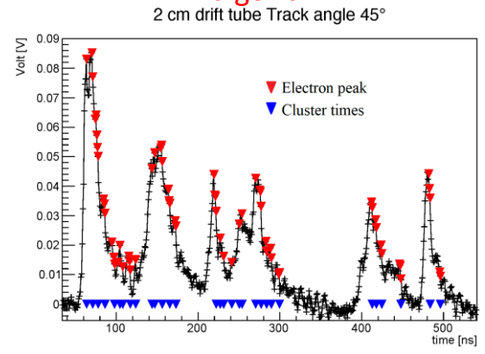


RTA algorithm

2 cm drift tube Track angle 45°



2 cm drift tube Track angle 45°



A further algorithm that is being implemented on FPGAs is the Running Template Algorithm (RTA). It is based on a bin-by-bin difference of the waveform with a normalized search template.

Summary

The derivate algorithm has been implemented and tested on FPGAs, while the RTA algorithm is in the testing phase with PC simulations and testbench. From these tests, it results that there is a peak detection efficiency of 72%, with 1.2% fake peak rate, for the derivative algorithm, while 70% for the RTA algorithm, with 1% of fake peak rate.

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