Implementation of the Cluster Counting and Timing realtime algorithm on FPGA to improve the impact parameter estimates of the Drift Chamber and particle identification.

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Abstract. Ultra-low mass and high granularity Drift Chambers fulfill the requirements for tracking systems of modern High Energy Physics experiments at the future high luminosity facilities (FCC-ee or CEPC).
We present how, in Helium based gas mixtures, by measuring the arrival times of each individual ionization cluster and by using proper statistical tools, it is possible to perform a bias free estimate of the impact parameter and a precise PID. Typically, in a helium-based drift chamber, consecutive ionization clusters are separated in time by a few ns, at small impact parameters up to a few tens of ns, at large impact parameters. For an efficient application of the cluster timing technique, consisting in isolating pulses due to different ionization cluster, it is, therefore, necessary to have read-out interfaces capable of processing high speed signals. We present a full front-end chain, able to treat the low amplitude sense wire signals (a ∼few mV), converted from analog to digital with the use of FADCs, with a high bandwidth (∼1 GHz). The requirement of high sampling frequency, together with long drift times, usually of the order of several hundreds of ns, and large number of readout channels, typically of the order of tens of thousand, impose a sizable data reduction, meanwhile preserving all relevant information. Measuring both the amplitude and the arrival time of each peak in the signal associated to each ionization cluster is the minimum requirement on the data transfer for storage to prevent any significant data loss. An electronic board including a Fast ADC and an FPGA for a real-time processing of the drift chamber signals is presented. Various peak finding algorithms, implemented and tested in real time with VHDL code, are also compared.

1. Introduction

The Cluster timing technique (CCT), which consists in measuring the arrival times on the sense wires of each individual ionisation electron, overcomes a substantial bias in the impact parameter

estimate (normally in the drift chamber [1, 2], only the time of the first cluster is used to estimate the track impact parameter) offers the possibility of greatly improving the particle identification capabilities.
This technique uses statistical tools to reduce the biased estimate, by exploiting the information of all clusters detected with a peak finding algorithm. An on-line algorithm (in VHDL/Verilog languages) identifies, in the digitized signals after a first analog amplification, in real time, the peaks due to the single ionization electrons, records their times and amplitudes and sends the data stored when a specific trigger signals occurs.

2. Acquisition channel

The wire signals generated by the drift chamber, before being processed, are amplified to increase the Signal-Noise Ratio. After the signal is converted from analog to digital with the use of an ADC [2]. Requirements on drift chamber performance impose an amplification of about 20db with 1GHz bandwidth, this allows to amplify all the peaks of the signal and an ADC with at least 1-2 GS/s and 12-14-bit resolution, a schematic, a block diagram of the acquisition channel in the figure 1. These constraints, together with the maximum drift times, usually of the order of 1 μm and with the large number of acquisition channels demand some sizeable data reduction, however the data must preserve all the relevant information. In the following sections we will see the possible amplifiers and algorithms implemented on FPGAs

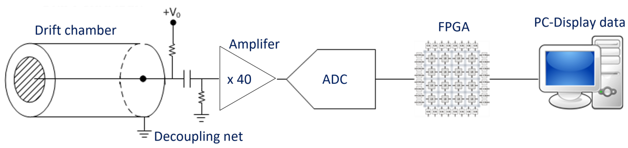

Figure 1. Typical chain acquisition of drift chamber

3. Amplifer

In a Helium based gas mixture the rise time of the signal from a cluster is approximately 1 ns, so front-end electronics with about 1 GHz bandwidth are required with high linearity, low distortion and sufficiently high bandwidth . Furthermore, it would be useful for the readout electronics to be able to easily adapt its gain to the detector's operating point. The use of a variable gain amplifier (VGA) allows to meet the needs arising from the changed operating conditions of the detector. The idea is to use multi-channel amplifiers (like LMH6522 in the figure 2) to have more space close to the detector and one has also to the distribution of the power and of cooling.

4. FPGA and ADC

A fast read-out CCT algorithm has been developed with success as VHDL code implemented on a Virtex 6 FPGA (maximum clock switching frequency of 710 MHz). The hardware setup includes also a 12-bit monolithic pipeline sampling ADC at conversion rates up to 2.0 GSPS. To improve the performance of the algorithms used (and try others with better performance) it was decided to focus on more performing hardware. The new hardware for this reason uses an FPGA with better performances (temporal and powering) allows us to reduce the processing time and manage multichannel ADCs. The new hardware (in figure 3)consists:

- KIT EVAL ULTRASCALE FPGA KCU105 [6]
- Texas Instrument ADC ADC32RF45 [7]

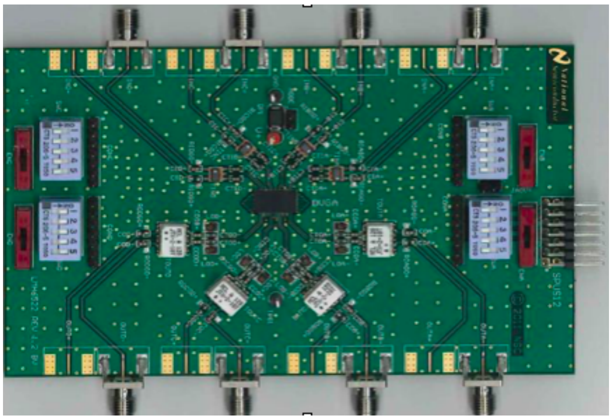

Figure 2. Eval board LMH6522.

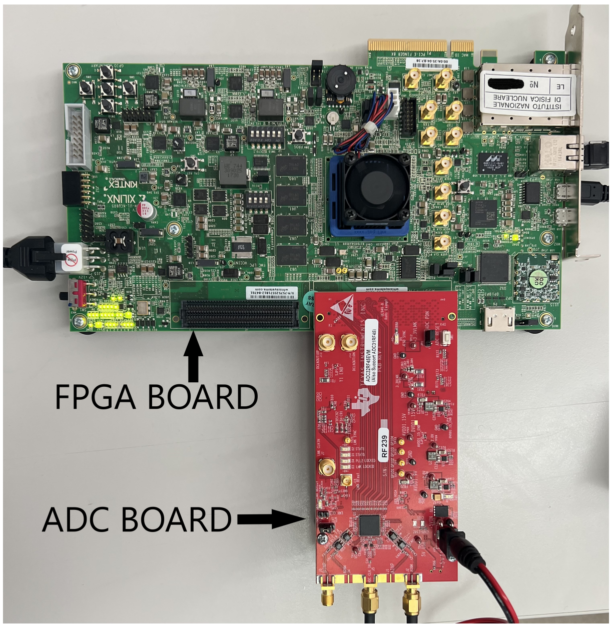

Figure 3. Experimental setup using as FPGA the EVAL KIT KCU105 and as ADC the Texas Instruments ADC32RF45EVM used for testing the performance of the algorithm.

5. CCT Algorithm

We have several algorithms to test all are based on the following steps. The idea of the algorithm is to transfer only the essential information. It consists in transferring, for each hit drift cell, instead of the full spectrum of the signal, only the minimal information relevant to the application of the CCT techniques [4, 5], i.e. the amplitude and the arrival time of each peak associated with each individual ionization electron.
The real-time algorithms , that we developed, is able to process the data in real-time and in particular it:

- identifies, in the digitized signal, the peaks corresponding to the different ionization clusters;
- stores each peak amplitude and its time in an internal memory;
- sends the data stored to an external device when specific trigger signals occur.

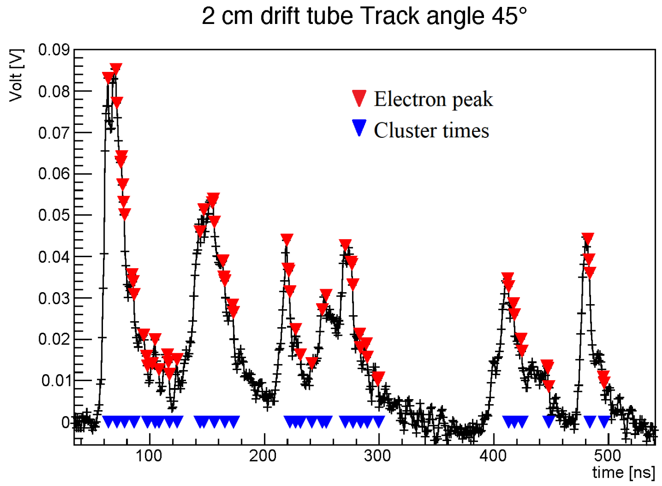

Figure 4. The figure shows typical waveform with red markers indicating the single electron peak found by the derived algorithm and blue markers indicating the cluster obtained as an association of multiple electron ionization acts. The image is processed with the DA algorithm.

In the following subsections we will describe some algorithms that we want to implement. Some signal spectra obtained from simulations will be shown.

5.1. Derivative Algorithm

The derivative algorithm (DA) is based on the calculation of the first and second derivative of the digitized signal function$f$, is defined for each time bin i

$$f'(i) = \frac{f(i) - f(i - \Delta b)}{\Delta b}, \qquad f'' = f'(i) - f'(i-1) \tag{1}$$

Δb being the number of bins (signal rise time) over which the average value of i is calculated. A peak (assumed to be an ionization electron) is found when Δf, f' and f'' are above a threshold level defined according to r.m.s. noise of the signal function f, and when the time difference a contiguous peaks is larger than the time bin resolution. The association of electrons in clusters is based on the time difference among consecutive electrons. Electrons belonging to the same cluster are separated by time difference which are compatible with single electron diffusion. Figure 4 shows an example of how the algorithm works on a simulated waveform.

5.2. Running Template Algorithm (RTA)

The RTA algorithm is based on the definition of a digitised electron peak model, composed by a raising and a falling exponential over a fixed number of bins, adapted to experimental data and sampling rate. If inside the waveform there is a peak that corresponds, within a χ^2 cut, to the properly scaled electron peak template, the algorithm will save its amplitude and subtract it from the waveform. The procedure is repeated until no further peaks are found (Figure 5.).

6. Conclusion

The derivative algorithm has been implemented and tested on FPGAs, while the RTA algorithm is in the testing phase with PC simulations and testbench. From these tests, it results that there is a peak detection efficiency equal to about 72% of the derived algorithm (with about 1.2% of

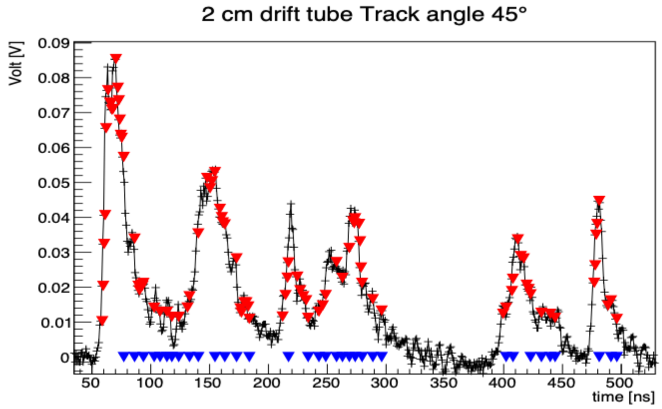

Figure 5. The figure shows typical waveform with red markers indicating the single electron peak found by the derived algorithm and blue markers indicating the cluster obtained as an association of multiple electron ionization acts. The image is processed with the RTA algorithm.

peak fake rate) while the 70% of the RTA algorithm (with about 1% of the peak falsification rate).

Acknowledgment

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