9 I/O Pads

9.1 Pad Types

The chip has I/O Pads on all 4 sides. There 4 different types of IO Pads: *PG* (Power or Ground supply)*CML* (differential digital pad), *dig* (single ended digital pad) and *ana* (analog pad). The description indicates if the Pad is for the matrix (M), periphery (P) or some other component.

9.2 Pad Map and Pad Groups

The RD50-MPW3 has a lot of different IO signals to control and monitor as many features as possible. Due to layout constrains, these signals are not in any specific order. Thus, they are grouped by their functionality and colored in figures 17, 18, 19, 20 and section 9.3, accordingly. Table 5 gives an overview of different pad types.

Type	**Pad List**	**Color**	**Section reference**
Analog IO	T11, R3, R35, L21, L28	**violet**	3 PS:better ref needed
I2C	R28, R29, R30, R36, R37	yellow	4.7
Monitoring for digital circuits	B1-B3, B30, B31, L37-L41	**blue**	4.7
Clocks and resets	B12-B15, B42, B43, L29-L32, L42	**green**	4.6
Data output & configuration readback	T10, B5-B7, B16, B17	**brown**	4.2 and 4.4
External control	B4, B32, B37, B41	pink	4.7
Timestamp control	B33-B35	**red**	4.5
Analog MUX & analog Buffer	L24-L27	orange	3 PS:better ref needed
Pads for Teststructures	S1-S22	gray	8
Power and Ground	all other	**black**	3 PS:better ref needed

Table 5: Different pad types for RD50-MPW3.

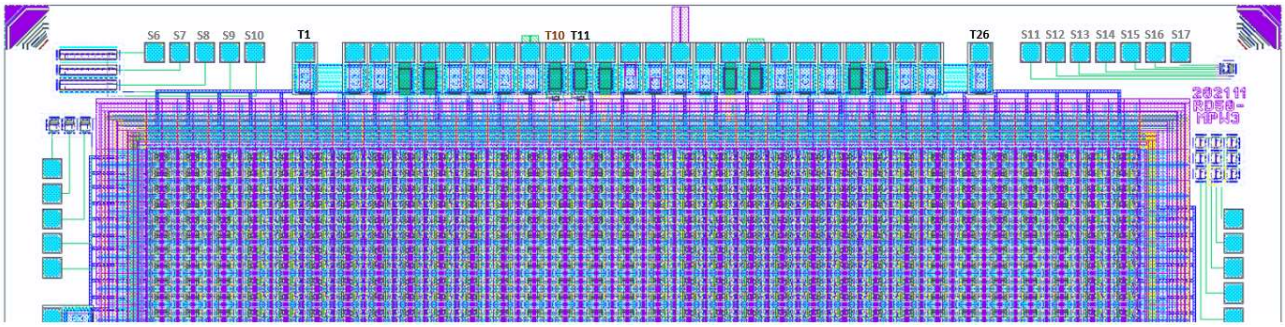

Figure 17: Top IO Pads

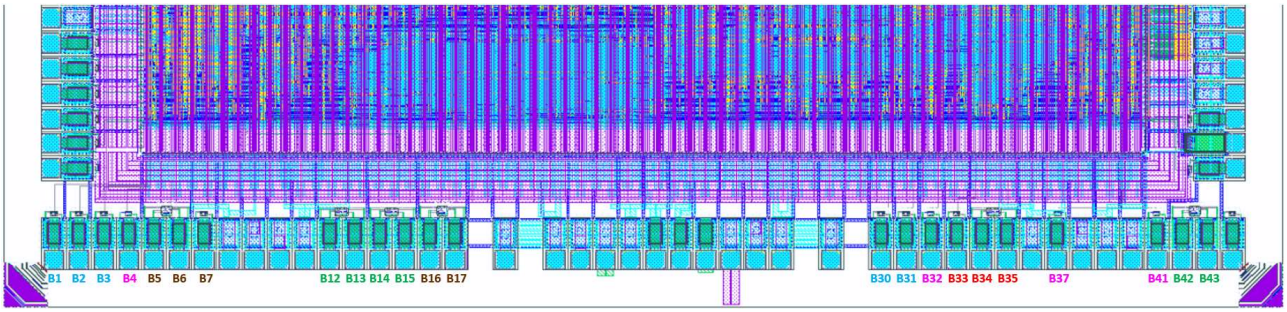

Figure 18: Bottom IO Pads

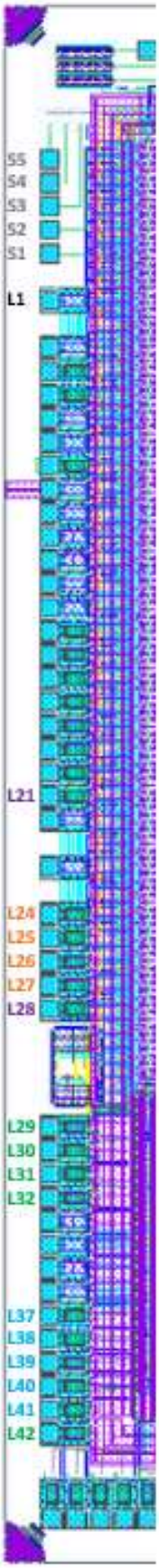

Figure 19: Left IO Pads

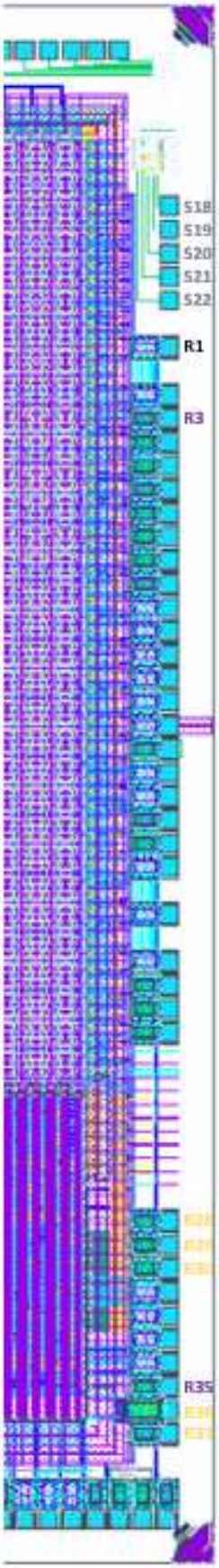

Figure 20: Right IO Pads

9.3 Pad List

9.3.1 Top I/O Pads

Number	Name	Direction	Type	Voltage	Current	Description
T1	sub_T1	x	PG			Bias for M
T2	GNDA_3	x	PG			Bias for M
T3	VDDA_2	x	PG			Bias for M
T4	VSSA	x	PG			Bias for M
T5	VDDC	x	PG			Bias for M
T6	gnd_T1	x	PG			Bias for M
T7	vdd_T1	x	PG			Bias for M
T8	GNDA_2	x	PG			Bias for M
T9	PW_RING	x	PG			Bias for guardring
T10	SEROUT_DC13	O	dig			Data Output
T11	COMPOUT_DC13	O	dig			Monitoring
T12	BL	x	PG			
T13	vdd_io_T	x	PG			Bias for Pads
T14	vss_io_T	x	PG			Bias for Pads
T15	SEAL_RING	x	PG			Bias for guardring
T16	VDDA_1	x	PG			Bias for M
T17	VSENSBIAS	x	PG			
T18	NW_RING	x	PG			Bias for guardring
T19	GND_A_1	x	PG			Bias for M
T20	vdd!_T0!	x	PG			Bias for M
T21	gnd!_T0	x	PG			Bias for digital circuits
T22	VDDC	x	PG			Bias for M
T23	VSSA	x	PG			Bias for M
T24	VDDA_0	x	PG			Bias for M
T25	GNDA_0	x	PG			Bias for M
T26	sub_T0	x	PG			Bias for M

9.3.2 Right I/O Pads

Number	Name	Direction	Type	Voltage	Current	Description
R1	sub_R0	x	PG			Bias for M
R2	GNDA_R0	x	PG			Bias for M
R3	INJECTION	I	ana			Charge Injection
R4	VSENSBIAS	x	PG			Bias for M
R5	VSSA	x	PG			Bias for M
R6	VDDC	x	PG			Bias for M
R7	BL	I	ana			
R8	DEL_LO	I	ana			
R9	DEL_HI	I	ana			
R10	TH	I	ana			
R11	GNDA_R1	x	PG			Bias for M
R12	VDDA_R1	x	PG			Bias for M
R13	vss_io_R	x	PG			Bias for Pads
R14	vdd_io_R	x	PG			Bias for Pads
R15	PW_RING	x	PG			Bias for guardring
R16	SEAL_RING	x	PG			Bias for guardring
R17	NW_RING	x	PG			Bias for guardring
R18	gnd!_R	x	PG			Bias for digital circuits
R19	vdd!_R	x	PG			Bias for digital circuits
R20	VDDC	x	PG			Bias for M
R21	VSSA	x	PG			Bias for M
R22	GNDA_R2	x	PG			Bias for M
R23	sub_R1	x	PG			Bias for M
R24	VDDA_R0	x	PG			Bias for M
R25	VP_COMP	x	PG			
R26	VN	x	PG			
R27	VN_CS_BB	x	PG			
R28	ADR_2	I	dig			I2C
R29	ADR_1	I	dig			I2C
R30	ADR_0	I	dig			I2C
R31	vdd_B_R_DIG0	x	PG			Bias for M
R32	vdd_io_R_B_DIG	x	PG			Bias for M
R33	vss_io_R_B_DIG	x	PG			Bias for M
R34	gnd_B_R_DIG0	x	PG			Bias for M
R35	HB	O	dig			HitBus Signal
R36	SDA_io	IO	dig			I2C
R37	SCL	I	dig			I2C

9.3.3 Bottom I/O Pads

Number	Name	Direction	Type	Voltage	Current	Description
B1	EOC0_TOKEN_OUT	O	dig			Monitoring
B2	EOC0_FIFO_FULL	O	dig			Monitoring
B3	EOC0_FIFO_EMPTY	O	dig			Monitoring
B4	EOC0_READ_ext	I	dig			External Control
B5	SER_OUT_CHIP_P	O	CML			Data Output
B6	SER_OUT_CHIP_N	O	CML			Data Output
B7	SHIFT_IN_PROGRESS	O	dig			Data Output
B8	vdd!_B_L_DIG1	x	PG			Bias for digital circuits
B9	vss_io_B_L_DIG	x	PG			Bias for Pads
B10	vdd_io_B_L_DIG	x	PG			Bias for Pads
B11	gnd!_B_L_DIG1	x	PG			Bias for digital circuits
B12	EXT_CLK_640MHZ_N	I	CML			CLK640MHz Input
B13	EXT_CLK_640MHZ_P	I	CML			CLK640MHz Input
B14	EXT_CLK_40MHZ_N	I	CML			CLK40MHz Input
B15	EXT_CLK_40MHZ_P	I	CML			CLK40MHz Input
B16	DATA_OUT_P	O	CML			Data Output
B17	DATA_OUT_N	O	CML			Data Output
B18	sub_B1	x	PG			Bias for M
B19	GNDA_0	x	PG			Bias for M
B20	vdd_io_B	x	PG			Bias for Pads
B21	PW_RING	x	PG			Bias for guardring
B22	VDDA	x	PG			Bias for M
B23	VSSA	x	PG			Bias for M
B24	VDDC	x	PG			Bias for M
B25	NWELL_RING	x	PG			Bias for guardring
B26	SEAL_RING	x	PG			Bias for guardring
B27	vss_io_B	x	PG			Bias for Pads
B28	GNDA_1	x	PG			Bias for M
B29	sub_B0	x	PG			Bias for M
B30	TX_FIFO_FULL	O	dig			Monitoring
B31	TX_FIFO_EMPTY	O	dig			Monitoring
B32	TX_FIFO_RD_n_ext	I	dig			External Control
B33	TS_OVERFLOW	O	dig			Timestamp Control
B34	INI_TS_ext_N	I	CML			Timestamp Control
B35	INI_TS_ext_P	I	CML			Timestamp Control
B36	gnd_B_R_DIG1	x	PG			Bias for M
B37	CU_RD_ext	I	dig			External Control
B38	vss_io_B_R_DIG	x	PG			Bias for Pads
B39	vdd_B_R_DIG1	x	PG			Bias for M
B40	vdd_io_B_R_DIG	x	PG			Bias for Pads
B41	CU_RQT_DATA_ext	I	dig			External Control
B42	CLK40_o_P	O	dig			Monitoring, Clock
B43	CLK40_o_N	O	dig			Monitoring, Clock
B44	*not used (???)*	x	x			

9.3.4 Left I/O Pads

Number	Name	Direction	Type	Voltage	Current	Description
L1	sub_L0	x	PG			Bias for M
L2	GNDA_L0	x	PG			Bias for M
L3	VSSA	x	PG			Bias for M
L4	VDDC	x	PG			Bias for M
L5	vdd!_L	x	PG			Bias for digital circuits
L6	gnd!_L	x	PG			Bias for digital circuits
L7	NW_RING	x	PG			Bias for guardring
L8	SEAL_RING	x	PG			Bias for guardring
L9	PW_RING	x	PG			Bias for guardring
L10	vdd_io_L	x	PG			Bias for Pads
L11	vss_io_L	x	PG			Bias for Pads
L12	VDDA_L	x	PG			Bias for M
L13	GNDA_L1	x	PG			Bias for M
L14	TH	I	ana			
L15	DEL_HI	I	ana			
L16	DEL_LO	I	ana			
L17	BL	I	ana			
L18	VDDC	x	PG			Bias for M
L19	VSSA	x	PG			Bias for M
L20	VSENSBIAS	x	PG			
L21	INJECTION	I	ana			Charge Injection
L22	GNDA_L2	x	PG			Bias for M
L23	sub_L1	x	PG			Bias for M
L24	ABUFF_POWER	x	PG			Analog Buffer
L25	AMUX_CLK	I	ana			Analog MUX
L26	AMUX_INIT	I	ana			Analog MUX
L27	ABUFF_OUT	I	ana			Analog Buffer
L28	SFOUTBUFF	O	ana			SFOUT Signal
L29	EXT_RST_N	I	CML			Reset
L30	EXT_RST_P	I	CML			Reset
L31	EXT_AUX_RST_N	I	CML			Reset
L32	EXT_AUX_RST_N	I	CML			Reset
L33	vdd_io_L_B_DIG	x	PG			Bias for Pads
L34	vdd!_B_L_DIG0	x	PG			Bias for digital circuits
L35	vss_io_L_B_DIG	x	PG			Bias for Pads
L36	gnd!_B_LDIG0	x	PG			Bias for digital circuits
L37	EOC0_HIT_OUT	O	dig			Monitoring
L38	EOC0_HIT_OUT_reg	O	dig			Monitoring
L39	EOC0_RQT_DATA	O	dig			Monitoring
L40	EOC0_RD	O	dig			Monitoring
L41	EOC0_TOKEN_IN	O	dig			Monitoring
L42	SEL_EXT_CLK40MHz	I	dig			Clock select

9.3.5 I/O Pads for Teststructures

Number	Name	Direction	Type	Voltage	Current	Description
S1	gnd!					
S2	sub!					
S3	DIO3					
S4	DIO2					
S5	DIO1					
S6	DIO1					
S7	DIO2					
S8	DIO3					
S9	sub!					
S10	gnd!					
S11	sub!					
S12	gnd!					
S13	NWELL					
S14	CONNLOW					
S15	I_NOCAP					
S16	CONNHI					
S17	VDDA					
S18	DIO_CENTRE					
S19	gnd_CENTRE					
S20	gnd!					
S21	DIO_8_NEIGH					
S22	sub!					