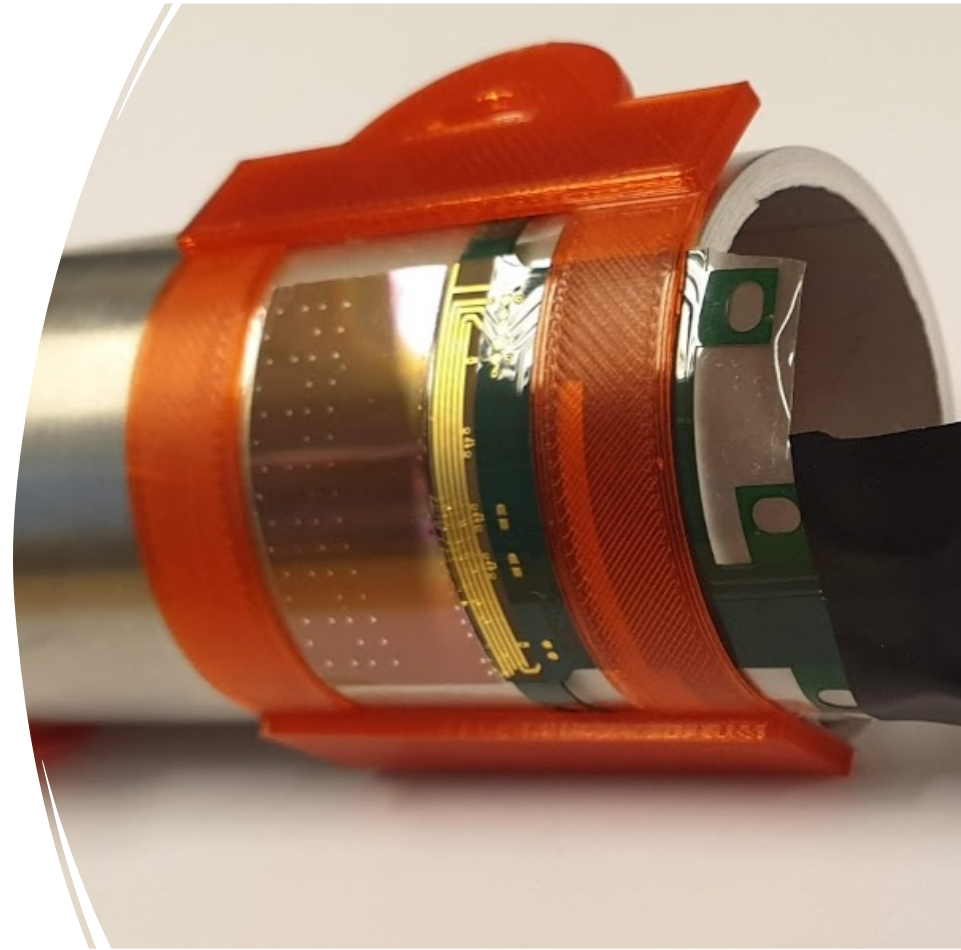


Detector R&D activities –



ECFA Roadmap

Detectors for future colliders

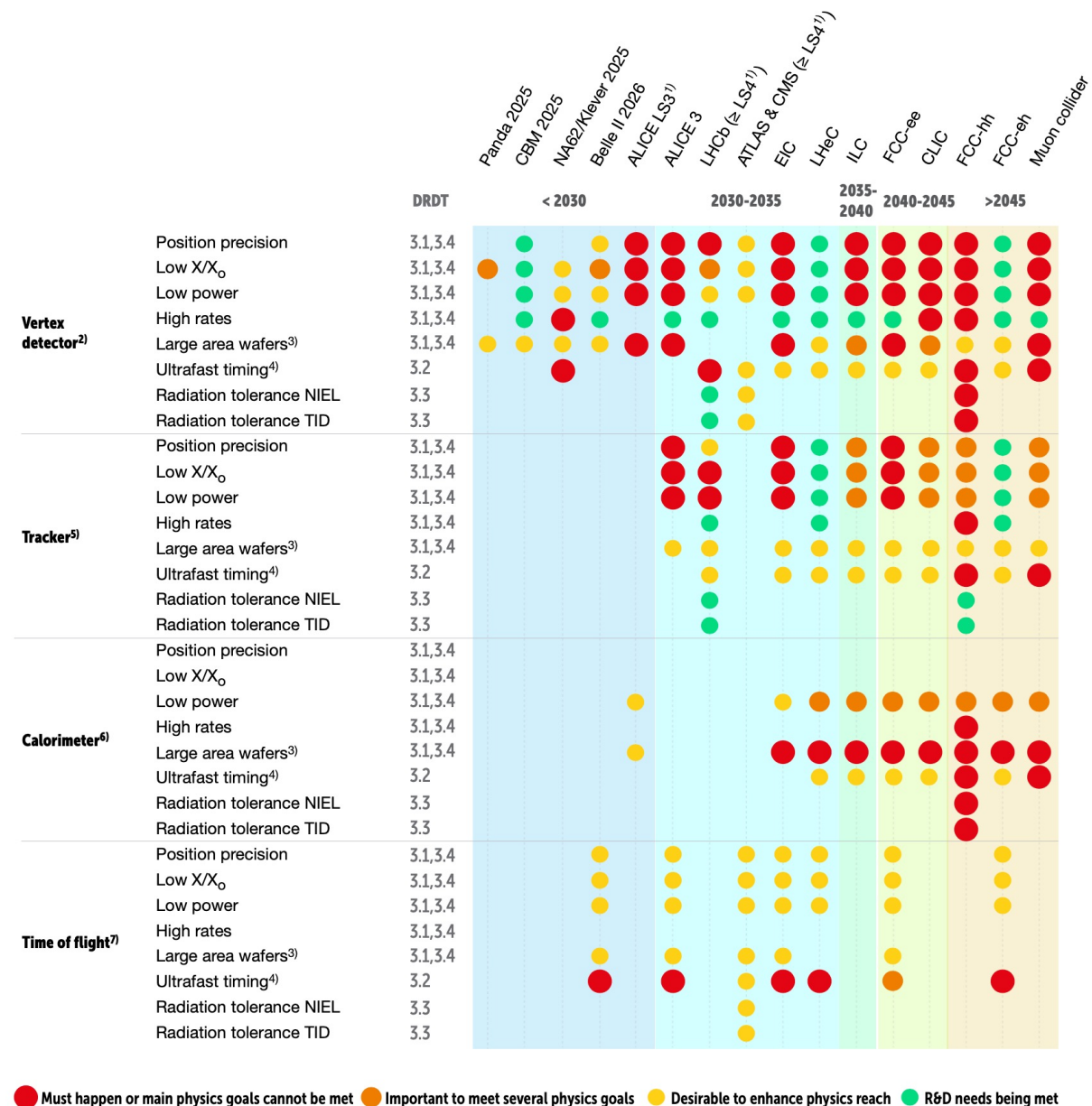
- low mass
- low power
- high-resolution trackers
- Sub-nanosecond timing
- increased radiation tolerance

3.5 Recommendations

3.5.1 Detector R&D Themes

During the various ECFA Symposia (see [Appendix C](#)) and from the feedback through the National Contacts, four main areas of research were identified.

The further evolution of active monolithic sensors is considered key to achieving several of the goals at future facilities such as very small pixels, low material budget and large area. MAPSs are also in a position to benefit greatly from the further evolution of the main consumer electronics (DRDT 3.1).

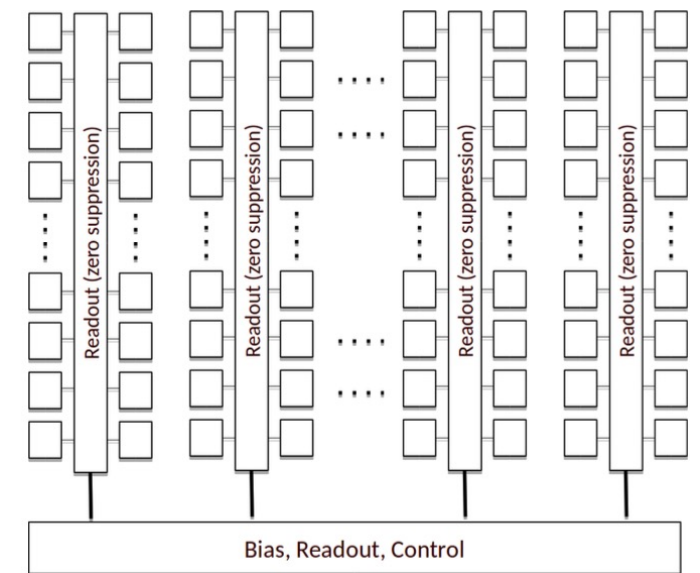
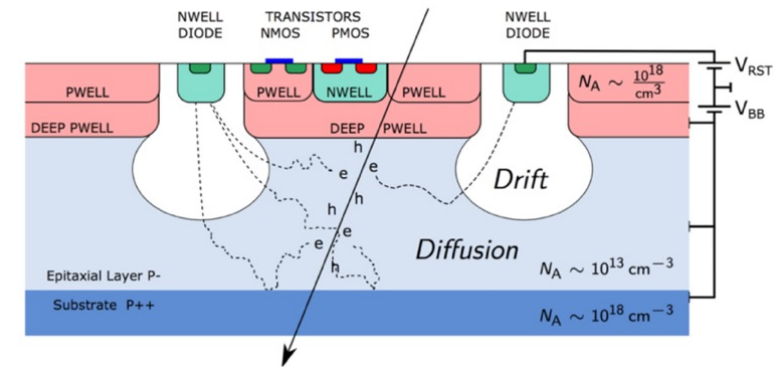


Monolithic Active Pixel Sensor (MAPS)

- Readout electronics and sensor matrix on same silicon
 - no need for bump-bonding / flip-chip technology
- Commercial CMOS technology,
 - low cost
 - Small feature size, small pitches (pixels) and position resolution
 - Low power – reduced need for cooling

“Standard process” – charge collection by diffusion

- radiation damage beyond $10^{12} - 10^{13}$ 1 MeV n_{eq}/cm^2
- Slower collection signal, less precise timing



State-of-the-art

- ~12.5 Gpixels CMOS detector
- 24000 chips, 10 m²
- Radial distance: 23 mm
- Material (mean X/X₀): 0.3%
- ALICE Pixel Detector (ALPIDE) MAPS
 - 29 x 27 μm², 1024 x 512 pixels
 - 1.5 x 3.0 cm²
 - ~40 mW/cm², ~4 μs integration time

ITS2 installed @ P2 for Run3

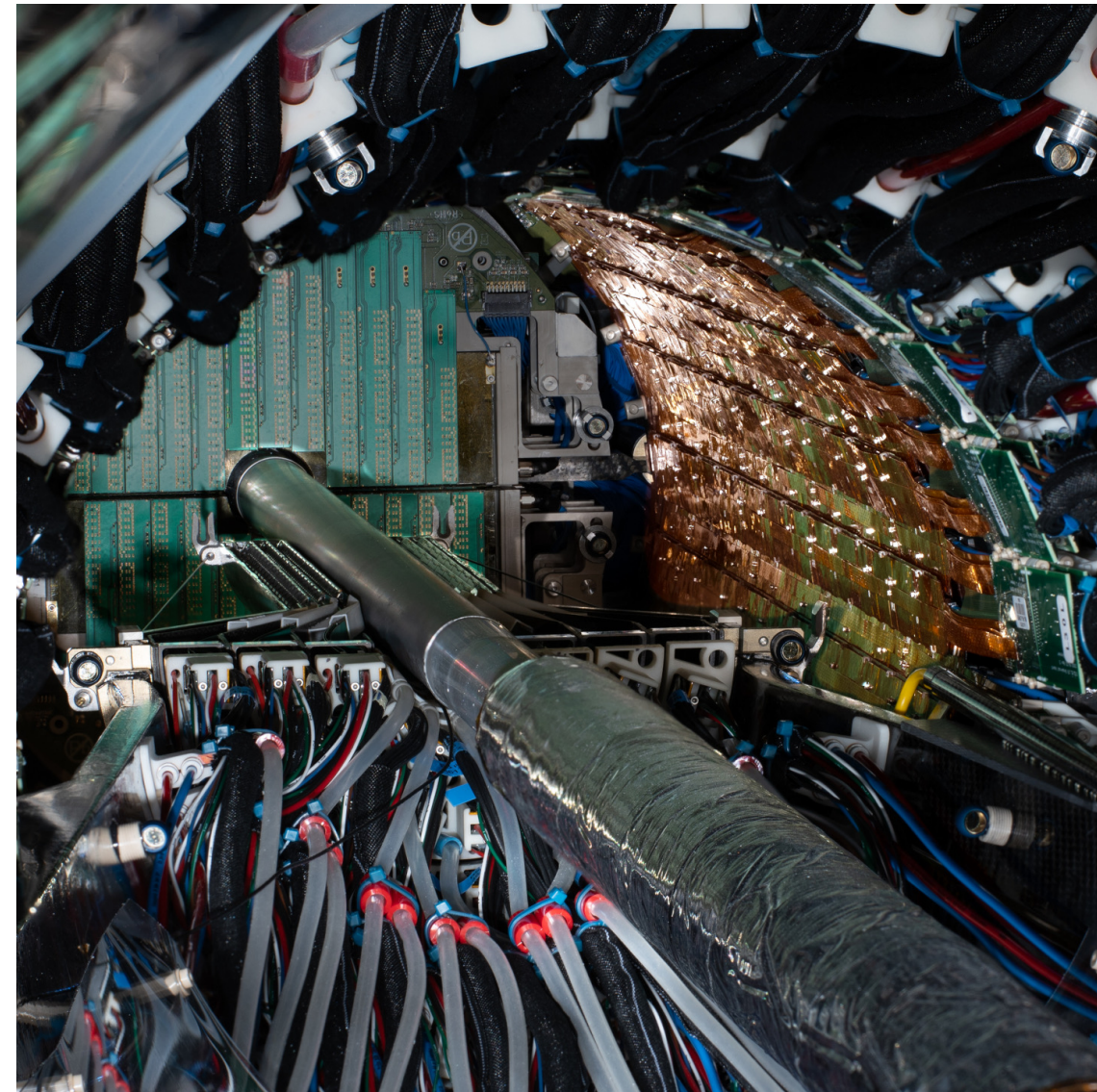
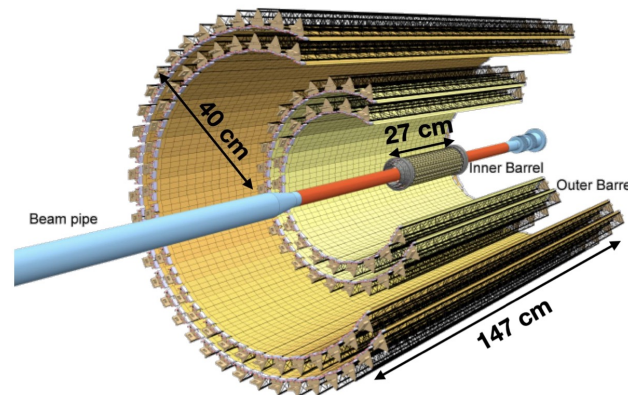
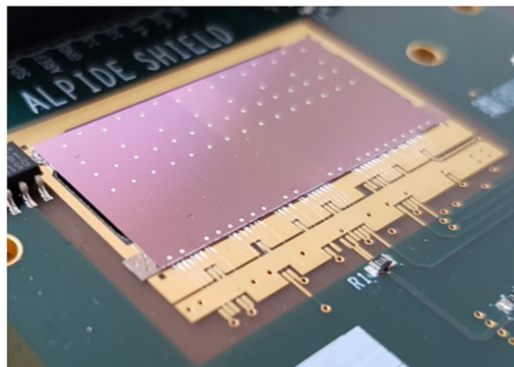
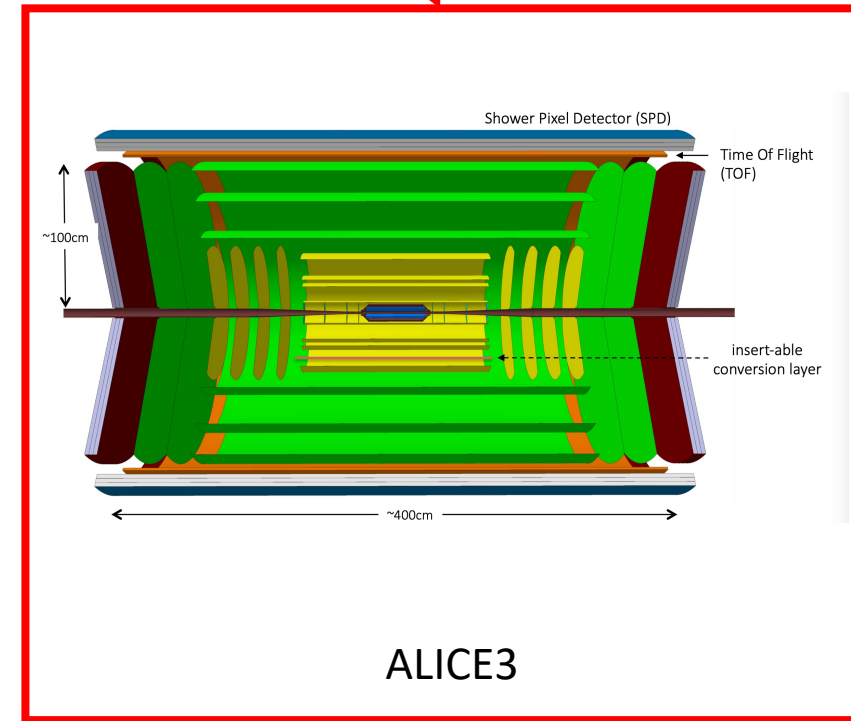
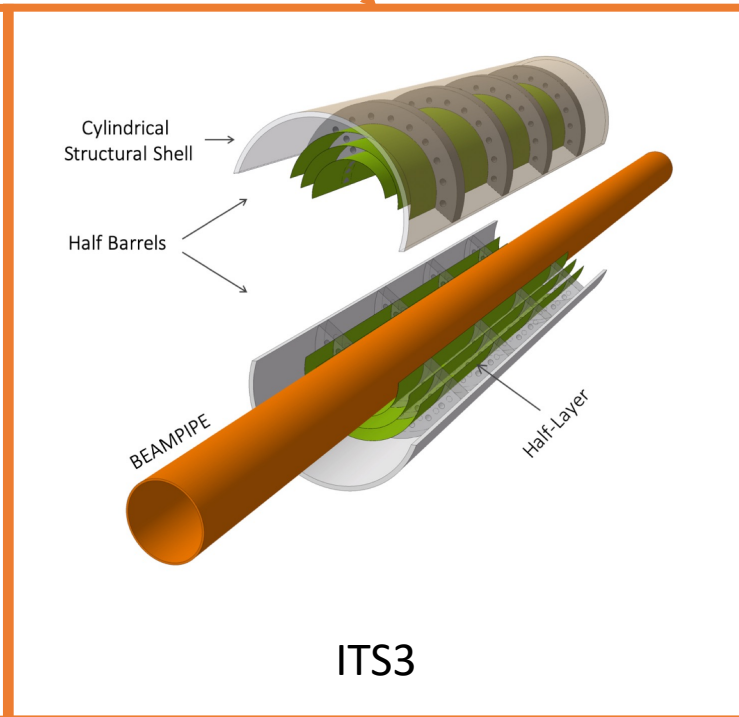
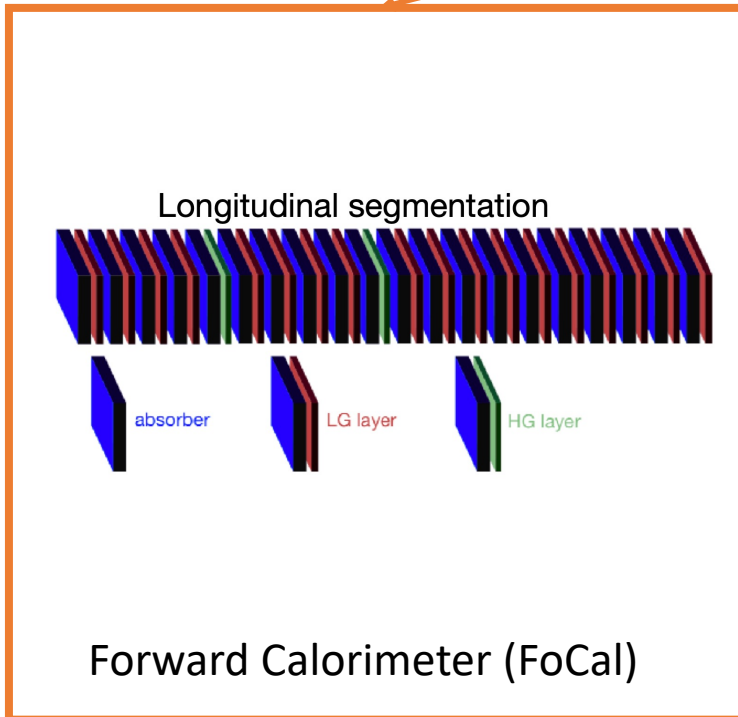
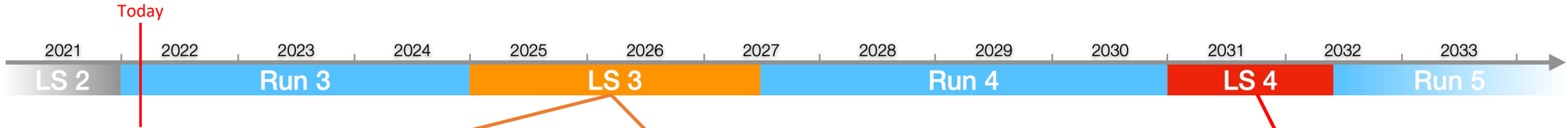


Photo credit: ALICE

Future upgrades using MAPS

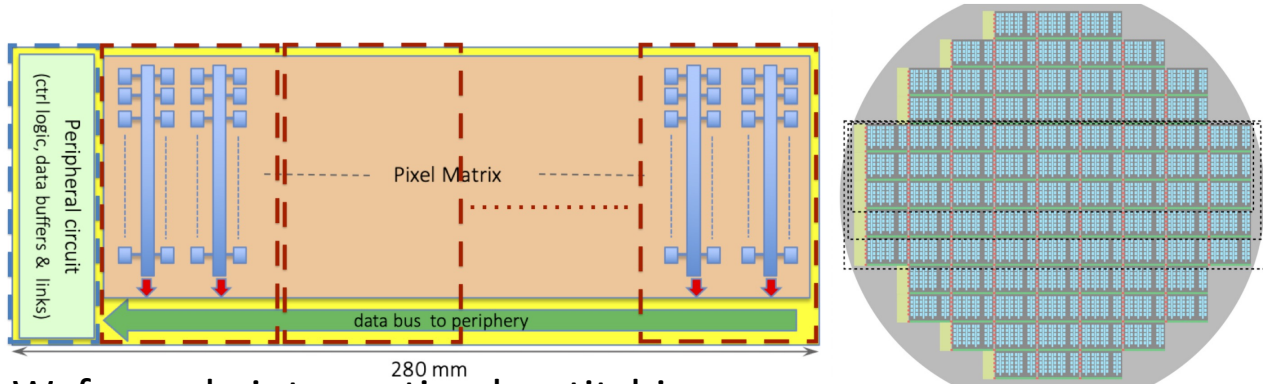


Letter of Intent for an ALICE ITS Upgrade in LS3, <https://cds.cern.ch/record/2703140>

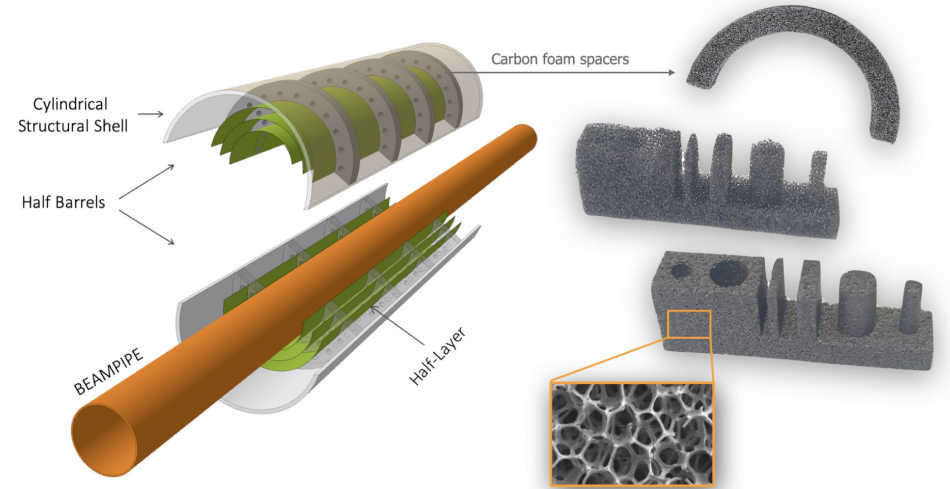
Letter of Intent: A Forward Calorimeter (FoCal) in the ALICE experiment, <https://cds.cern.ch/record/2719928?ln=en>

A next-generation LHC heavy-ion experiment, <http://arxiv.org/abs/1902.01211>

Bent, wafer scale CMOS detector



Wafer-scale intergration by stitching
65 nm technology → smaller pixel size



ITS3: Replace inner layers with 3 layers of two halves
Thinning to 20–40 μm , 0.02–0.04 X/X0

Bending of single chip and dummy wafer proven,
wafer scale chip prototypes under development

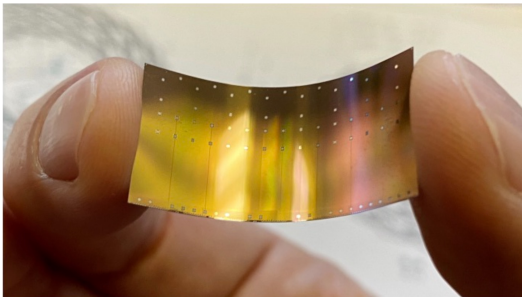
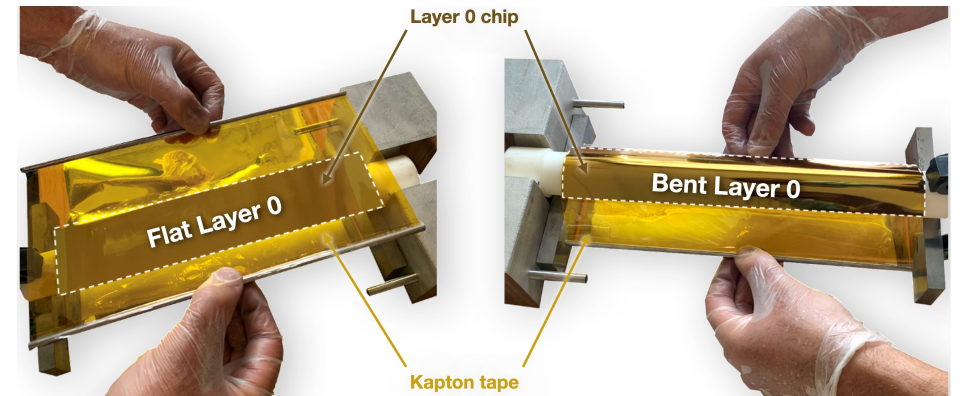
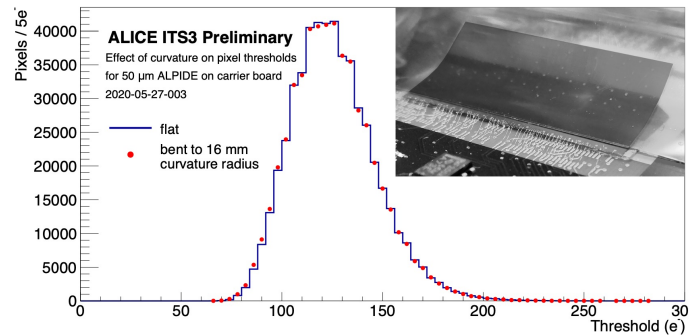


Photo credit: ALICE ITS3 https://alice-collaboration.web.cern.ch/menu_proj_items/ITS-3



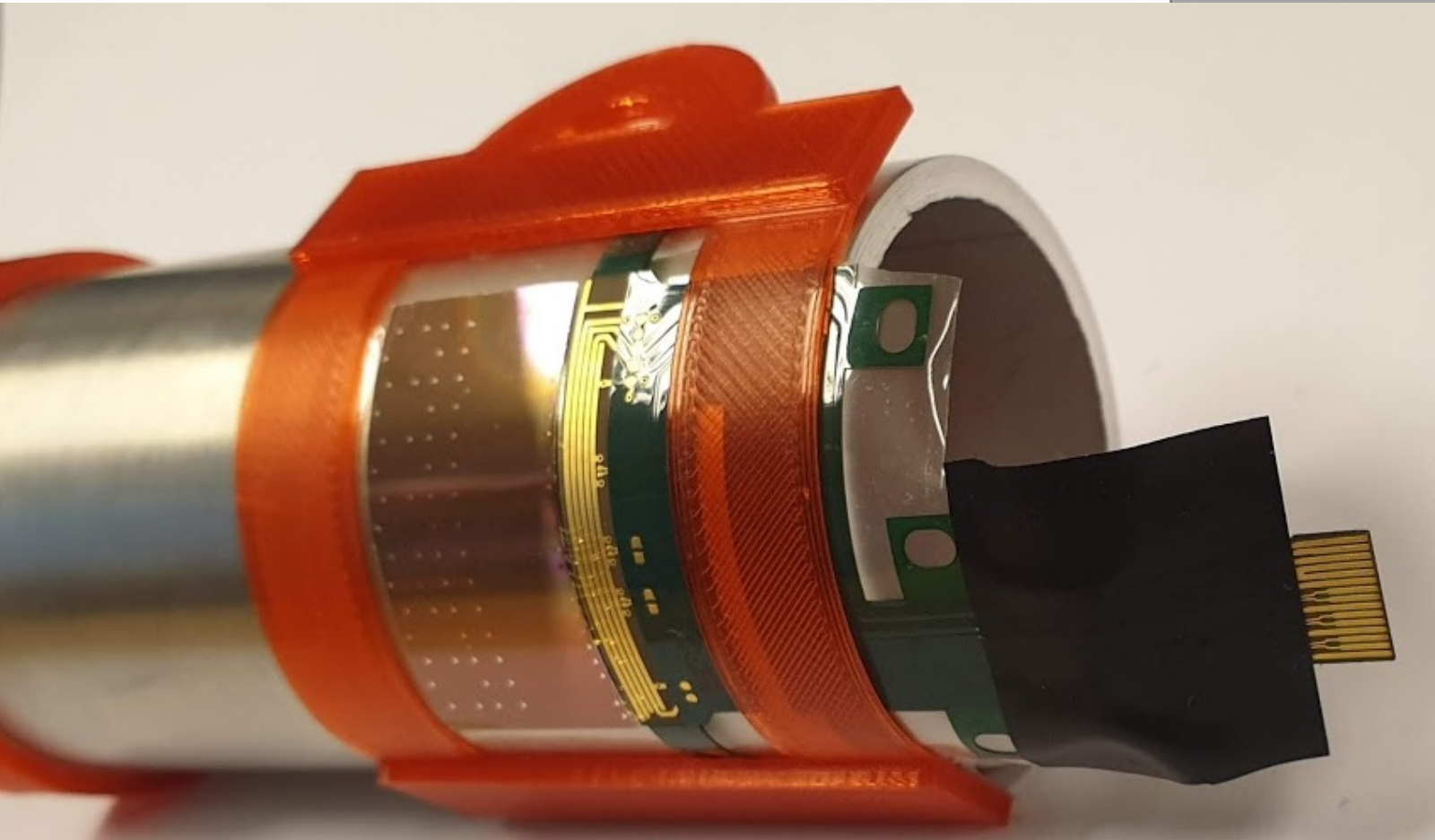
ALICE ITS3 WP4: thinning, bending, interconnect



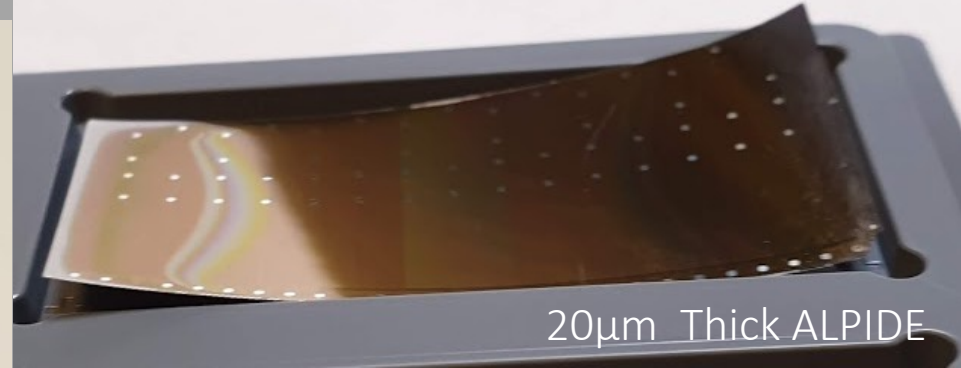
University of
South-Eastern Norway



ALICE

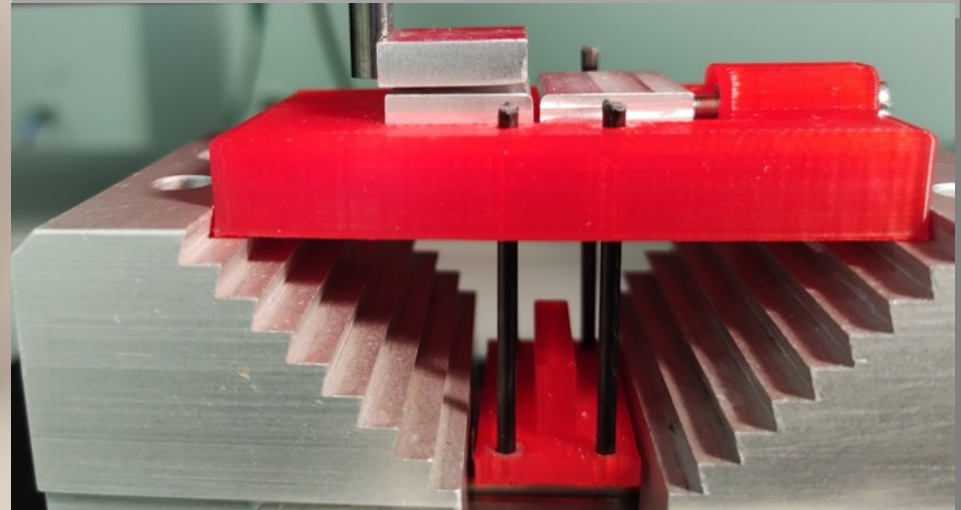


Curved and interconnected ALPIDE



20µm Thick ALPIDE

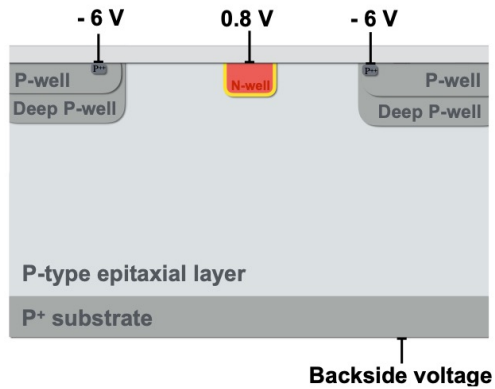
Silicon Deep Reactive Ion Etching (DRIE)
in the ranges of 20,30,50,56µm



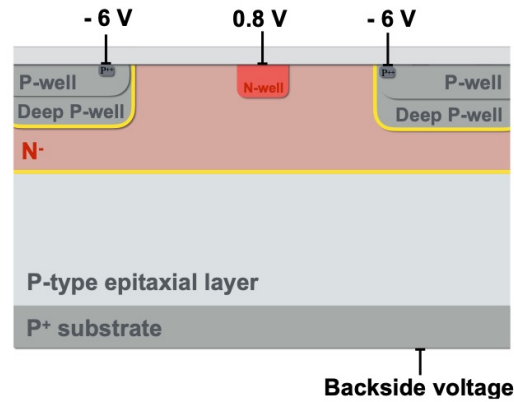
ALPIDE (Die) strength testing

Improved timing and radiation tolerance – full depletion

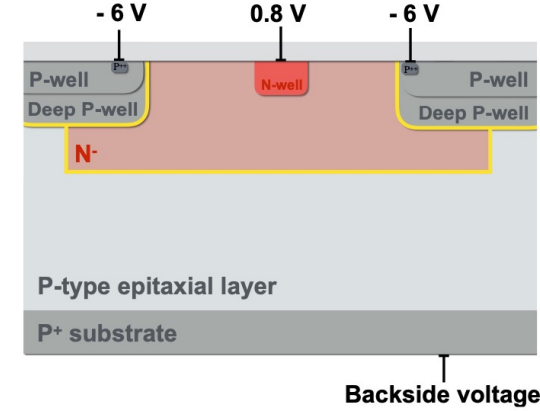
Standard process:



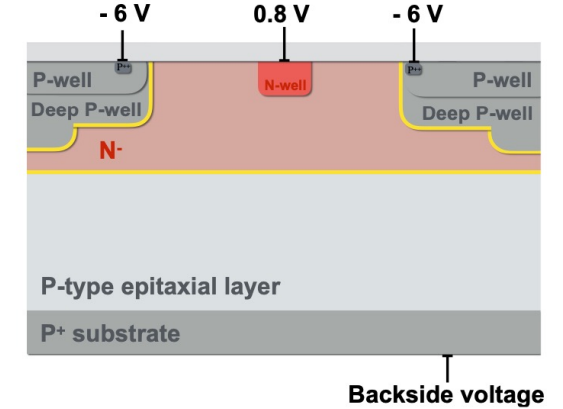
Modified process:



Gap in deep n-implant:



Additional p-implant:

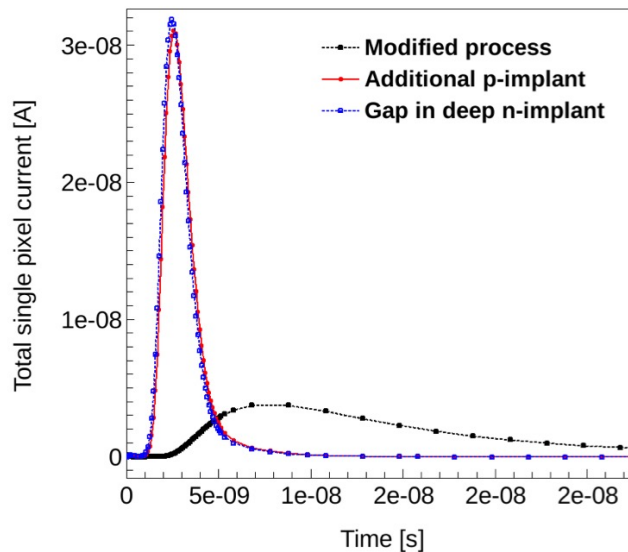


TCAD simulations for 180 nm process

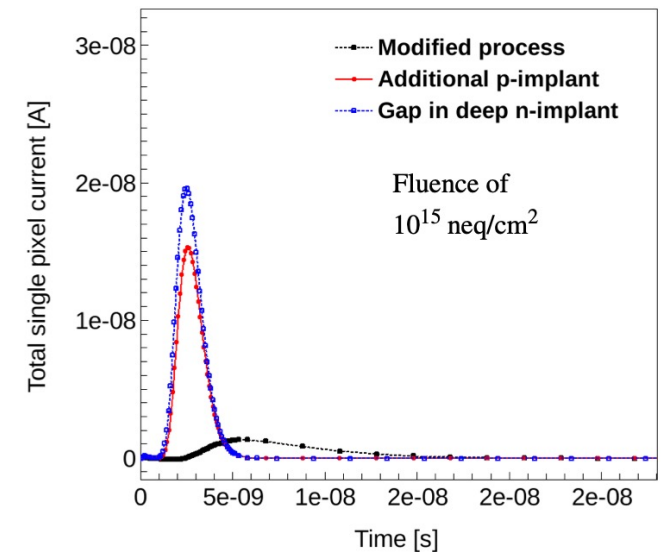
10^{15} neq/cm² demonstrated for 180 nm

Needs to be verified for 65 nm

Before irradiation:



After irradiation:



Munker et al., 2019 *JINST* **14** C05013

<https://doi.org/10.1088/1748-0221/14/05/C05013>

Pernegger et al., 2017 *JINST* **12** P06008

<https://doi.org/10.1088/1748-0221/12/06/P06008>

Long-term activities

- Participate in the R&D for FoCal, ITS3, ALICE3
- Increase access to and knowledge of this technology in Norway
- Characterization of single MAPS, as well as bent, wafer-scale CMOS MAPS (mechanical, electrical, timing, energy resolution, radiation tolerance, simulations)
- Complex readout electronics required, both on-sensor and off-sensor
- Be open to synergies/opportunities with
 - Future ee-/eh-colliders, medical, space

