# Event Filter Tracking
# for the Upgrade of the ATLAS Trigger and Data Acquisition System

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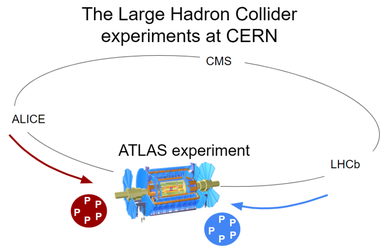
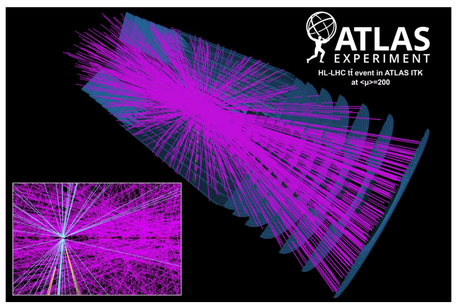
## 1. The High Luminosity Large Hadron Collider (HL-LHC)

The **HL-LHC program** [1], starting in 2029, aims at increasing the potential for discoveries, searching for new physics through the study of rare processes and exploring in greater details known physics models.

To reach these objectives more data needs to be gathered by the LHC experiments. An **increase** of the average number of **simultaneous proton-proton collisions** per bunch crossing (defined as pile-up and happening every 25 ns) is foreseen from 2029: from a current value of 40 up to 200.




## 2. The ATLAS upgrades

To cope with the HL-LHC challenging conditions and keep up with its ambitious physics program, the **ATLAS experiment** [2] is planning major upgrades, including :

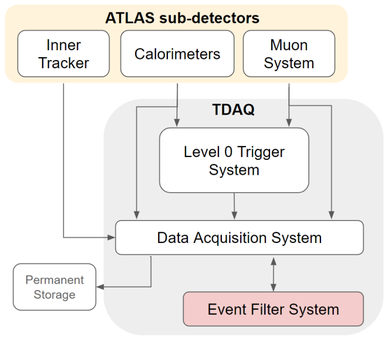
- **a new Inner Tracker** (ITk) detector [3,4] with higher granularity and extended coverage
- **The redesign of the Trigger and Data Acquisition (TDAQ)** system [5] for a more efficient real-time data selection

## 3. The TDAQ system

The proton-proton collisions produce **60 TB of data every second**, however only a **small part** of it might **lead to new discoveries**. The ATLAS TDAQ system **analyzes and selects in real-time** the collision data to reduce the flow to manageable levels and to save only events with distinguishing characteristics for physics analysis.

For the HL-LHC period the TDAQ system design [6] is the following:

1. **Level-0 trigger:** uses calorimeter and muon system data at 40 MHz to apply an initial event selection within 10 us. The output data rate is 1 MHz.
2. **Data Acquisition:** provides a common interface between all the detectors and the multi-gigabit data network, as well as detector -specific processing, as data formatting and monitoring.
3. **Event Filter**: performs a more sophisticated event selection on 1 MHz input data, within hardware and software infrastructure, for a final output data rate of about 10 kHz.




The TDAQ upgrade **Technical Design Report** (TDR) for the HL-LHC period has been **revised**, in particular fo the part related to the Event Filter, due to recent **advances in the track reconstruction software** and **commercial accelerator technology** [7].

**References:**

[1] **High-Luminosity Large Hadron Collider (HL-LHC)** https://cds.cern.ch/record/2284929
[2] **The ATLAS Experiment at the CERN Large Hadron Collider**, https://cds.cern.ch/record/1129811
[3] **TDR for the ATLAS Inner Tracker Strip Detector**, https://cds.cern.ch/record/2257755
[4] **TDR for the ATLAS Inner Tracker Pixel Detector**, https://cds.cern.ch/record/2285585
[5] **ATLAS high-level trigger, data-acquisition and controls: TDR**, https://cds.cern.ch/record/616089
[6] **TDR for the Phase-II Upgrade of the ATLAS TDAQ System**, https://cds.cern.ch/record/2285584/
[7] **TDR for the Phase-II Upgrade of the ATLAS TDAQ System - Event Filter Tracking Amendment,** https://cds.cern.ch/record/2802799/
[8] **Fast Track Reconstruction for HL-LHC,** https://cds.cern.ch/record/2693670

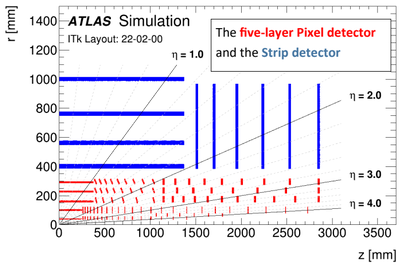
## 4. The Event Filter (EF) tracking project

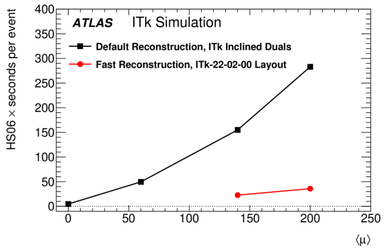
In the expected high pile-up environment of the HL-LHC, **track reconstruction** from the ITk pixel and strip detectors data can **greatly assist in the events reconstructions** at the data selection level. However, tracking algorithms are challenging with respect to processing time due to **combinatoric complexity**.

The EF tracking project [7], as a part of the TDAQ EF system, aims at **exploring** recent **advances in software tracking and heterogeneous computing systems,** which integrate multiple types of computational units. Demonstrators of tracking on several types of commodity hardware (CPU, without and with FPGA and GPU accelerators) will provide confidence that the final system will meet all the necessary specifications .

The **track reconstruction chain** involves the following steps: (1) **Data Preparation**, (2) **Track Seeding & Pattern Recognition**, and (3**) Track Extension, Fitting & Ambiguity Resolution**.

**Demonstrators** have been developed to start understanding the optimal configuration of the system.




### 4.1 Fast-Tracking CPU Demonstrator

A **novel software approach** for fast track reconstruction has been developed [8], leading to a **factor 8 speedup** with respect to the default reconstruction on earlier ITk layout.

**Data Preparation**: algorithms as clustering have been optimized e.g. cutting by half the number of neighboring pixels to look at.

**Track Seeding & Pattern Recognition**: the search for track candidate seeds is performed only on five pixel layers.

**Track Extension, Fitting & Ambiguity Resolution**: for the track parameter estimation the fast Kalman Filter track fit is used. The Ambiguity Resolution algorithm is omitted (largest contributor to the overall track reconstruction time).

**The CPU demonstrator** provides **near offline-quality tracking performance** with requirements that are compatible with the available power and space.

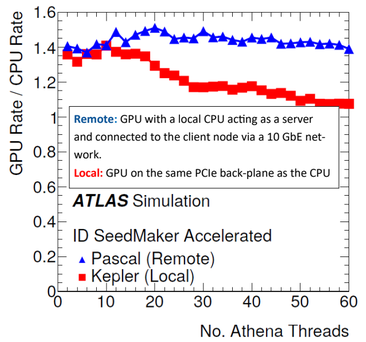
### 4.2 GPU Demonstrator

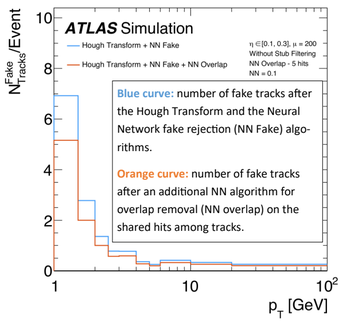
**Initial studies** were done for the currently used **ATLAS Inner Detector**, using a **pile-up of 46** and by Kepler (K80 from 2014) and Pascal (GP104 from 2018) GPUs, in comparison with a 14-core Intel Xeon E5-2695 CPU [6].

**Data Preparation** and **Track Seeding**: these compute intensive algorithms were implemented as CUDA modules.

The increase in events processed per second (rate) that can be achieved when GPUs are added to a CPU-only system depends on the fraction of the CPU workload that is exported to the GPU: the rate could be doubled if it were possible to export 50% of the CPU work-load to GPU.

**These studies** shall be taken as **an indication that the software can be successfully adapted** to other architectures in order to perform a full cost/benefit evaluation with current and future GPU models.




### 4.3 FPGA Demonstrator

A tentative **reconstruction flow for ITk data** has been developed **in FPGA** to demonstrate its feasibility [7]: lightweight CPU-based load-balancing **software** would **route** a particular **event to an available FPGA**, **where all** the EF tracking **steps are implemented**. The target FPGA model (wherever possible) was a Xilinx Alveo U250.

**Data Preparation**: ITk data decoding and clustering

**Track Seeding & Pattern Recognition**: space-points and stubs finding, followed by Hough Transform (HT) algorithm.

**Track Extension, Fitting & Ambiguity Resolution**: series of duplicate and fake removal steps followed by an 8-layer track fit.

Preliminary estimates for the resource usage of the different algorithms have been made: **HT** and **Track Fitting** seems to be the most **resource consuming** steps. To be noticed that the **HT algorithm performance** for the regions in the central part of the detector is **comparable to the offline software.**

**The FPGA demonstrator includes** a resource estimate for the **HT algorithm** which shows to **fit** within the **target FPGA**, **software aspects** that take advantage of novel developments in fast tracking software for ATLAS, and **reduced power consumption**.