A 25 Gbps VCSEL driving ASIC For Detector Front-end Readout

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Design

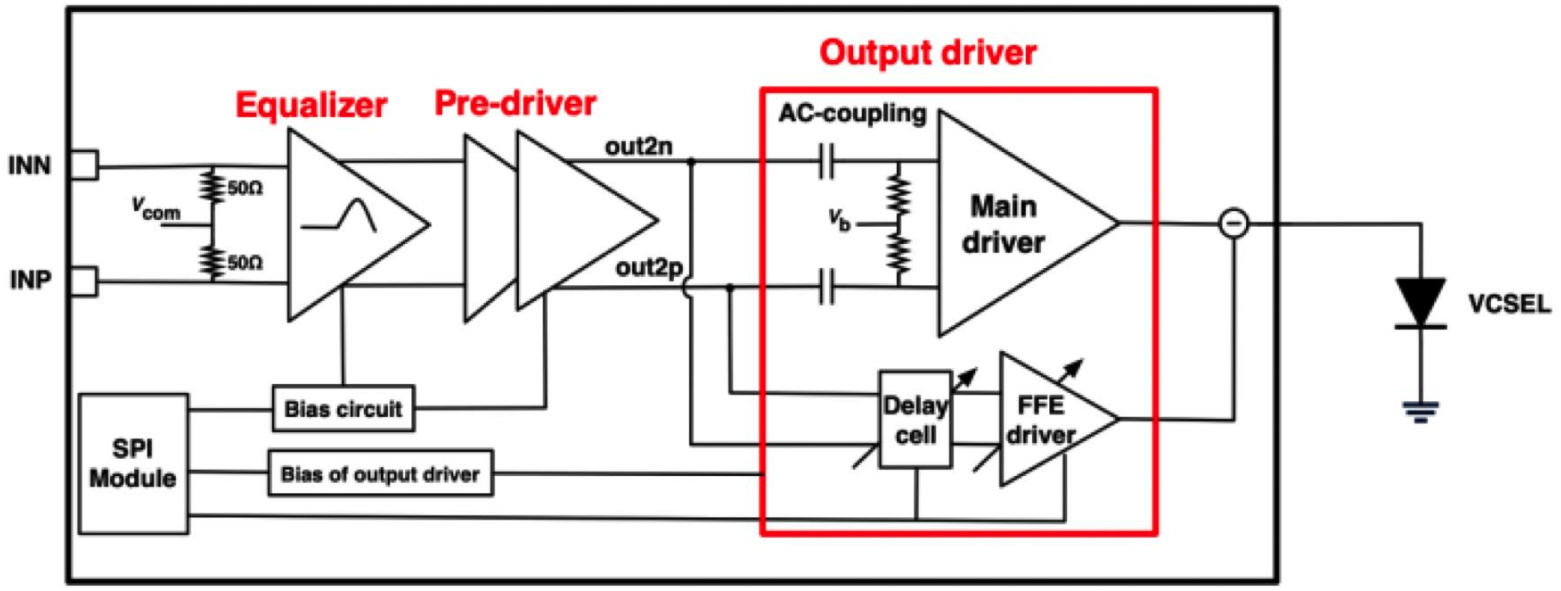

Fig.1 Block diagram of the 25 Gbps VCSEL driving ASIC

It includes an input equalizer stage, a pre-driver stage and a novel output driver stage. The input equalizer stage receives a pair of 25 Gbps differential CML signals with appropriate peaking effect. The pre-driver stage receives the signals from the input equalizer stage, and further amplifies the differential signals with sufficient gain and bandwidth (>18 GHz) for the output driver stage. Following the pre-driver stage, the proposed output driver stage includes a main driver, an adjustable delay cell and an emphasis driver (FEE driver). The main driver converts the amplified differential voltage signals from the pre-driver to single-ended high speed current signal, and drives the external VCSEL.

Test results

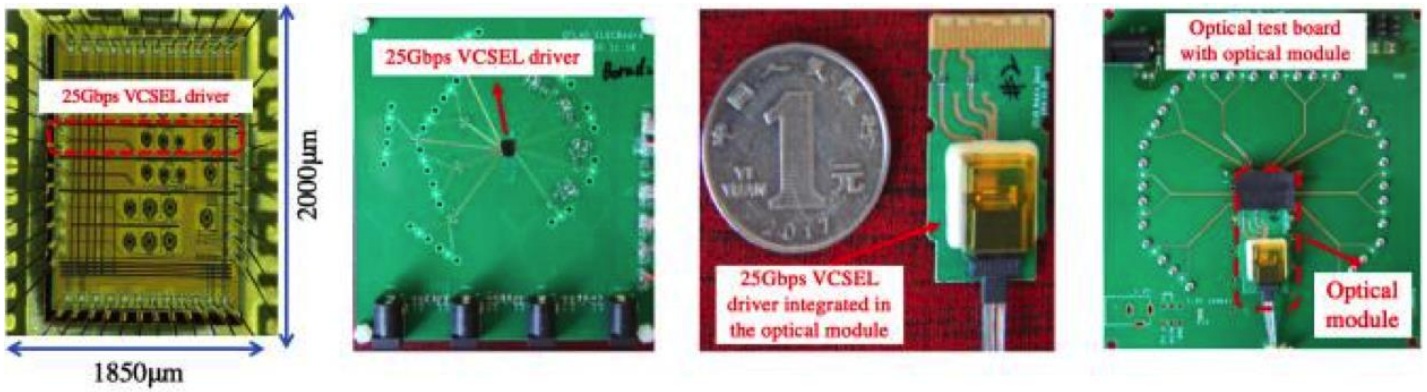

Fig.2 Chip micrograph and test boards (a)chip micrograph (b)electrical test board (c)optical module (d)optical test board

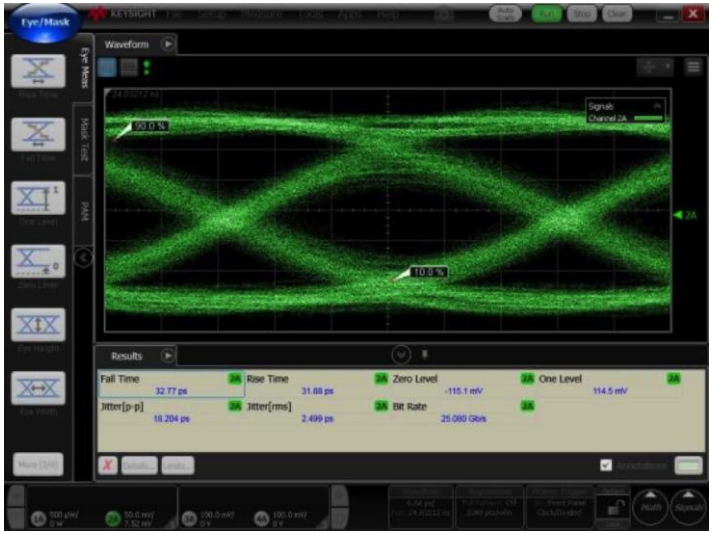

Fig.3 Electrical eye diagram

RMS jitter: 2.5ps

PP jitter : 18.2ps

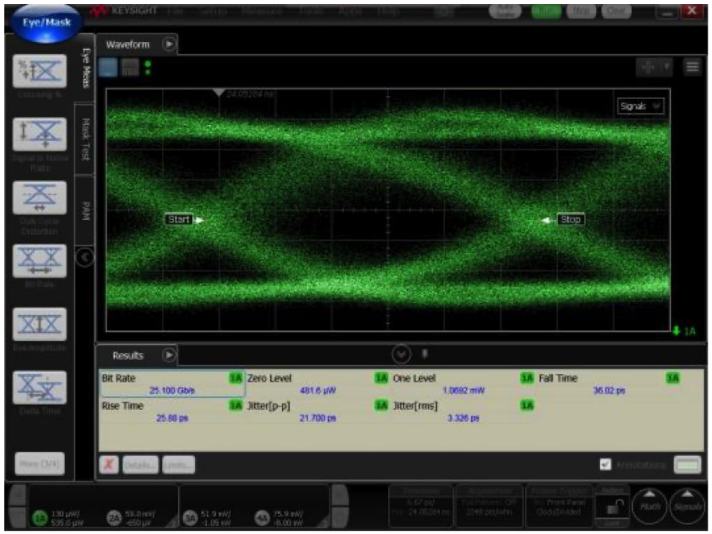

Fig.4 Optical eye diagram

RMS jitter: 2.9ps

PP jitter : 19.5ps