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A 25 Gbps VCSEL Driving ASIC for Detector Front-end Readout

This paper presents the design and the test results of a 25 Gbps VCSEL driving ASIC fabricated in a 55 nm CMOS technology for detector front-end readout. This VCSEL driving ASIC is composed of an input equalizer stage, a pre-driver stage and a novel output driver stage. The input equalizer stage adopts a 5-step CTLE structure to compensate the high frequency loss at the PCB traces, bonding wires and input pads. It can boost maximum up to 5.8 dB at 18 GHz while providing a DC gain of 10.7 dB. To meet both the gain/bandwidth requirements and the area restriction, the pre-driver stage adopts the inductor-shared peaking technology and the active feedback structure. The total gain and the overall bandwidth of the pre-driver stage are better than 18 dB and 19.5 GHz at all process corners, respectively. The proposed output driver stage uses the double feedforward capacitor compensation, T-coil technique and the adjustable FFE pre-emphasis technique to improve the bandwidth. This VCSEL driving ASIC has been integrated in a customized optical module with a VCSEL array. Both the electrical function and the optical performance have been fully evaluated. The output optical eye diagram has passed the eye mask test at the data rate of 25 Gbps. The peak-to-peak jitter of 25 Gbps optical eye is 21.7 ps and the RMS jitter is 3.3 ps.

Minioral

Yes

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No

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