The Design of Low-Jitter Delay-Locked Loop for Ultra High-Resolution Time Measurement

M. Feng, Z. Zhao, X. Wei, J. Wang, R. Zheng, F. Xue, Y. Hu.

***Abstract*—This work is the demand for the fixed and low-jitter delay generation circuit in the time measurement system. As the timing resolution required by modern electronic products constantly improve, the multi-phase clock sampler and the vernier delay line have become frequently-used structures of the ultra-high-resolution time-to-digital converter (TDC), which are both implemented with the fix delay provided by the delay-locked loop (DLL). This work presents a low-jitter and small-static-phase-error DLL, which is composed of an incorrect lock prevention circuit, a phase detector, a charge pump, a voltage-controlled delay line and auxiliary circuits. The proposed charge pump in this work is equipped with the wide-swing cascode current mirror, the clamping amplifier and the virtual switch to eliminate the influence of non-ideal effects. A new current-starving delay cell is also proposed to expand the adjustable range of the control voltage. The proposed DLL is designed and fabricated with standard 180 nm CMOS process. According to simulation results with 100MHz reference clock, this DLL can get the rms jitter better than 15 ps and the static phase error better than 40 ps. The power consumption of the overall circuit is about 3.3mW.**

***key words*—TDC, DLL, low-jitter, small-static-phase-error.**

I. Introduction

In the high-energy physics experiment, the time of flight (TOF) of the charged particle is one of the most important information for particle identification. Thus, the high-resolution time-to-digital converter (TDC) is required to identify various particles as accurately as possible. [1] The time interpolating is a kind of TDC whose resolution is determined by the number of phases of the delay-locked loop (DLL). The vernier delay line is another high resolution TDC, which can be realized with two DLLs whose unit delays can be locked to two close values. Based on the high resolution TDC design requirements, we propose a low-jitter and small-static-phase-error DLL in this paper. On one hand, the proposed DLL can be applicated to the time interpolator and the vernier delay line to greatly improve time resolution. On the other hand, the feedback in DLL can fix the phases of generated multi-phase clocks with low-jitter, thus we can get good measure linearity of TDC. So that a low-jitter DLL is of great significance to the high-resolution time measurement system.

II. Circuit Design

The proposing DLL is mainly composed of a lock controller(LC), a phase detector (PD), a charge pump (CP), a low pass filter (LPF), a voltage-controlled delay line (VCDL) and start-up circuit. The block diagram of DLL is shown in Fig. 1. The reference clock is the only input signal of DLL, which passes through the VCDL to generate 16 evenly distributed multi-phase clocks.

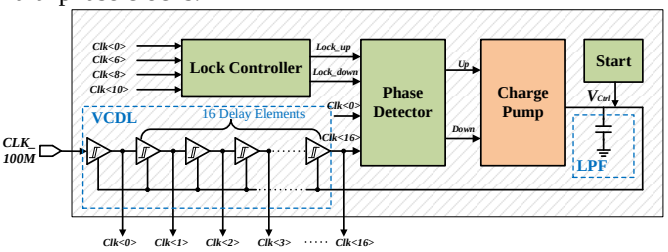

Fig. 1. The block diagram of the proposed DLL ASIC

This DLL uses the incorrect lock prevention circuit proposed in [2]. The first and second multi-phase clocks generated by the VCDL are fed into the PD and the control signal is generated to adjust the output of CP, which is denoted by the control voltage. The control voltage adjusts the delay of the output clocks of VCDL. Finally, the input phase difference of PD approaches 0, and the dynamically balanced state of DLL is realized, which make sure the multi-phase clocks and control stable enough to provide to TDC.

The charge pump adopts drain-switch structure, as shown in Fig. 2. In order to reduce the mismatch between charge and discharge currents caused by channel-length modulation, a wide-swing cascode current mirror is used to increase the output impedance of current source. An amplifier for voltage clamping is added to eliminate charge-sharing. The charge injection can be counteracted with the complementary switch and the virtual switch. It was found that the clock feed-through effect had been effectively suppressed when the size of virtual switch were set to be the half size of the real switches [3]. As shown in Fig. 3, the bias of the charge pump adopts supply independent structure, then the bias voltage can be adjusted with an off-chip resistor. The proposed current-starving delay cell is shown in Fig. 4, in which the extra biasing transistor (M7、M8) is added to extend the adjustable range of control voltage.

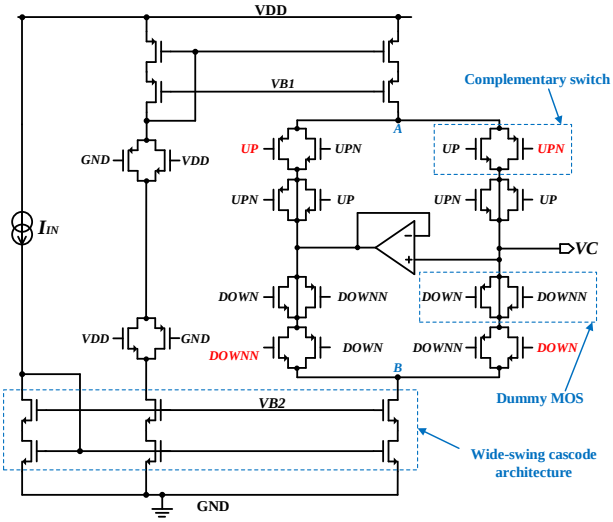

Fig. 2. The schematic diagram of the proposed charge pump

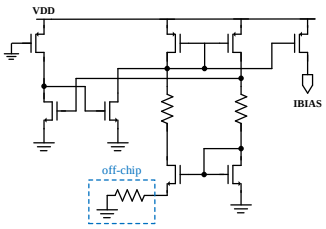

Fig. 3. The proposed bias of CP

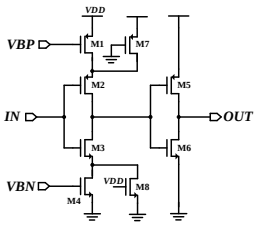

Fig. 4. The proposed delay cell

III. Simulation Results

The DLL proposed in this paper is designed and implemented with standard 180 nm CMOS process. The layout is shown in Fig. 5. The DLL is simulated with the 100MHz reference clock. Fig. 6 is delay-voltage characteristics of VCDL under different processes, voltages and temperatures (PVT), which shows that the VCDL can cover the range of 6.6 ns to 11.2 ns. The acceptable input clock frequency is 90 MHz to 150 MHz. The simulation results under different PVT conditions are concluded in Table I. It can be observed that the circuit under the condition of SS/125℃/1.62V spend the minimum time to reach locked state. The worst edge-to-edge rms jitter is 14.8 ps and the worst static phase error is 39.9 ps. The power consumption of the overall circuit is about 3.3mW.

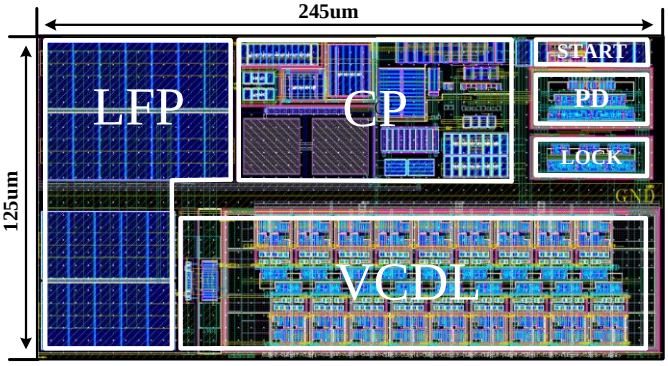

Fig. 5. The DLL chip layout

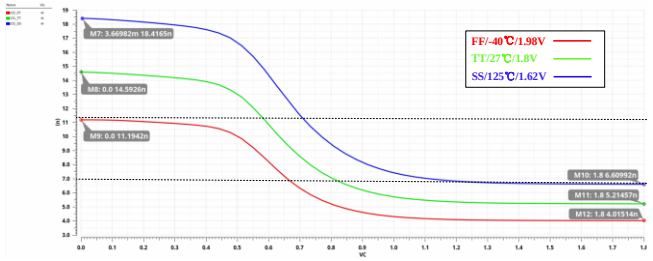

Fig. 6. The simulation of delay-voltage characteristics of VCDL

TABLE I THE SIMULATION RESULTS UNDER DIFFERENT PVT CONDITIONS

Parameters		FF/-40℃/ 1.98V	TT/27℃/ 1.8V	SS/125℃/ 1.62V
Static Phase Error (ps)		39.9	20.6	14.3
Locking Time (us)		17.1	15.6	14.2
Jitter (rms/peak-peak)	Jee(ps)	14.8/91.6	13.0/80.5	11.3/69.9
	Jc(ps)	19.8/122.6	17.5/108.4	15.4/95.1
	Jcc(ps)	34.2/211.7	30.0/187.3	26.6/164.4

Acknowledgment

The authors would like to thank the financial support in part by the National Natural Science Foundation of China under Grant No. 11835007, No. 11835008 and No. 12105224, in part by the Natural Science Foundation of Shaanxi province under Grant No. 2021JQ-118 and No. 2021JM-075, Innovation Foundation for Doctor Dissertation of Northwestern Polytechnical University, CX2021025.

References

[1] Y. Xie，C. Chen，M. Wang, et al. Particle detectors and data acquisidon．Beijing: Science Press，2003.

[2] S. Ok, K. Chung, J. Koo, and C. Kim, "An Antiharmonic, Programmable, DLL-Based Frequency Multiplier for Dynamic Frequency Scaling," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 18, no. 7, pp. 1130-1134, 2010.

[3] B. Razavi, Design of analog CMOS integrated circuits. Tsinghua University Press, 2005.