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Clock distribution system using IOSERDES based clock-duty-cycle-modulation

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The author has developed a clock distribution system for front-end electronics synchronization using the clock-duty-cycle-modulation (CDCM) [1] based transceiver (CBT), which is realized by the Xilinx Kintex-7 IOSERDES primitives. In addition, the link layer protocol called the MIKUMARI link was developed. The link protocol can transfer not only data using frame structure but also a one-shot pulse with a fixed latency to a destination. A clock distribution system consisting the CBT and the MIKUMARI link sends the clock, data, and the pulse through a pair of TX and RX lines. Thus, the system is independent from an FPGA high-speed serial transceiver. The system will be introduced a new standard system for clock, trigger, and synchronous command distribution in J-PARC hadron experiments.
The author tested the CBT and the MIKUMARI link using a general-purpose FPGA module. Two FPGA modules were connected by an optical fiber. In the slave module, the CDCM encoded clock signal was fed into a mixed-mode clock manager (MMCM) in FPGA and an external jitter cleaner IC, CDCE62002, to recover the clock. During the tests, 8-bit incremental data is continuously transferred. The measured random jitters of the recovered clocks were 5.0±0.1 ps and 5.2±0.1 ps for CDCM-10-1.5 and CDCM-10-2.5 [1], respectively.
In this contribution, the author will report the design of the CBT and the MIKUMARI link. The performances for several clock frequencies will also be discussed.
[1] D. Calvet, IEEE TNS vol. 67, Issue 8, Aug. 2020, 1912-1919.

Minioral

Yes

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