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An eFPGA core embedded in a pixel chip and SEU reinforcement design

In high energy physics detection technology, X-ray polarization detection experiment is an important means to study astrophysics. One of the most commonly used two-dimensional detectors is the photoelectron track pixel detector. The readout electronics system of pixel detector is composed of several modules. With the development of high energy experiment, the readout electronics system of pixel chip becomes more and more complex. Based on the rapid development of semiconductor manufacturing technology, it is possible to make pixel chip readout electronics system into SOC chip. In order to improve the programmability and processing efficiency of pixel chip readout electronics system, an embedded eFPGA core is designed in this paper. eFPGA is a embedded FPGA integrated in SoC, which is a small SCALE FPGA in essence. It is programmable and has the speed only second to that of asIC. The eFPGA core uses Verilog hardware description language to model several basic element modules of eFPGA, and the scale can be configured. For eFPGA core, a special bit stream generation software VTB is designed. The software can complete logic synthesis, process mapping and so on. At the same time, in space radiation environment, semiconductor devices are easy to produce single particle flip (SEU) effect, so this paper designs a SEU radiation reinforcement circuit for the configuration register in eFPGA core. In this circuit, error detection and recovery circuit are added to the traditional three-mode redundant circuit, so that the circuit can recover the flipped register, and enhance the radiation resistance of eFPGA core.

Minioral

Yes

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No

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