The mircoTCA.4 fast control and processing board for generic control and data acquisition applications in HEP experiments

Jie Zhang[1,2], Cong He[1,2], Aoqi Su[3], Manhao Qu[3], Wei Wei[1], Xiaoshan Jiang[1,2]

1. Institute of High Energy Physics(IHEP), Chinese Academy of Sciences(CAS)
2. University of Chinese Academy of Science
3. Zhengzhou University

MicroTCA.4 Fast Control and Process board (u4FCP) is an FPGA-based MicroTCA.4 compatible Advanced Mezzanine Card (AMC) targeting generic clock, control and data acquisition in High-Energy Physics(HEP) experiments.

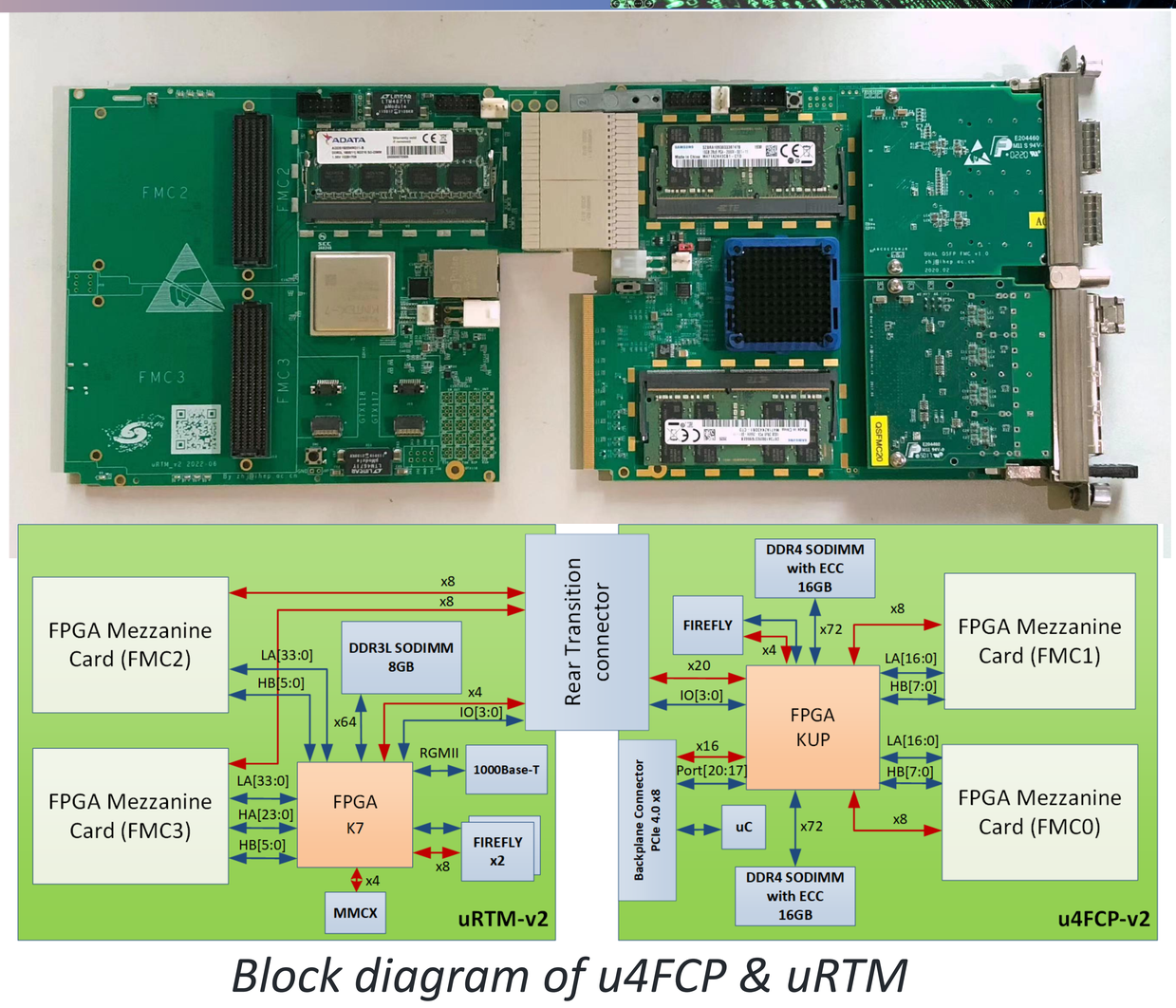
MicroTCA.4 Rear Transition Module (uRTM) is a rear transition module in the rear of the crate to increase the I/O capability of the u4FCP. The u4FCP and uRTM are connected through fabric connectors in the upper area above the standard µTCA backplane area, defined as Zone 3. The pin assignment is compatible with the Zone 3 recommendation D1.4 for digital applications.

u4FCP & uRTM are conceived to serve a mid-sized system residing either inside a MicroTCA crate or stand-alone on desktop with high-speed optical links or Ethernet to PC.

The I/O capability of u4FCP & uRTM can be further enhanced with four VITA-57.1 FPGA Mezzanine Cards (FMC) through the high-pin-count sockets.

Hardware

A block diagram of the u4FCP and uRTM is shown below. The red lines are high-speed serial links connected to the gigabyte transceivers (GTY/GTH/GTX) of the FPGA. The blue lines are the general input/ outputs connected to the High Performance (HP), High Range (HR) or High Density (HD) banks of the FPGA.

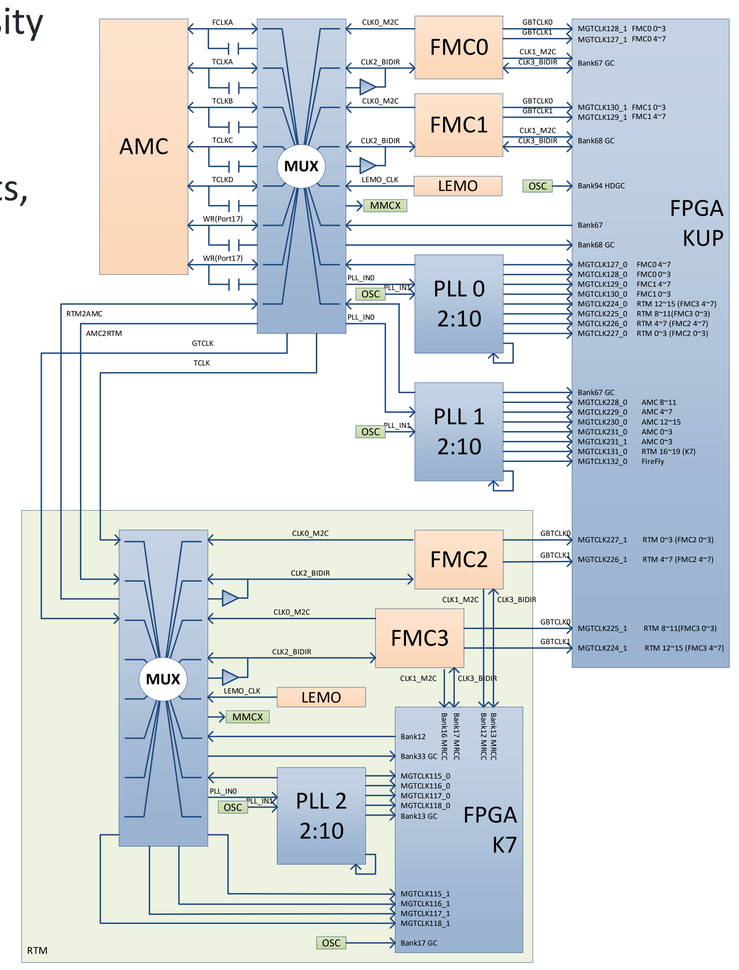


Block diagram of u4FCP & uRTM

FMC connection

Although the FMC standard defines LA, HA, HB and DP differential ports, only parts of them are connected to FPGA duo to limited IO resources. The table below summarizes the connections of FMC

FMC	HPC							
	LPC							
	LA[16:0]	LA[33:17]	DP[0]	DP[9:1]	HA[16:0]	HA[23:17]	HB[16:0]	HB[21:17]
FMC0	HP bank (1.0V~1.8V)	-	1 GTY	7 GTY	-	-	HD bank (3.3V), 8 ADC Channels	-
FMC1	HP bank (1.0V~1.8V)	-	1 GTY	7 GTY	-	-	HD bank (3.3V), 8 ADC Channels	-
FMC2	HR bank (1.2V~3.3V)	HR bank (1.2V~3.3V)	1 GTH	7 GTH	-	-	HR bank (2.5V), 5 ADC Channels	-
FMC3	HR bank (1.2V~3.3V)	HR bank (1.2V~3.3V)	1 GTH	7 GTH	HR bank (1.2V~3.3V)	HR bank (1.2V~3.3V)	HR bank (2.5V), 5 ADC Channels	-



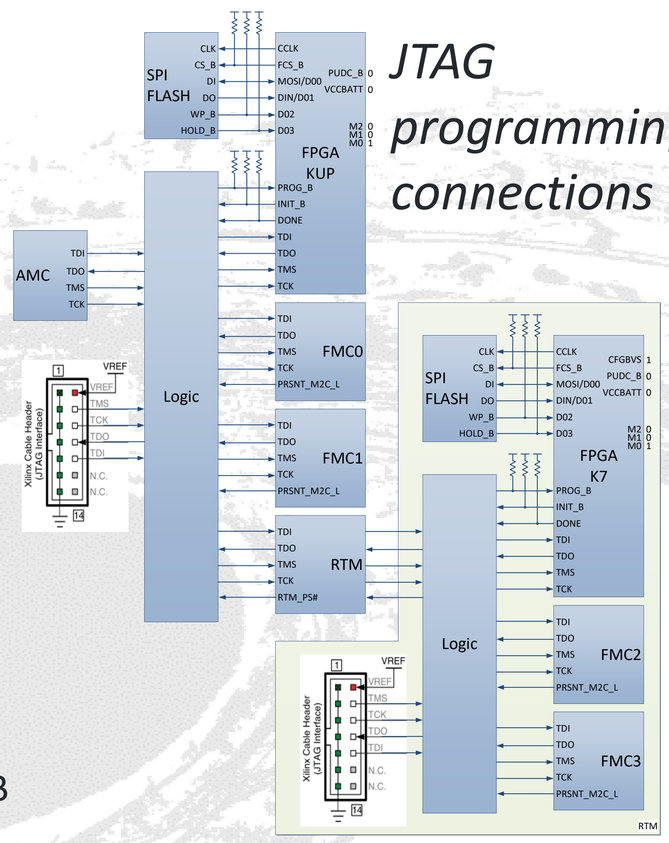
Clock generation and distribution

Clock Features

Based on cross-point switches and programmable clock multipliers, the clock distribution for u4FCP & uRTM offer a large selection of input clock sources (e.g. the LEMO connectors in the front/rear panel, the AMC clocks, the FMC clocks, or onboard oscillators). The clean clock is used as a reference clock for the gigabyte transceivers. This makes the u4FCP & uRTM give users the possibility of implementing various high speed serial data protocols for custom applications.

JTAG

Users can access to the FPGA through the MicroTCA crate or JTAG header. A configurable logic circuit acts as a bridge selecting the JTAG master source between the JTAG header and AMC/RTM JTAG lines. When an FMC card is attached to u4FCP & uRTM, the circuit automatically adds the attached device to the JTAG chain as determined by its FMC_PRSNT_M2C_B signal.



JTAG programming connections

Use case

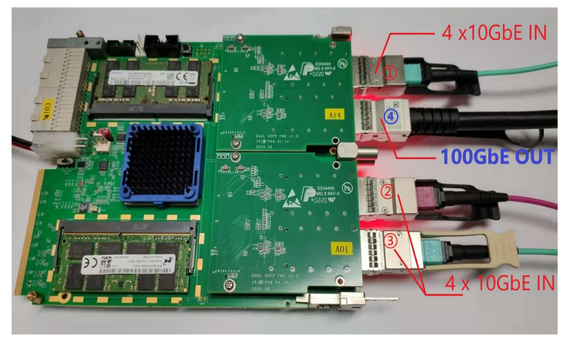
The hardware has benefited from the multiple high-speed data links of FPGA, the u4FCP is adopted in the SHINE pixel detector. The prototype system was assembled with 12 channels and achieves a peak rate of 94 Gbps.

More details:

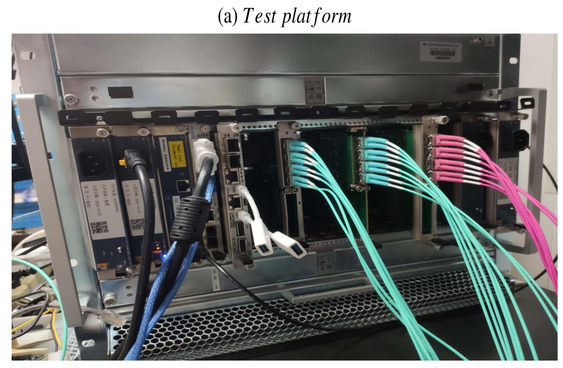
https://github.com/palzhj/u4FCPv2

Ref:

1. FPGA-based 100G network readout solution for SHINE pixel detector
2. An implementation of module management controller for MicroTCA data processing system



(a) *Test platform*



(b) *N.A.T MicroTCA crate*