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The Real-Time System for Distribution of Clock, Control and Monitoring Commands with Fixed Latency of the LHCb experiment at CERN

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The LHCb experiment has gone through a major upgrade for LHC's Run-3, scheduled to start in the middle of 2022. The entire readout system has been replaced by Front-End and Back-End electronics that are able to record LHC events at the full LHC bunch rate of 40MHz.

In order to maintain synchronicity across the full system, clock and control commands are originated from a single Readout Supervisor (SODIN) and distributed downstream through a Passive Optical Network (PON) infrastructure, reaching all Back-End cards of the readout system, via a two-level hierarchy and utilizing PON splitters. An FPGA-based firmware core, called LHCb-PON and based on the CERN TTC-PON, is instantiated on SODIN and all Back-End cards and provides the communication protocol while ensuring a stable distribution of control commands within the readout period of 25 ns as well as a clock signal with fixed and deterministic latency with a precision of a few hundreds of picoseconds. This is achieved by the firmware backbone that provides clock recovery and ensures the transmission of a control word downstream with fixed latency.

Additionally, the LHCb-PON also provides monitoring functionalities over the upstream link, with less strict timing requirements, connecting multiple Back-End cards to the central SODIN. This is achieved by having each Back-End card send data upstream through a time division multiplexing scheme.

This paper describes the implementation, measurements and results from the usage of the system during the start-up of Run 3 at the LHC.

Minioral

Yes

IEEE Member

No

Are you a student?

No

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