Fast-Settling high input dynamic range Automatic Gain Control Front-end circuit for particle detect

PingYang[1,*],YunqiDeng[1],XiaoWang[1],GuangmingHuang[1],ZhuangYue[1]
PLAC, Key Laboratory of Quark & Lepton Physics (MOE), Central China Normal University, Wuhan, China
* pingyang@ccnu.edu.cn

ABSTRACT

In this paper, a variable gain amplification chain is designed using GMSC 0.13um CMOS process to cover signal measurement with a large dynamic range. The post-simulation result shows that the gain dynamic range is -6.6dB ~19.73dB, covering 60dB the input dynamic range. The -3dB bandwidth is about 20MHz, and the gain adjustment time is less than 5ns. The nonlinear error is 0.27% for the high gain gear and 1.29% for the low gain gear. This method can cover a large input dynamic range and save power consumption by using only one analog-to-digital conversion and single path.

Objective

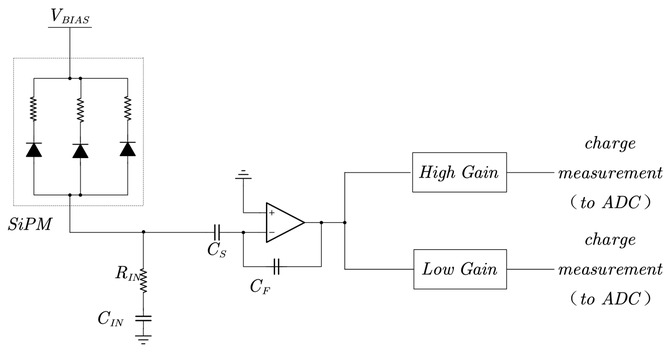


Figure 1: traditional SiPM readout system

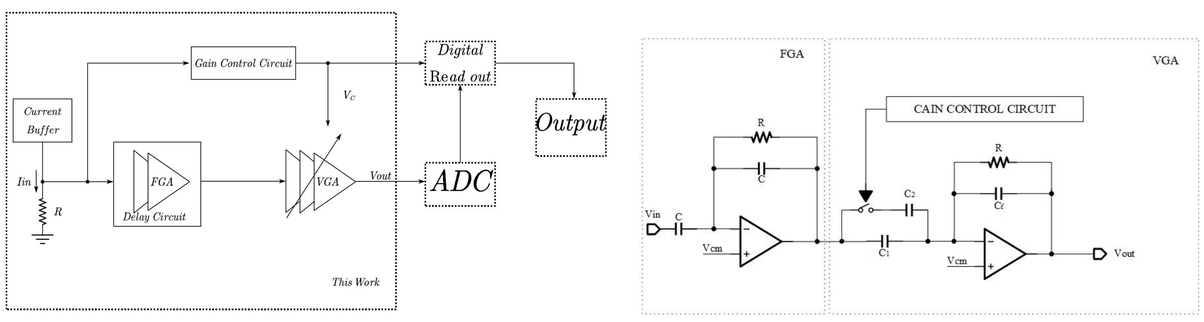
In high-energy physics experiments, the particles generated after particle collision move randomly, and the energy is uncertain, so the signal output by the front-end sensor SiPM of the zero-angle calorimeter is a current pulse signal with random amplitude.

Figure 1 shows a typical SiPM readout system, traditional SiPM readout circuits use two paths to cover a large dynamic range, which will cause a lot of power consumption and area. Therefore, this paper designs an AGC based on a new control system, which consists of delay circuit、variable gain amplifier 、current buffer and gain control circuit.

SiPM readout requirements

- The smallest signal we handle is 1.4mV and the largest is 1.4V ,we should set a suitable gain for the signal .
- The dynamic range of the signal covers 1000 times.
- The random pulse signal we process is very fast with a pulse width of only 10ns,the particle collider frequency is 1MHz .
- The SNR of system should be as large as possible,system linearity should be good to cover a large dynamic range.

Method



(a) (b)

Figure 2: (a)Variable Gain Amplifier Circuit Architecture (b)VGA circuit diagram

The variable gain amplifier circuit adopts a feedforward method.(Figure 2(a)).The working principle is as follows:

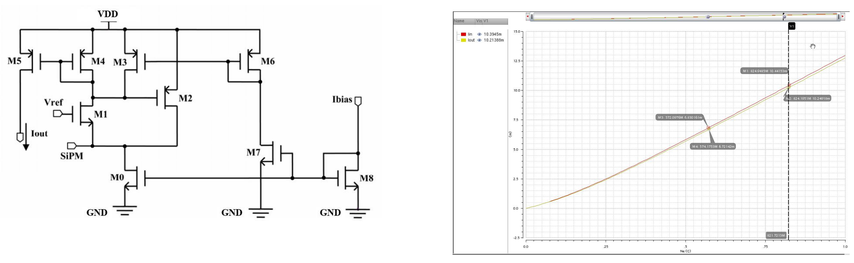
Step1: In order to avoid the small signal being lost, the initial gain is set to 20dB.

Step2: If the signal exceeds the setting threshold, a signal is given to the VGA via the comparator and D flip-flop to switch it to the low gain.

Step3: After the above steps are completed, the adjusted signal will be sent to the ADC module for processing, and Read out the results of the ADC module and the gain gear value. Then reset the gain gear and waiting for the next pulse signal.

As shown in Figure 2(b),Since the system is a feedforward system, the most important thing is that the random pulse signal needs to be delayed to ensure that when the signal reaches the VGA, the adjustment of the gain gear has been completed, so the FGA is designed.

Current Buffer



(a) (b)

Figure 3: (a) current buffer circuit (b) Simulation results of current buffer following ability

Current buffer is used to isolate the large capacitance of SIPM and is designed to handle signals of 10 ns pulse width.The common gate structure has a low input impedance and allows a large dynamic range of current to pass through.

- Input Dynamic Range :10uA~10mA(60dB)
- Input Resistance:17Ω
- Power consumption:830uA
- Linearity is well

Layout

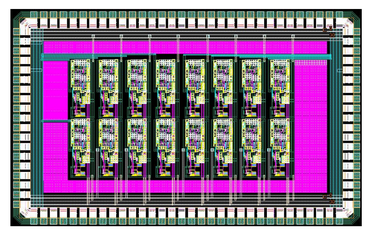


Figure 4:The circuit layout

- Channel : 16 channel
- Die size : 3520x2220um^2
- Two gain gears : The post-simulation result shows that the gain dynamic range is -6.6dB or 19.73dB

Post-Simulation Results

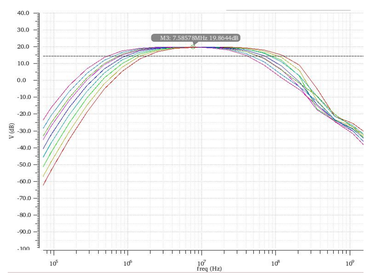


Figure 5(a)

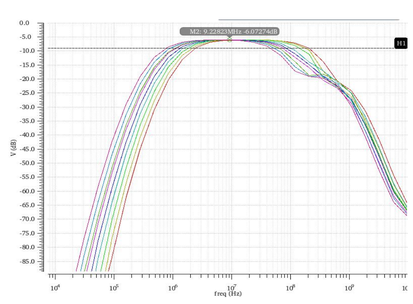


Figure 5(b)

Figure 5:The -3dB bandwidth of VGA (a)high gain (b)low gain

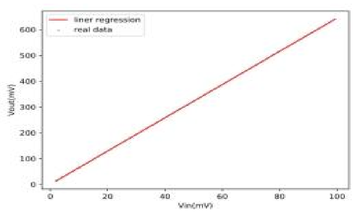


Figure 7(a)

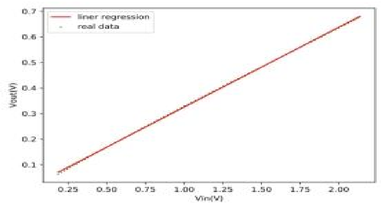


Figure 7(b)

Figure 7:Linearity of system (a)high gain Vout-Vin curve (b) low gain Vout-Iin curve

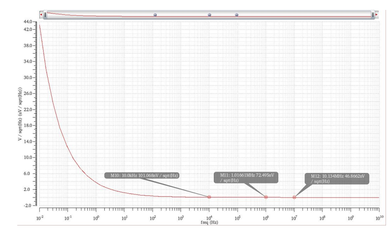


Figure 6 (a)

Figure 6(b)

Figure 6:The equivalent input noise@1MHz(a)high gain (b)low gain

- Figure 6 shows that the -3dB bandwidth of the high gain gear is 27.433MHz, and the -3dB bandwidth of the low gain gear is 82.037MHz
- The integral of the output noise of the high gain gear within 10kHz~300MHz is 1.416mV as shown in Figure 7.
- The nonlinear error(Figure 8) is 0.27% for the high gain gear and 1.29% for the low gain gear.

Summary

In this paper, a variable gain amplification chain is designed, the gain dynamic range is -6.6dB ~ 19.73dB, the -3dB bandwidth is greater than 20MHz and the gain adjustment time is less than 5ns. Covering 60dB input dynamic range(160fC~160pC), and perform a good linearity of the circuit, this AGC can be very effectively applied to SiPM front-end readout circuits that need to handle large input dynamic range signals.