

SiPM readout chip design for Heavy-ion Physics

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Abstract

Du to the small size, high gain, high time resolution, low operating voltage, and insensitivity to magnetic fields of the SiPM, the research of SiPM as sensor of the calorimeter has attracted a lot of attention. This work has designed 8-channel readout chips SICC0 and SICC1, which can simultaneously record the hit time and the energy information of particles. The SICC0 chip uses the traditional readout structure, including two readout paths, one path uses a TDC to record the arrival time and the other path uses front-end and ADC to save the energy information, three different gear selections are used for the energy detect to cover a large input dynamic range. The test results show the performance of the SICC0 is as expected. The linearity input range is from 10 µA to 3 mA, and the time resolution is less than 1LSB (25ns) which can be up to 5ns, the dynamic range is 25ns-6.375µs. To improve the time resolution, a new two-step TDC is designed on chip SICC1. The post simulation results show that the time resolution of the new TDC is 70 ps, the dynamic range is 640 ns, and the RMS is about 3 ps. The SICC1 chip is under testing now.

Structure and test results of the SICC0



Figure 1. Structure of the SICC0

- The chip contains two channels: Time measurement and Energy measurement
- The time measurement path is mainly composed of a hysteresis comparator and a counter-based TDC
- The energy measurement path mainly includes a capacitor proportional amplifier and a current buffer circuit







• The analog buffer is designed to drive large capacitive loads offchip



- The SICC0 is fabricated in 130nm CMOS technology
- The dimension of SICC0 is
 - 1.865mm x1.970mm

Figure 2. The Layout of SICC0



Figure 5. The test results of the current buffer using the SiPM of Beijing Normal University @LED source



Figure 6. The TDC DNL test results of SICC0 chip @ 40MHz

- The test results of the current buffer are shown in Figure 5, using a LED source, the output of the current buffer is monotonic linear.
- ♦ The test results of the DNL of TDC is shown in Figure 6, operating at the normal working frequency of 40MHz, the time resolution is less than 25ns, and the dynamic range is 25ns-6.375µs.

Layout of the SICC1

Two_step TDC circuit



3 ps.

The SICC1 is also fabricated in 130nm CMOS technology The dimension of SICC1 is 1.065mm x 0.960 mm

Falling edge of input signal

Figure 7. Structure of the Two-step TDC circuit



Figure 8. DNL post-simulation results of

the Two-step TDC

The new two-step TDC is shown in Figure 7. It is designed to improve the time resolution. Figure 8 shows the post-simulation results of the two-step TDC circuit. The results show that the resolution of the TDC can be up to 70 ps, the dynamic range is 640 ns, and the RMS is about

Figure 9. Layout of the SICC1

Conclusion

Both of the SICC0 and SICC1 use the traditional readout structure, including two readout path, one path uses TDC to record the arrival time and the other path uses front-end and ADC to detect the energy. The test results of the SICC0 chip is as expected. To improve the time resolution, a new two-step TDC is designed on chip SICC1. The post simulation results show that the resolution of the TDC is 70 ps, the dynamic range is 640 ns, and the RMS is about 3 ps. The SICC1 chip is still under testing now and the optimization of the chip is also ongoing.