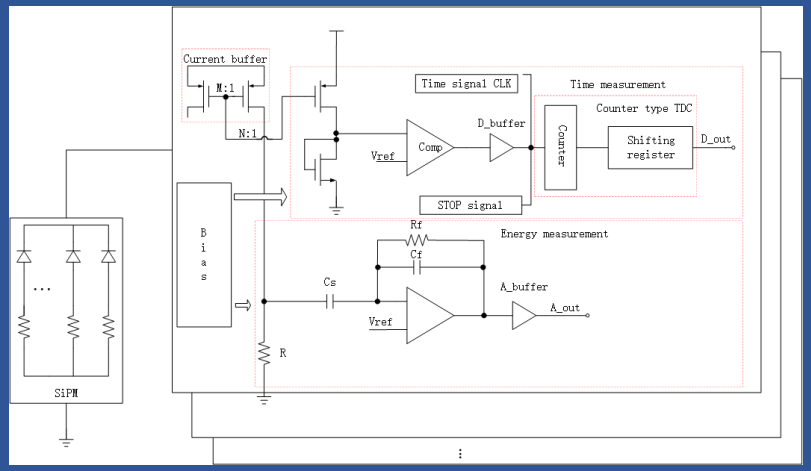
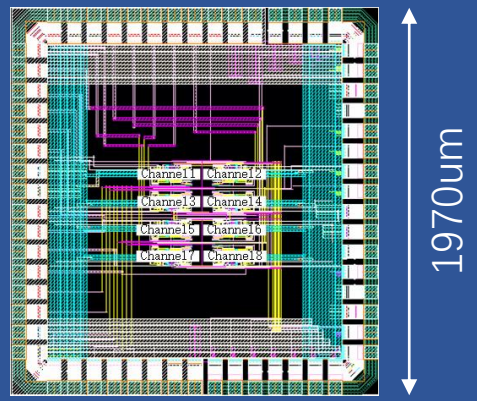
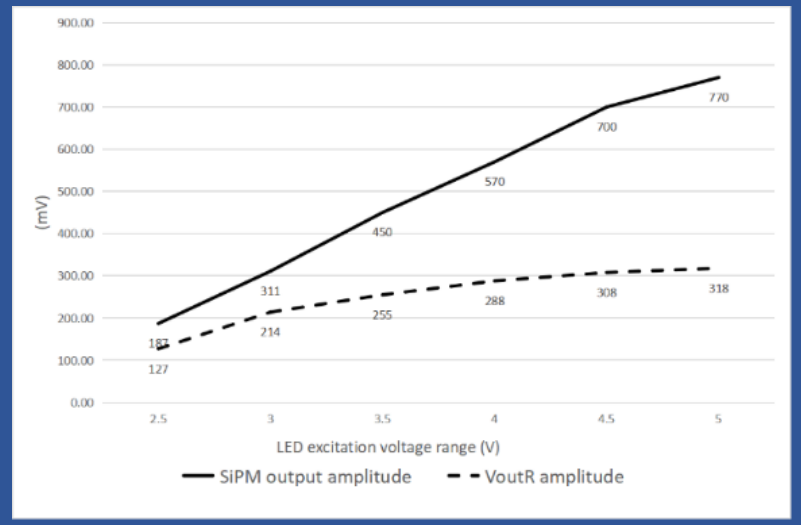
SiPM readout chip design for Heavy-ion Physics



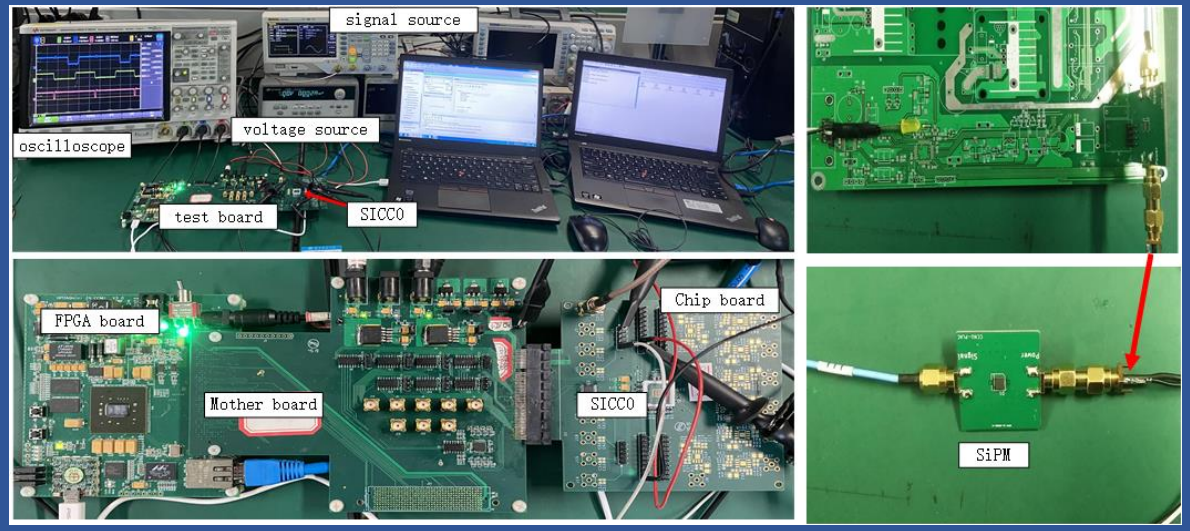
Block diagram of the SICC0 system



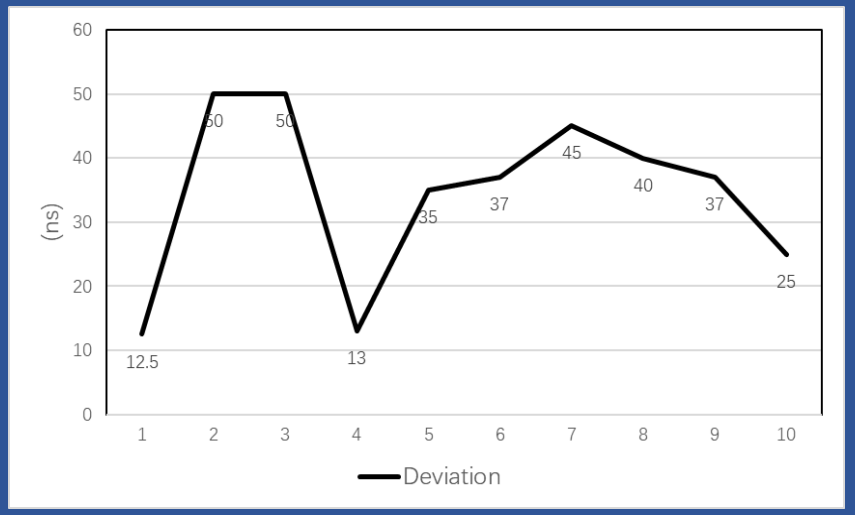
Layout of SICC0



Current buffer test results

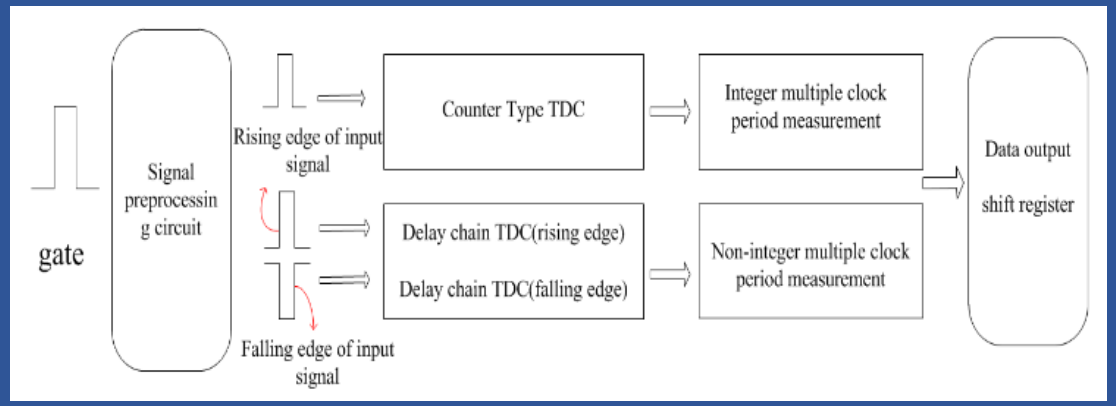


SICC0 test platform

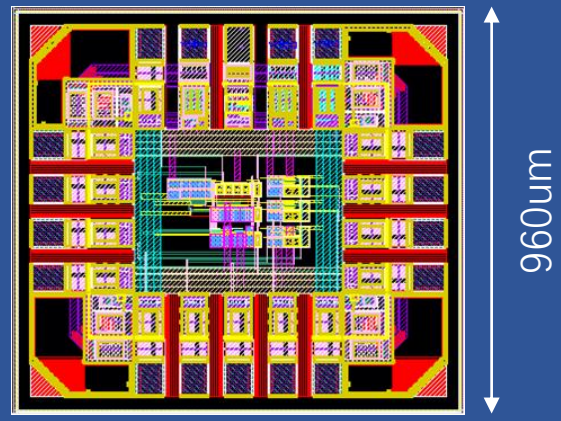


TDC DNL test results for SICC0 chip at 40MHz

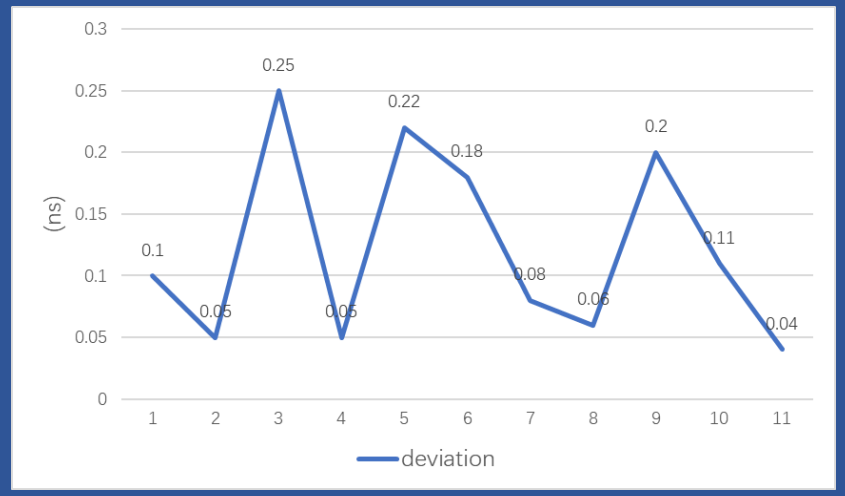
Two-step TDC Circuit



Two-step TDC circuit structure



Layout of SICC1



Post-simulation DNL results of a two-step TDC

The new two-step TDC is designed to improve the time resolution. The post-simulation results of the two-step TDC circuit show that the resolution of the TDC can be up to 70ps, the dynamic range is 640ns, and the RMS is about 3ps.