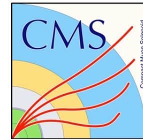
Upgrade of Trackers at LHC

Stefania Maria Beolé on behalf of



The 10th Annual
Large Hadron Collider Physics Conference
May 16-20, 2022

Charged particle tracker

- GOALS
  - Reconstruct charged particles trajectories = “tracks”
  - measure position of primary and secondary vertices
  - identify particles

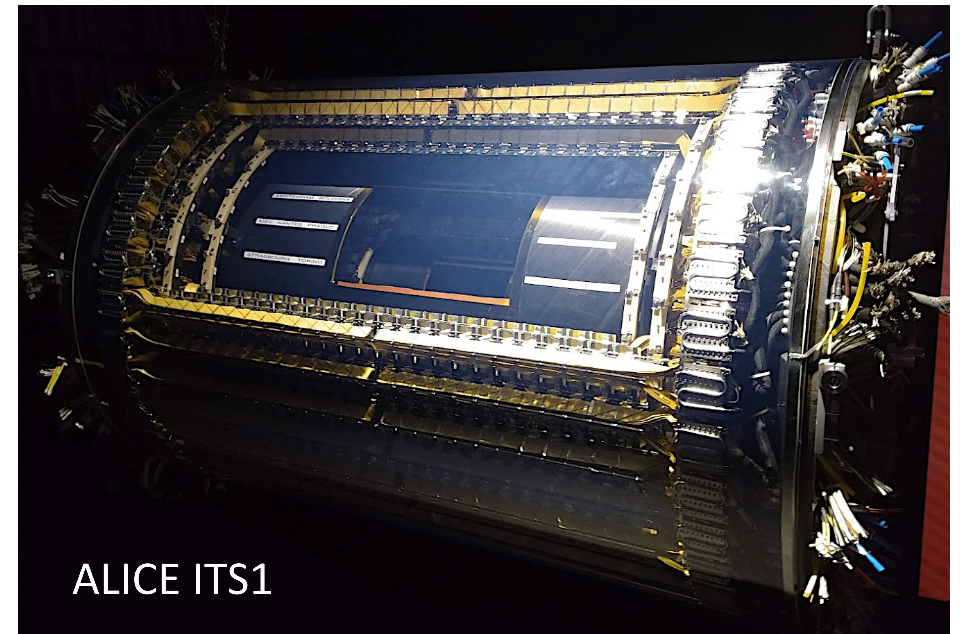
- Traditional silicon sensor technologies:
  - microstrips
  - hybrid pixels
  - drift detectors (ALICE only)

All trackers need to be upgraded (sensors replaced) to satisfy HL requirements:

- Peak luminosity: 5-7.5 x 10^{34} $cm^{-2}s^{-1}$
- Collision rates up to 1MHz
- Average pile-up (PU): up to ~200
- Total Ionizing Dose (TID) up to 1 Grad
- Particle fluence up to 2 x 10^{16} $n_{eq}cm^{-2}$ in the vertex region

- improved traditional technologies
- new tecnologies for present and future upgrades
  - CMOS sensors
  - 4D sensors

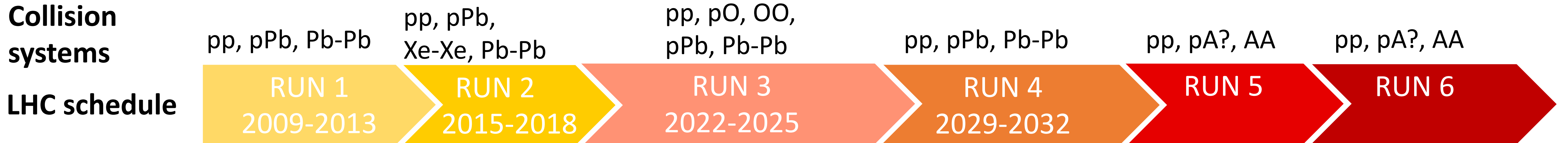
- Challenging requirements:
  - excellent pointing resolution
    - position resolution
    - material budget
    - distance from IP of the first layer
  - high data rates
  - radiation tolerant


ALICE ITS1

LHC Experiments upgrades program

Collision systems

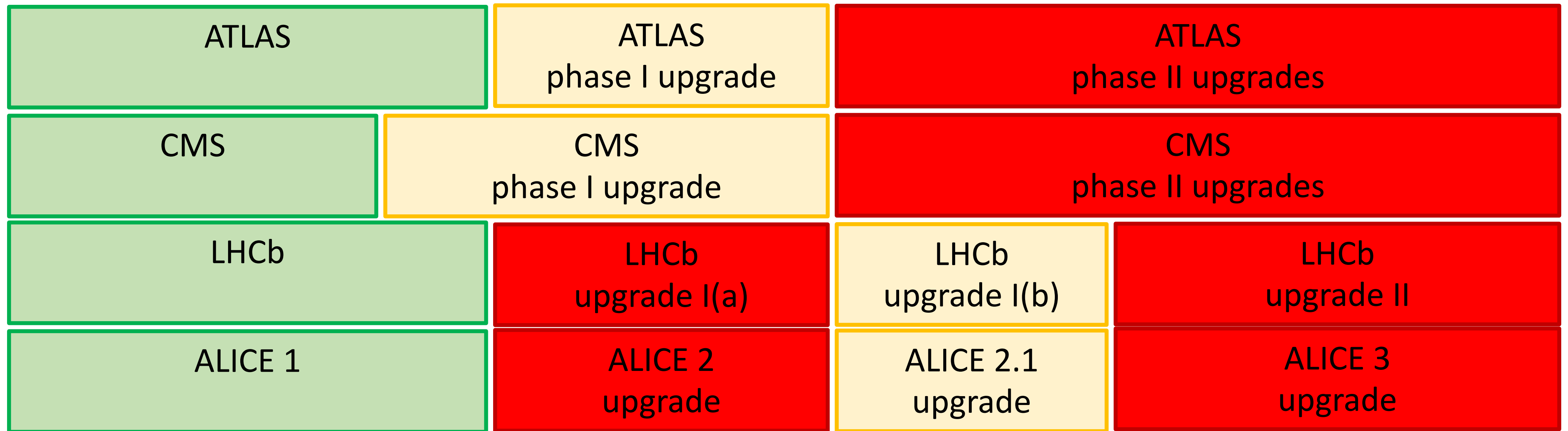
LHC schedule



High luminosity for ions (~$7 \cdot 10^{27}$ cm^{-2} s^{-1})

HL-LHC (~$5\text{-}7.5 \cdot 10^{34}$ cm^{-2} s^{-1})

Higher luminosities for ions

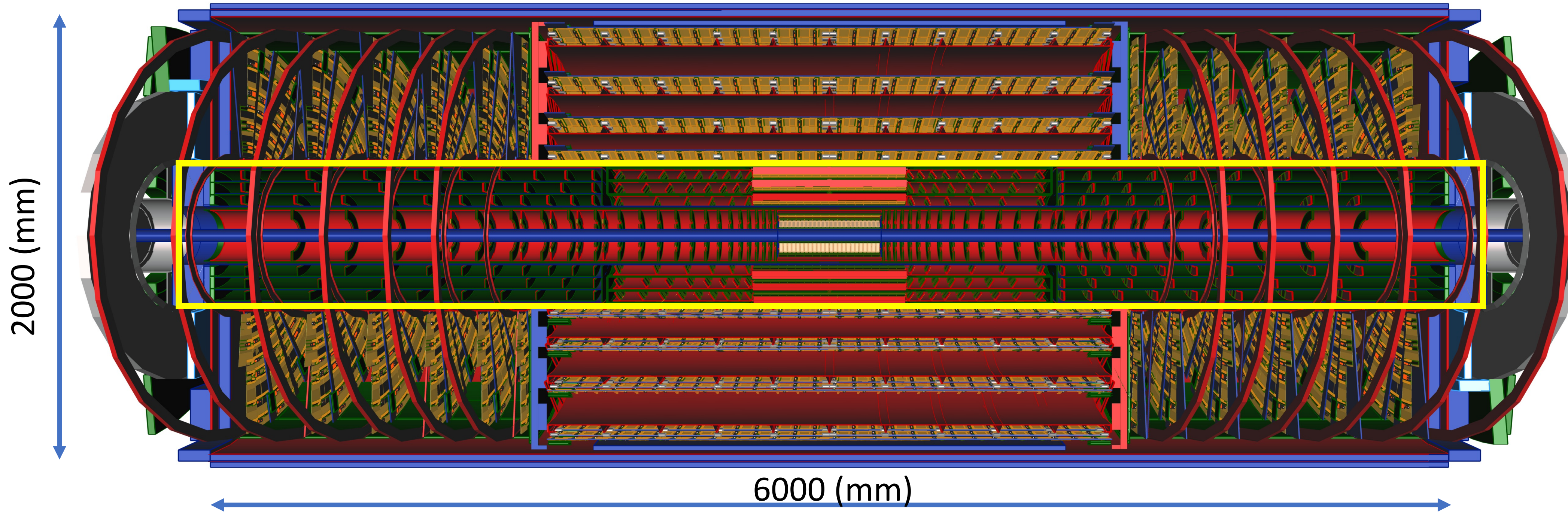


intermediate upgrade

major upgrade

ATLAS ITk

ATLAS EXPERIMENT



Technology:
- hybrid pixels
- microstrip

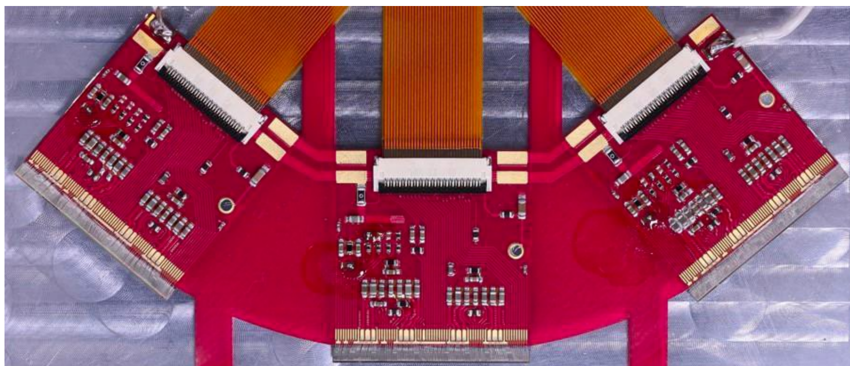
- Goal: maintain/improve RUN2 tracking performance
- Challenges:
  - Peak luminosity: 5-7.5 x 10^{34} $cm^{-2}s^{-1}$ → ~× 5-7
  - Average pile-up (PU): up to ~200 → ~× 5
- Layout
  - Factor of 2.7 larger than current ATLAS ID
  - coverage up to 4 η with at least 9 space point per track
  - 4 strip and 5 pixel (flat + inclined) barrel layers
  - 2x6 strip disks and a novel pixel ring structure

- New Pixel system
  - ~13 m^2 of active area (**~9200 modules**) 5.1 Giga-pixels
  - Impact parameter resolution improved by **finer segmented inner pixel layer (25×100 μm²) and reduction of material**
  - The two innermost pixel layers are replaceable (mitigate radiation damage)
- New Strip system
  - ~165 m^2 of silicon (**17888 modules**) ~60 Mega-channels

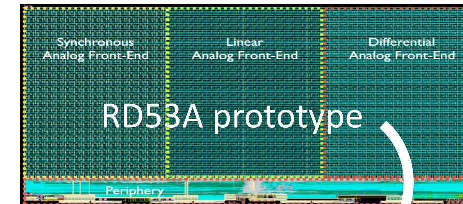
Technical Design Report for the ATLAS Inner Tracker Pixel Detector https://cds.cern.ch/record/2285585

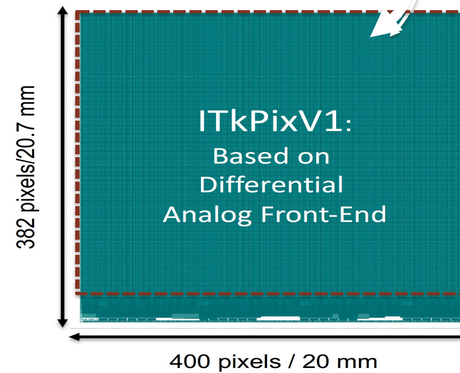
ATLAS: focus on pixel sensors and chips

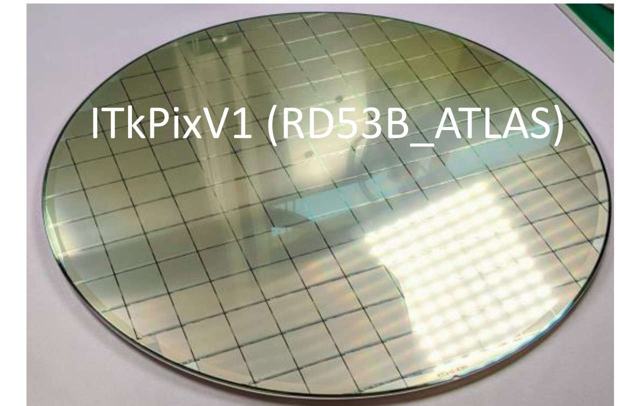
- **Sensors with 50×50 μm² pixels** in **3D** (100μm thick) and **planar** (150 μm thick) technologies (25×100 μm² 3D inner barrel layer)
  - Pre-production 3D sensors in hand (67% yield)
  - Pre-production planar sensors order finalized and first sensors in hand
- ITkPixV1 pixel FE chip**: Joint ATLAS-CMS effort (RD53) using TSMC 65 nm**
  - **Radiation hard > 500 Mrad (10^{16} $n_{eq}cm^{-2}$)**
    - Single Event Effects (SEE) hardened
  - **Trigger rate: 1 MHz**
  - High hit rate: 3 GHz/cm²
  - Improved shuntLDO design for serial powering
  - Data format including compression
  - Average chip yield of 75%
- Several RD53A and first ITkPixV1 electrical modules assembled and under-test

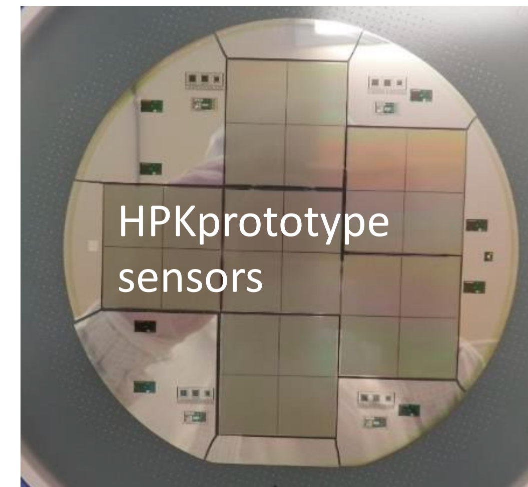


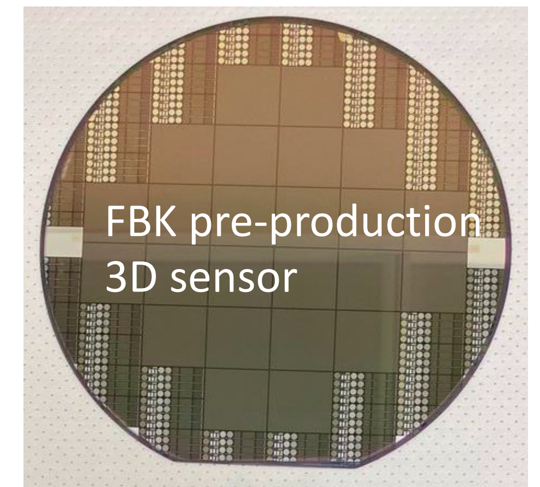
https://rd53.web.cern.ch/



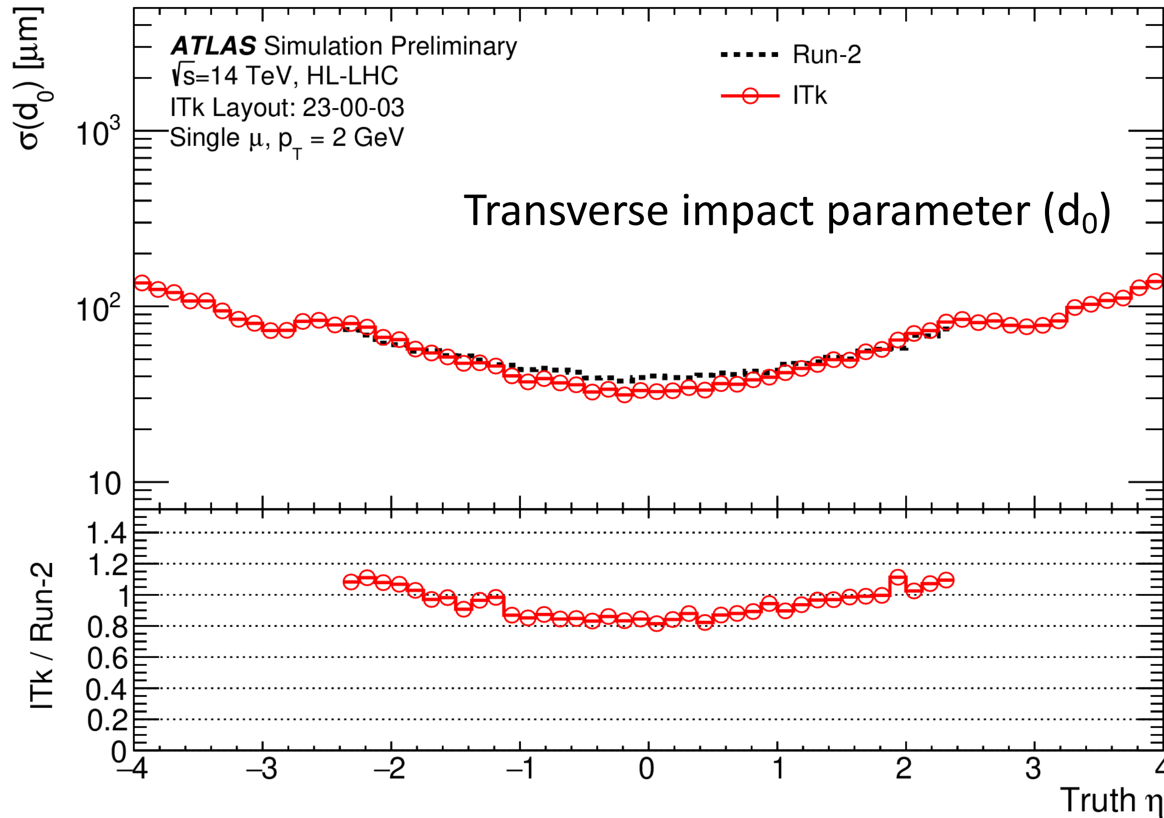


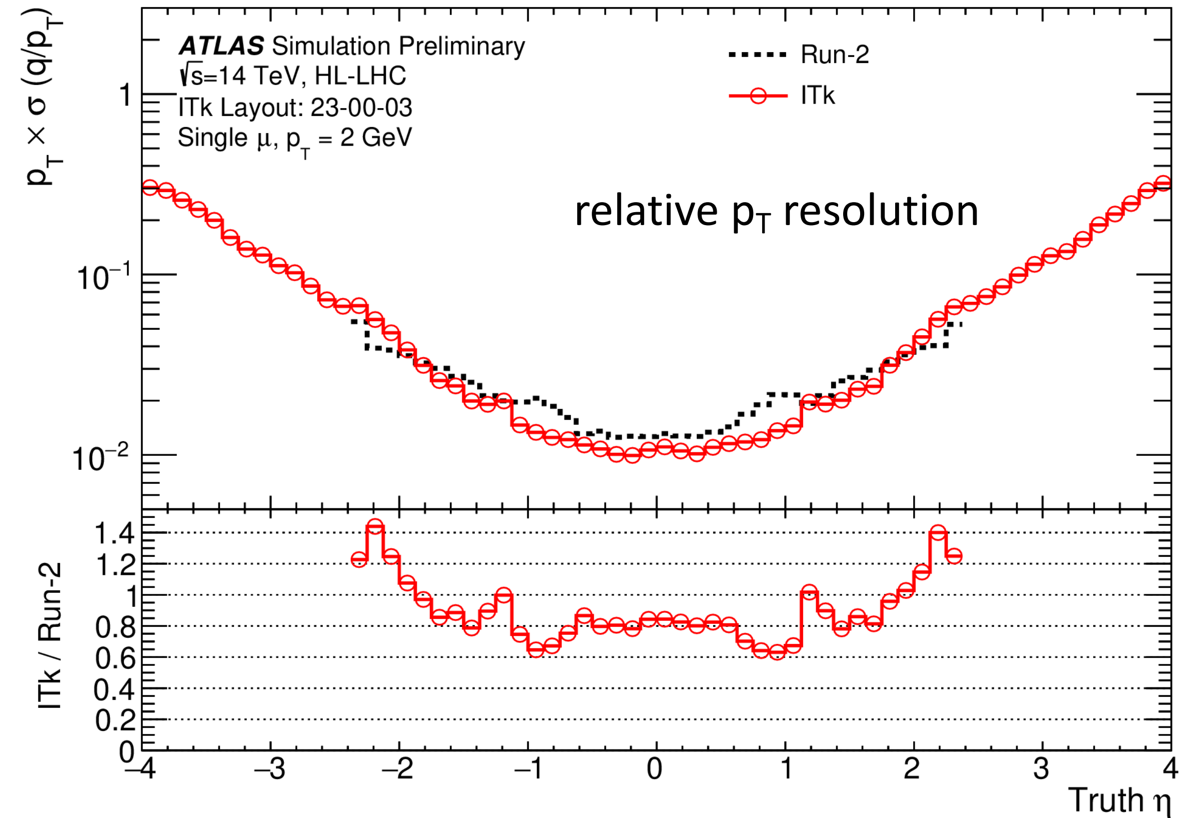






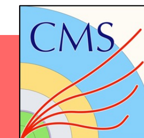
ATLAS: tracker performance



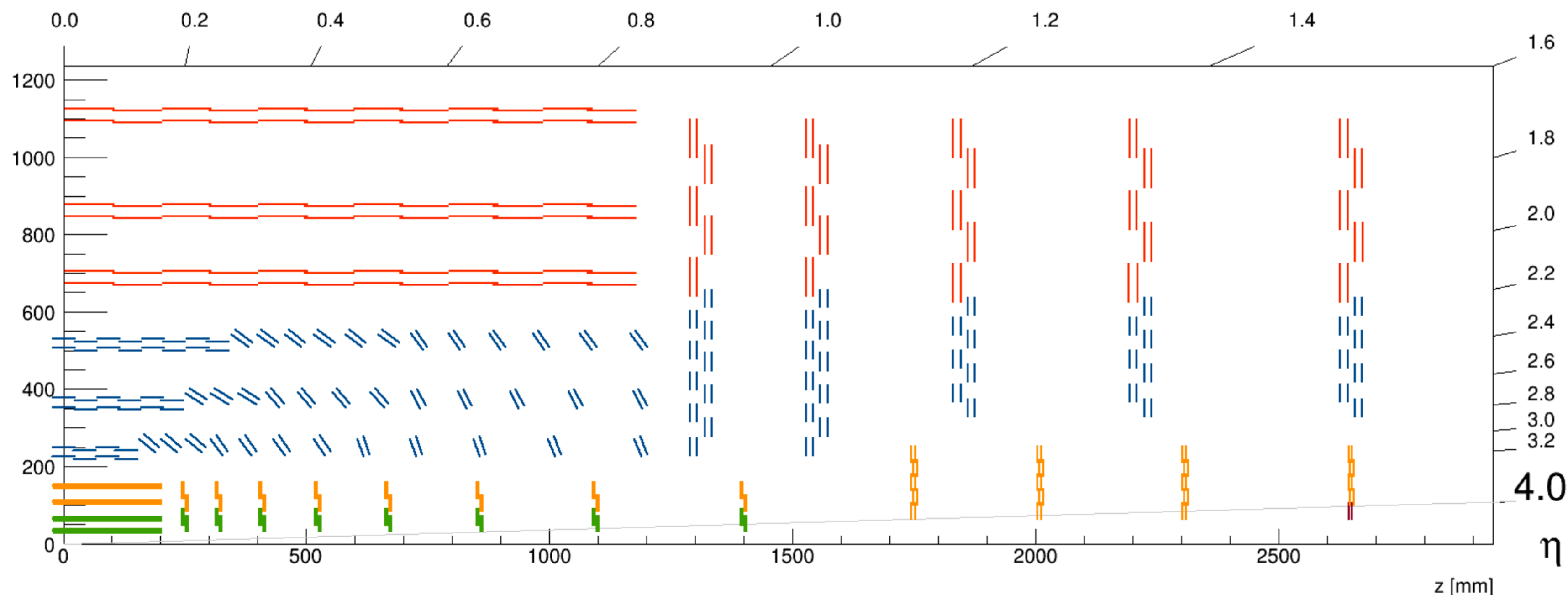


- achieve similar performance (slightly improved) in the central barrel (pile-up = 140-200) + coverage extended up to $|\eta|<4$
    - Track selection: 2 GeV muons
    - Transverse impact parameter (d_0) <100μm
    - Relative p_T resolution <10%

CMS: inner + outer tracker



Technology:
- hybrid pixels
- microstrip



- Goals: maintain/improve RUN2 tracking performance
- Change in running conditions for LHC to HL-LHC
  - Pileup increasing from 25 to ~200
  - Hit rate from 0.58 to 3.2 GHz/cm^2
- Requirements:
  - Smaller pixels to reduce occupancy
  - Lower detection threshold to allow two track separation
  - Reduced material budget
  - Increased radiation-hardness

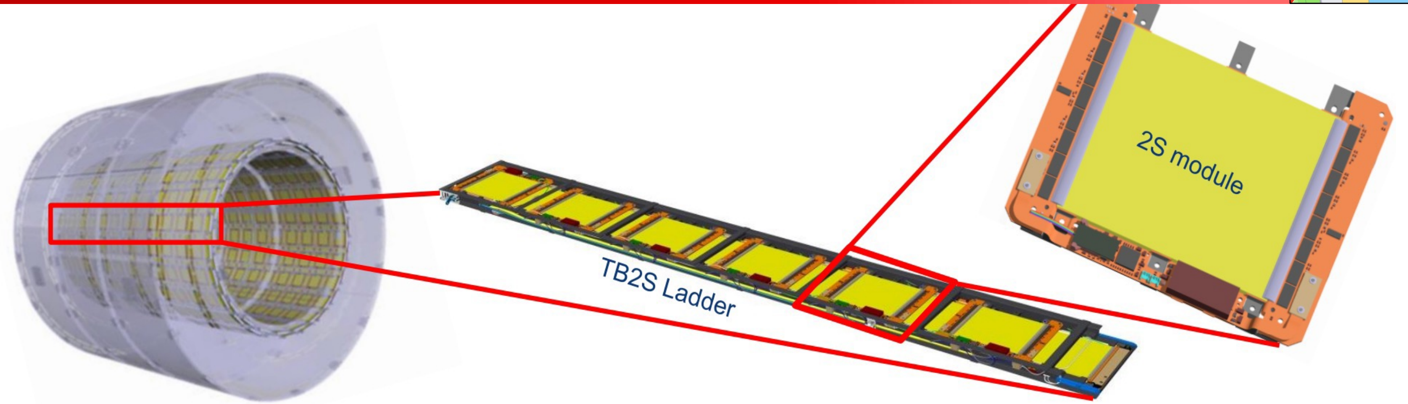
Layout:
- Inner Tracker (IT) replaces silicon pixel detector
- Outer Tracker (OT) replaces silicon strip tracker

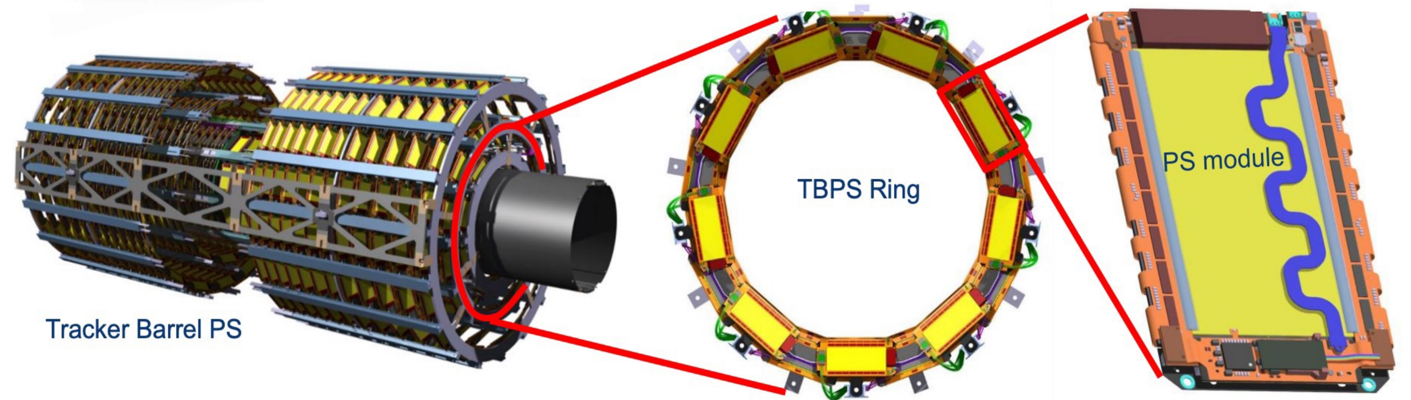
- Inner Tracker:
  - 4 barrel layers, 8 small disks, 4 large discs per side
  - Pixel size options: 50 x 50 µm^2 , 25 x 100 µm^2
  - n in p type Si sensors + 65 nm C-ROC developed in CMOS 65nm technology within the CERN RD53 project
- Outer Tracker:
  - 6 barrel layers, 5 discs per side
  - 9.5 million channels, **44M strips + 174M macropixels**

TDR: The Phase-2 Upgrade of the CMS Tracker https://cds.cern.ch/record/2272264

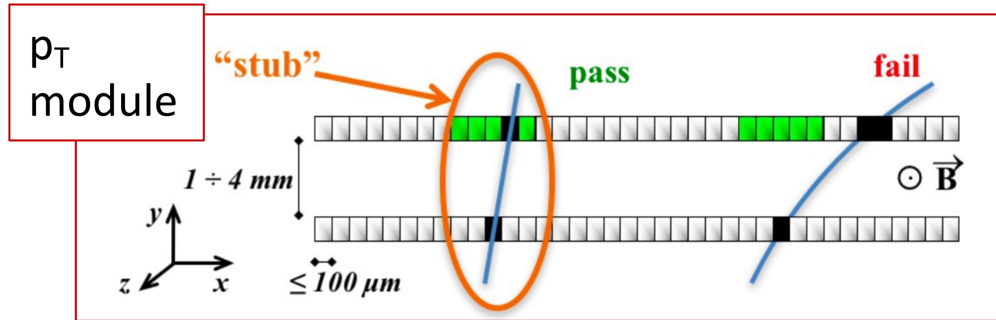
CMS: focus on outer tracker (strips+macro pixels)

- Upgraded CMS outer tracker to be segmented into three regions and **two module types**
- PS module = pixel-strip module, composed of a strip sensor and a macro-pixel sensor on top of each other
- 2S module = 2 layers of strip sensors





p_T module

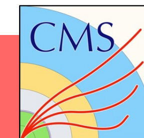


p_T module = module intrinsically capable to identify particles above a chosen p_T value.

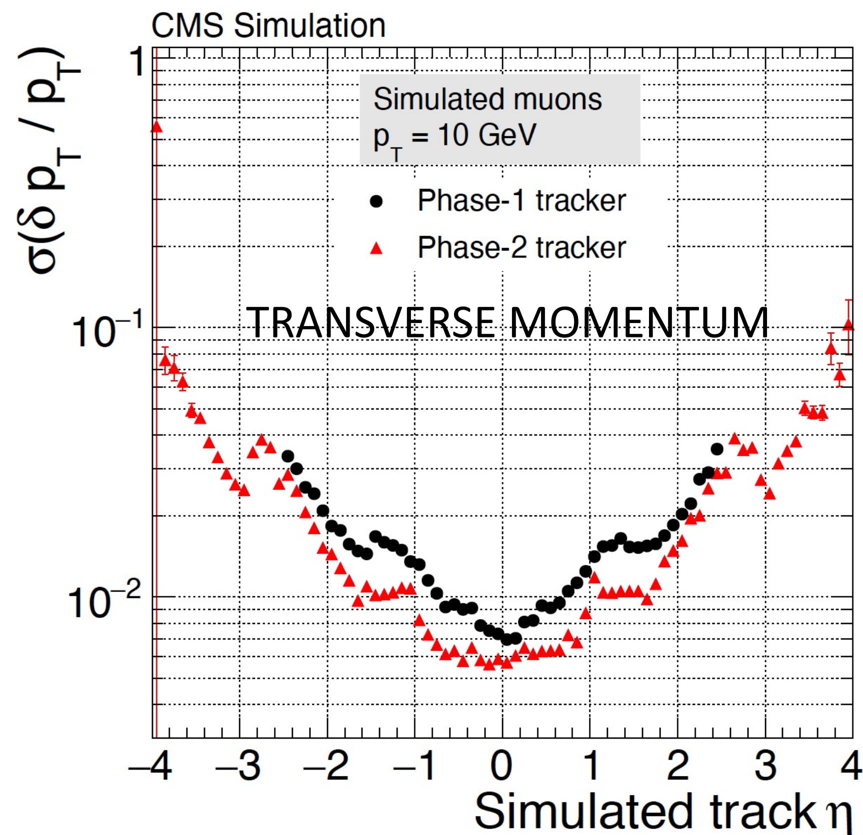
- Exploits p_T dependent bending of tracks in B
- Select tracks with p_T > 2 GeV

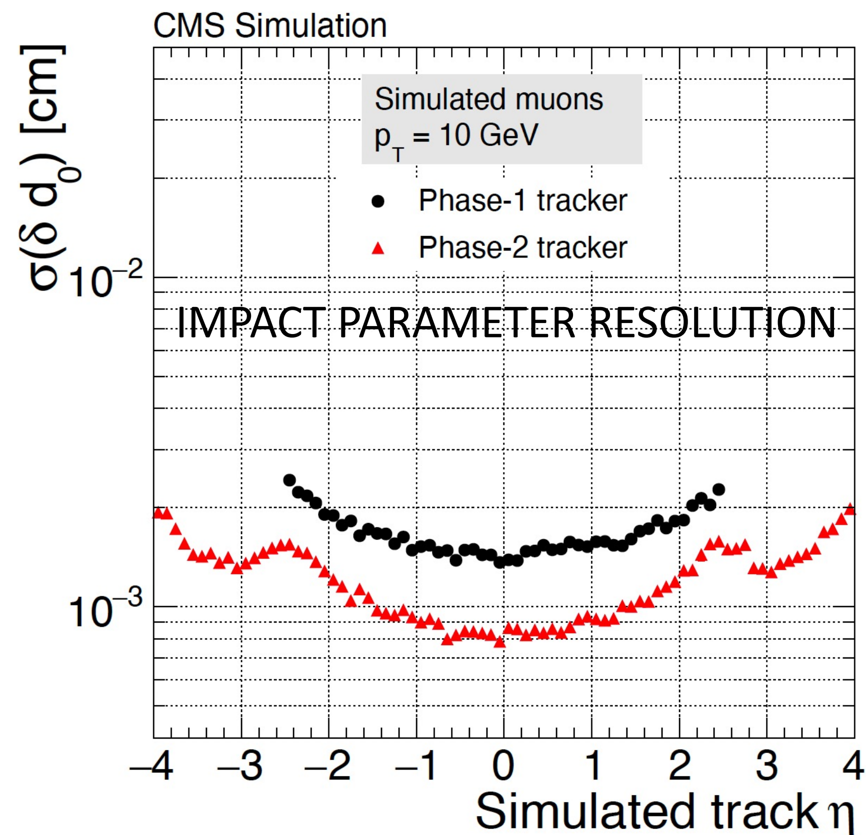
- Electrically, the basic building block is the module
  - no common service boards
- Each module is connected directly to the back-end

CMS tracker performance



track selection: single muons with p_T = 10 GeV

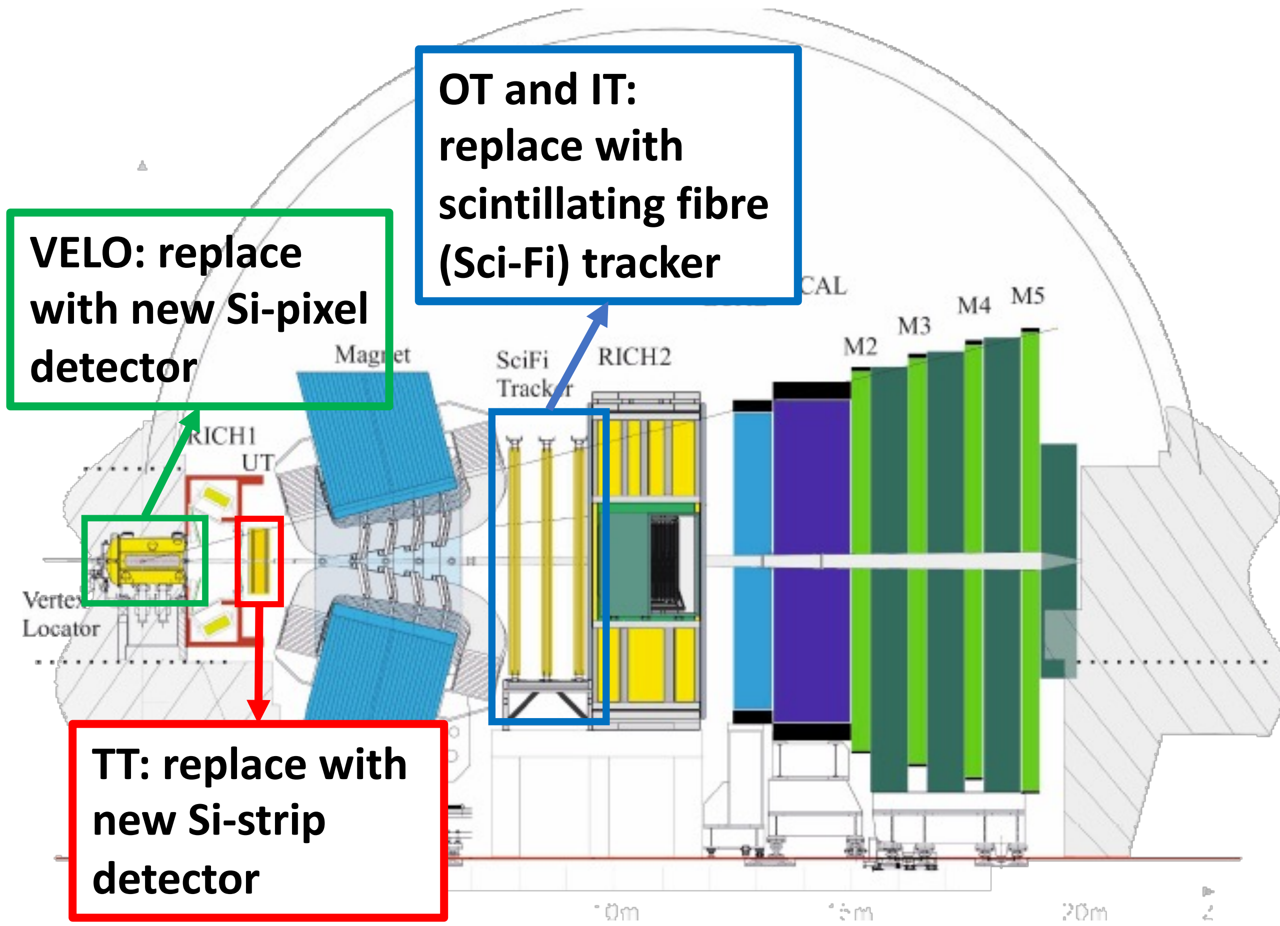




- Transverse momentum resolution significantly improved
- Transverse impact parameter resolution improved:
  - ranging from below 10 μm in the central region to about 20 μm at the edge of the acceptance

LHCb: upgrade I

- Increase in luminosity by factor 5, to = 2×10^{33} cm^{-2} s^{-1}
- Transform entire detector to 40 MHz readout



Technology:
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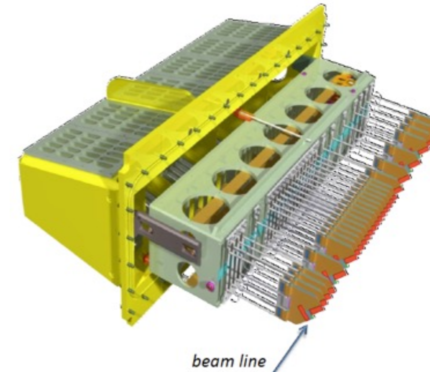
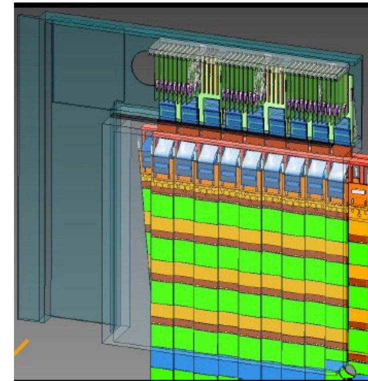
- microstrip



VELO: 52 hybrid pixel modules (more in next slides)



UT Upstream Tracker:
- Situated between VELO and dipole magnet
- 4 planes of Si microstrip detectors: ~1000 sensors
- improved performance wrt TT:
  - coverage, radiation hardness, 40 MHz readout, improved granularity, less material
- 4192 ASICs with 128 channels each:
  - 130 nm-TSMC with 30 MRad radiation tolerance

LHCb Tracker Upgrade Technical Design Report https://cds.cern.ch/record/1647400
LHCb VELO Upgrade Technical Design Report https://cds.cern.ch/record/1624070

LHCb upgrade I: focus on VELO

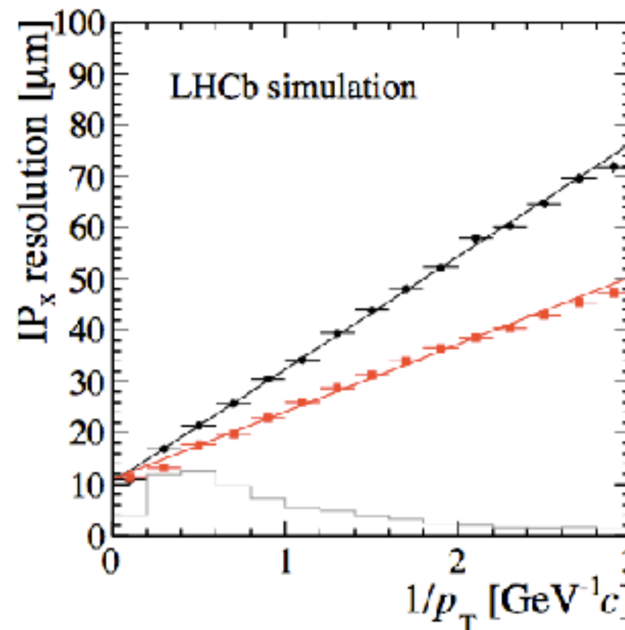
- GOAL: improve impact parameter resolution
- Challenges:
  - Vertex detector surrounding collision region
    - In vacuum
    - Close to the beam: 5.1 mm
  - Radiation Hardness:
    - 8 x 10^{15} n_{eq}/cm^2
    - non-uniform ~ $r^{-2.1}$
  - Readout: triggerless at 40MHz
  - Data rates: up to 20 Gbit/s for central ASICs (~ 3 Tbit/s in total)
- TECHNOLOGY CHOICE: HYBRID PIXELS

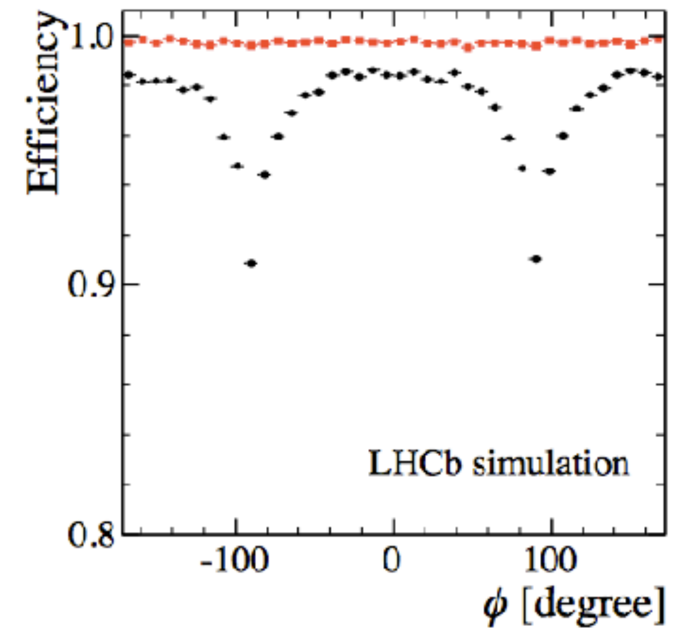
Hybrid Pixels instead of **strips:** better performance for impact parameter resolution and efficiency (red dots)

VELO installation just COMPLETED

rows of silicon microstrip modules

rows of silicon hybrid pixel modules





LHCb: VELO Upgrade layout

LAYOUT:

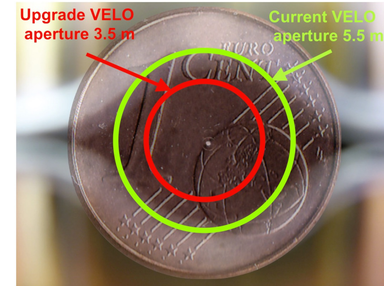
- Four hybrid pixel sensors (active area 0.12 m^2) per double sided module.
- Sensor:
  - p-type, 8.10^{15} 1 MeV n_{eq}/cm^2 lifetime fluence
  - area 43 x 15 mm
  - **768.256 pixels, each 55.55 µm²**
- VeloPix ASICs:
  - Derived from Timepix3 **(TSMC 130 nm CMOS)**
  - 624 ASICs, ~**41 Mpixels** thinned to 200 µm
  - Trigger-less, data driven readout (~2.9 Tbits/s)
  - **Radiation hardness to 400 MRad**
    - SEU/SEL tolerance

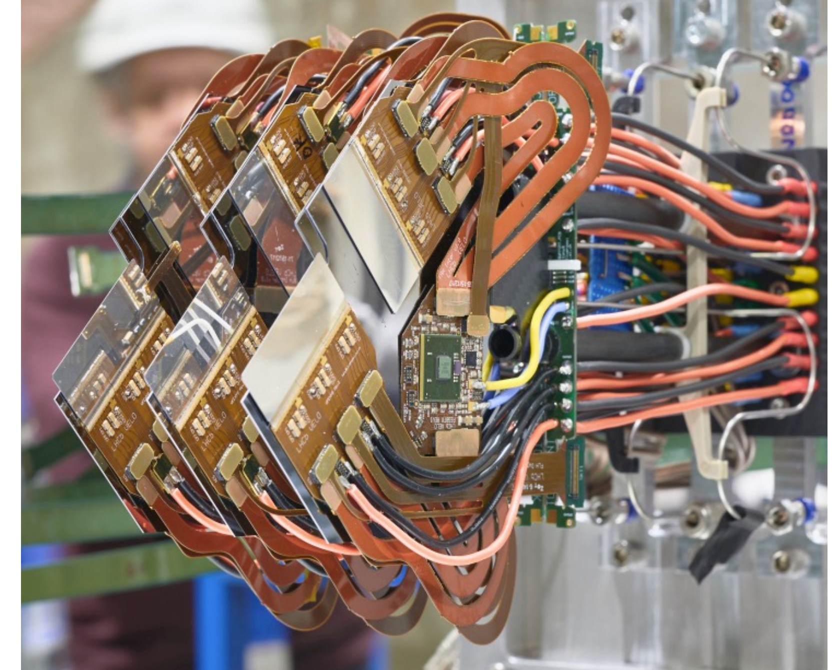
Cooling:

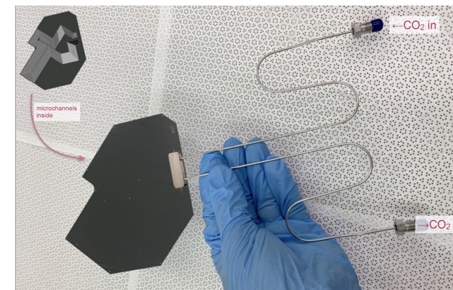
- Solution provided evaporative CO2 in 120 µm x 200 µm channels in silicon substrate. Total thickness: 500 µm

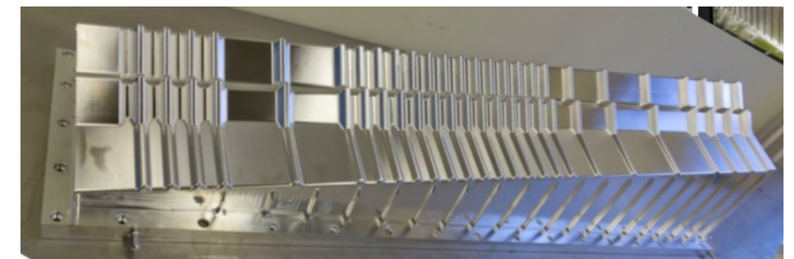
Foil:

- The VELO is separated from the primary vacuum by the 1.1 m long thin walled “RF foil”
- final thickness of 250 µm
- at just 3.5 mm from the beam and 900 µm from the sensors



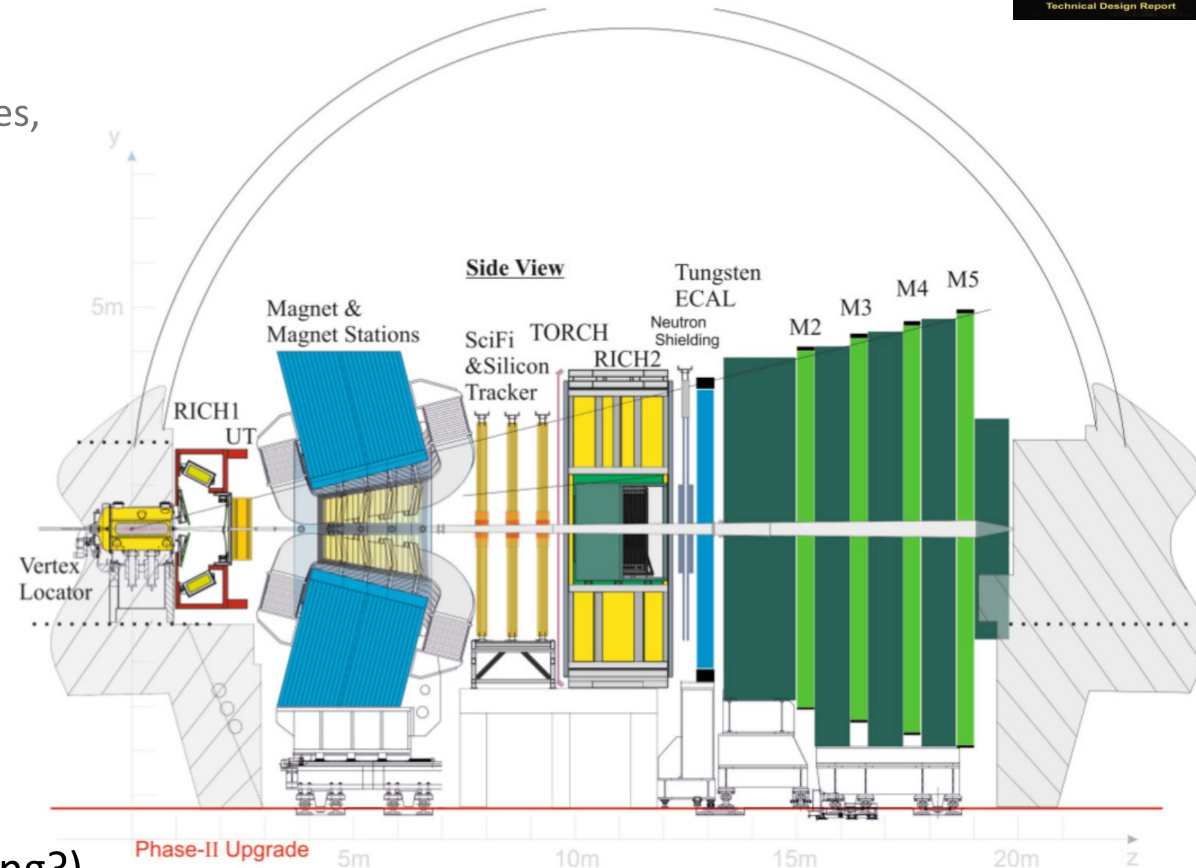






LHCb upgrade II

- Likely machine parameters for Phase II upgrade:
  - Pileup ~ 42, L_{max}=1.5 x 10^{34} cm^{-2} s^{-1}
- Goal: same quality performance as Upgrade I with
  - 10 x higher particle multiplicity, radiation damage, data-out rates, denser primary vertex environment
- New detectors:
  - new VELO (precision timing)
  - new Upstream Tracker (timing)
  - Mighty Tracker (SciFi + silicon)
  - Magnet stations (possibly) → p_T below 5 GeV/*c*
- Move towards **4D tracker concept with addition of timing**:
  - Timing information will contribute to Pattern Recognition
  - Track time stamping for PV association, PV timing
- Sensor: R&D thin planar, LGAD, 3D concepts, MAPS (with timing?)
- ASIC: 28nm, based on Timepix4, 20-50 ps time resolution



TDR https://cds.cern.ch/record/2776420

ALICE2 UPGRADE: ITS + MFT

Inner Tracking System

GOALS:

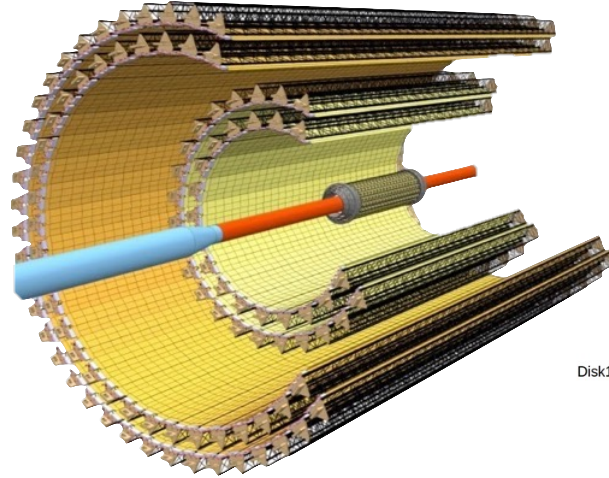
- improve pointing resolution
  - reduced material
  - closer to IP (39mm -> 22mm)
  - better spatial resolution (-> 5x5μm^2)
- faster readout (1->100kHz)

Detector layout

- Inner Barrel: 3 layers, 48 staves
- Outer Barrel: 4 layers, 144 staves

In total ~24000 chips = 12.5 Gpixels

~10m^2 of silicon pixel sensors

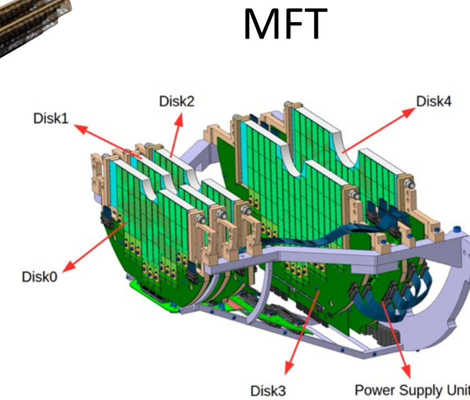


ITS

Technology:

- CMOS sensors (ALPIDE)

MFT



ITS Inner and outer barrels + MFT disk 0 during installation

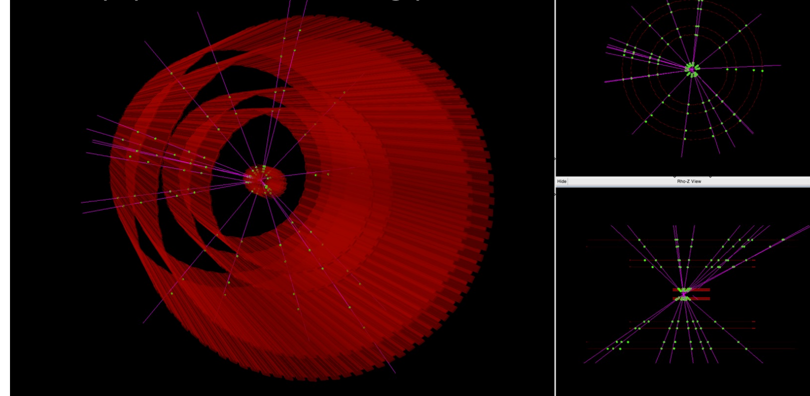
Muon Forward Tracker

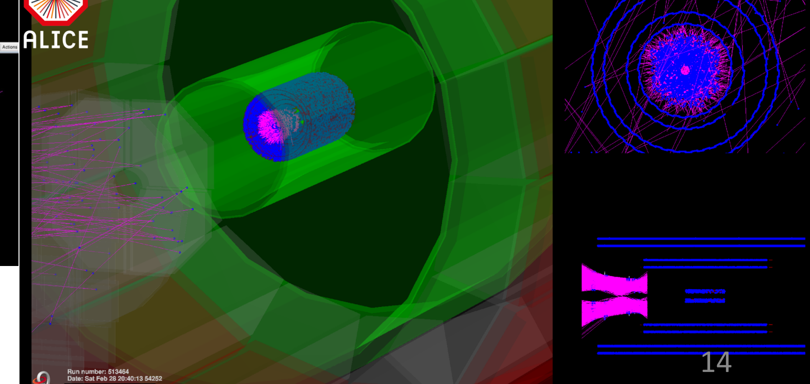
GOALS:

- add capabilities for secondary vertex measurement at forward rapidity

Detector layout

- upstream of the absorber
- 10 half-disks, 2 detection planes each
- 280 ladders of 25 sensors each: 920 chips (0.4 m^2)



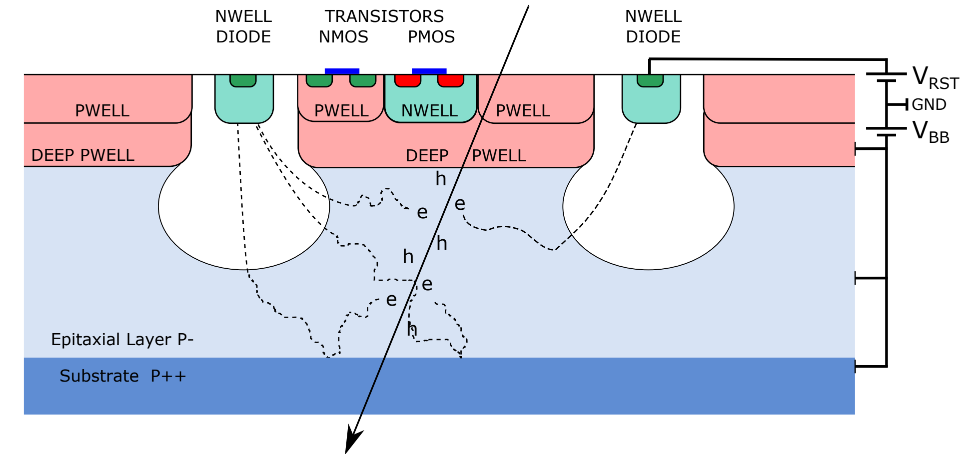


ITS TDR: J. Phys. G: Nucl. Part. Phys. 41 (2014) 087002
MFT: CERN-LHCC-2015-001. ALICE-TDR-018 https://cds.cern.ch/record/1981898

ALPIDE: CMOS monolithic active pixel sensor

CMOS Pixel Sensor – Tower Semiconductor 180nm CMOS Imaging Sensor (CIS) Process

- Deep PWELL shields NWELL of PMOS transistors (full CMOS circuitry within pixel active area)
- R&D effort within the ALICE collaboration
  - excellent collaboration with foundry
  - more than 70k produced and tested (for ALICE and other applications)
  - ALICE ITS pioneers large area trackers built of MAPS (see ALICE 3)
- in parallel studies to optimise process to reach full depletion and improve time response and radiation hardness up to 10^{15} 1MeV/n_{eq} :
  - **More details:** NIM **A871** (2017) https://doi.org/10.1016/j.nima.2017.07.046
  - **Now being further pursued: MALTA, CLICpix, FastPix, …**



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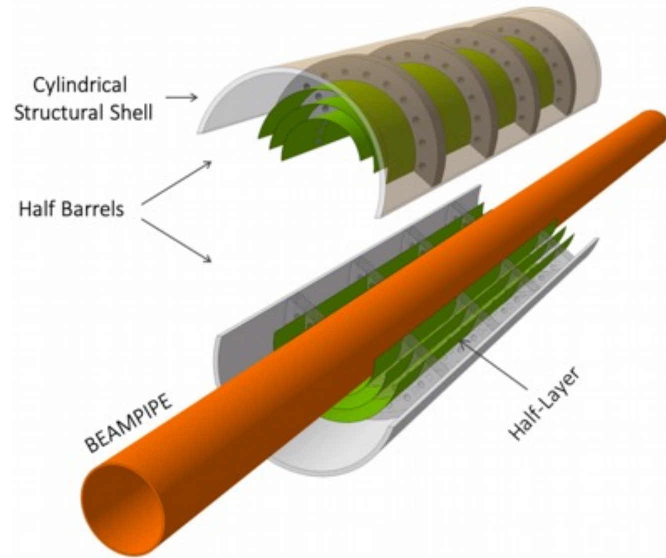
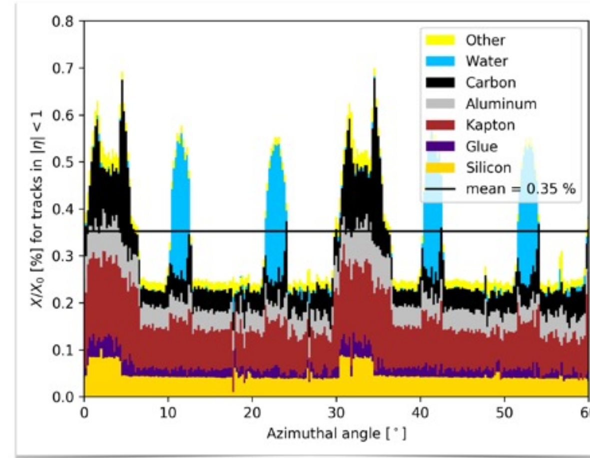
ALPIDE Key Features

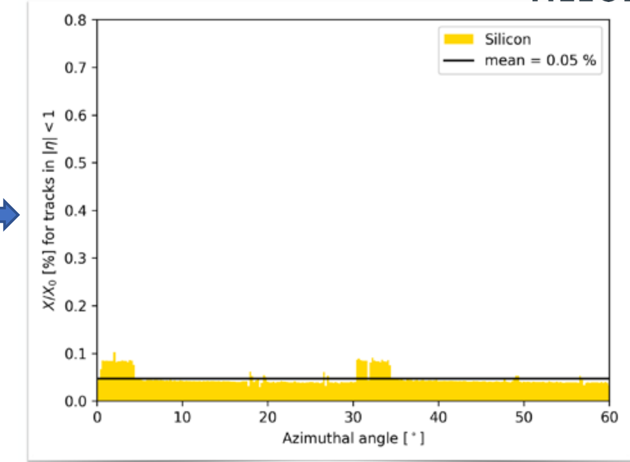
- In-pixel: Amplification, Discrimination, multi event buffer
- In-matrix zero suppression: priority encoding
- Ultra-low power < 40mW/cm^2 (< 140mW full chip)
- Detection efficiency > 99%
- Spatial resolution ~5μm
- Low fake-hit rate: << 10^{-6}/pixel/event (10^{-8}/pixel/event measured during commissioning)
- Radiation tolerance:
  - 270 krad total ionising dose (TID),
  - > 1.7 10^{13} 1MeV/n_{eq} non-ionising energy loss (NIEL)

ALICE 2.1: ITS3 all silicon detector



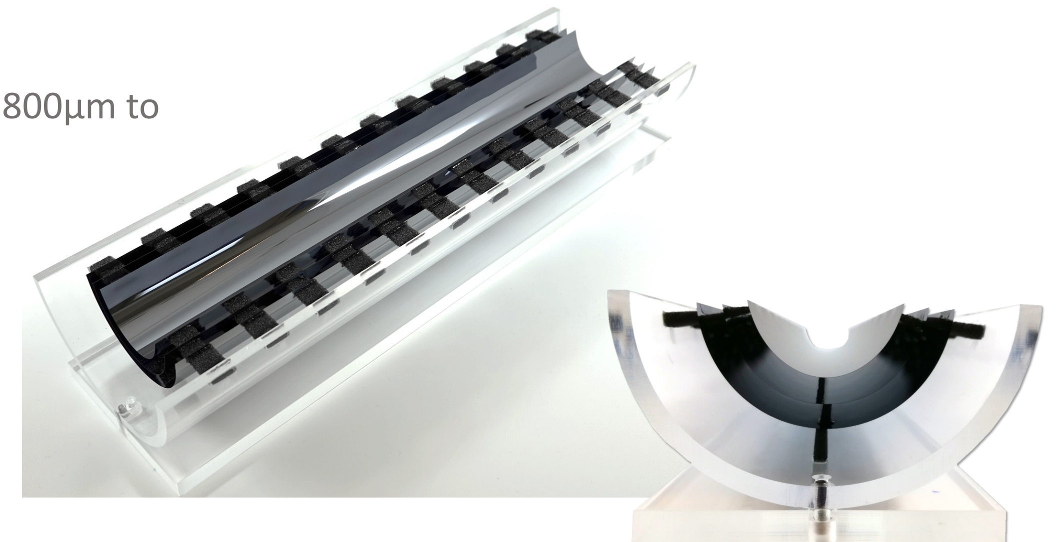


ITS2 Layer 0: X/X0=0.35



ITS3 only silicon: X/X0=0.05

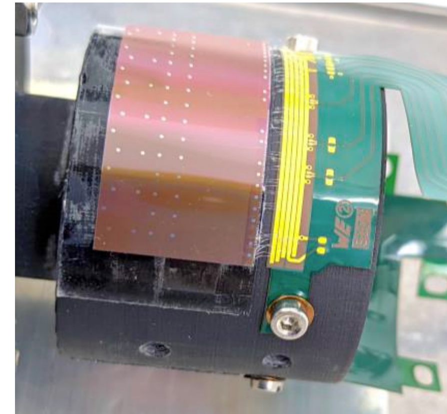
- Goal: improve vertexing at high rate
- Layout: 3 layers, replace ITS Inner Barrel,
  - beam pipe: smaller inner radius (18.2 mm to 16 mm) and reduced thickness (800µm to 500µm)
  - innermost layer: mounted around the beam pipe, radius 18mm (was 23mm)
- Technology choices:
  - 65 nm CIS of Tower & Partners Semiconductor (TPSCo):
    - larger wafers: 300 mm instead of 200 mm,
    - single “chip” equips an ITS3 half-layer (through stitching technology)
    - 6 sensors in total
  - thinned down to 20-40µm
    - -> flexible
    - bent to target radii
  - mechanically held by carbon foam ribs with low density and high thermal conductivity

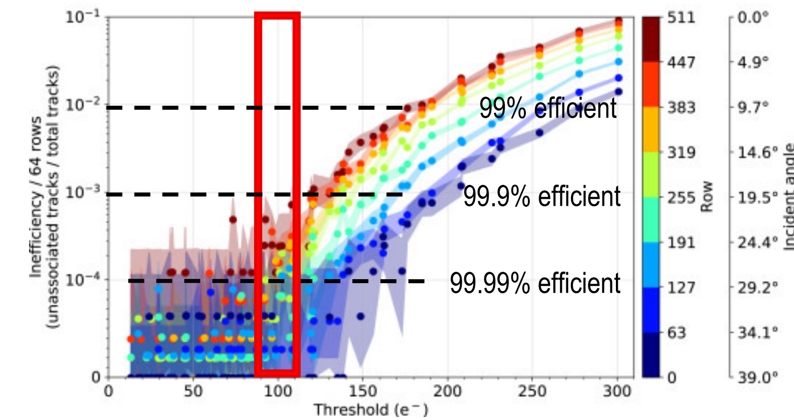


Letter of Intent for an ALICE ITS Upgrade in LS3 https://cds.cern.ch/record/2703140

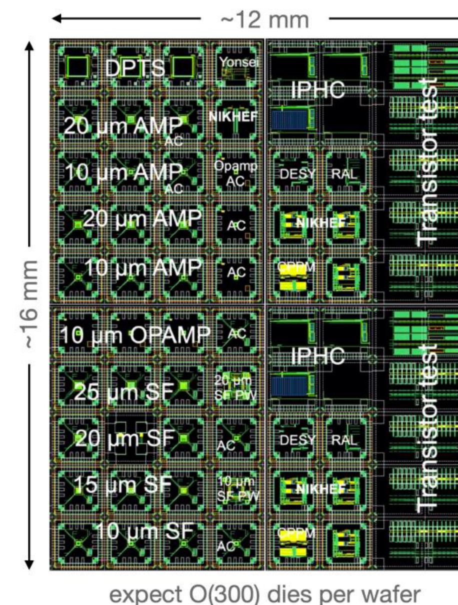
ALICE 2.1: ITS3 R&D first results

- **Bending: tests on bent ALPIDE**
  - > 99.9% efficiency at threshold of 100 e^- (nominal operating point of ALPIDE)
  - Proving that bent MAPS are operable and perform well
  - 1st paper published: https://doi.org/10.1016/j.nima.2021.166280

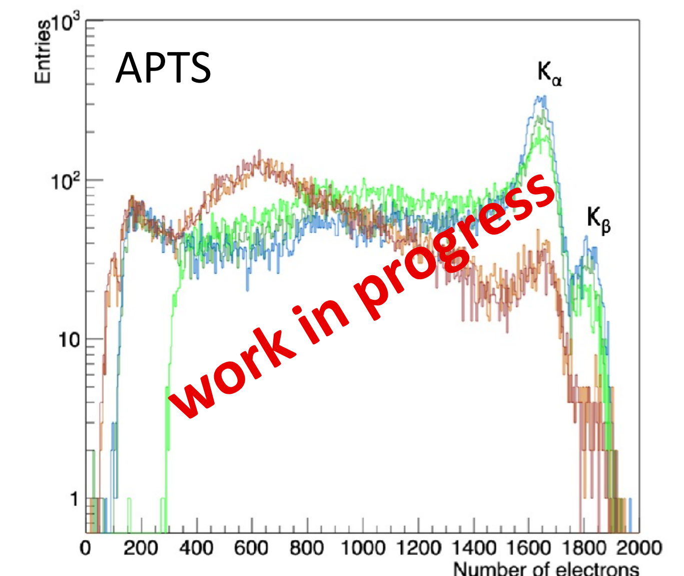




- **Technology: First chip submission in 65 nm TPSCo process**
  - First design and submission of 65 nm technology, MLR1, in collaboration with CERN EP R&D:
    - transistor test structures, DACs, analog pixel matrices, digital pixel matrices, …)
  - First wafers were received in summer 2021
    - Laboratory characterisation and yest-beam campaigns started and ongoing
    - Many Institutes and groups involved
  - first results on DPTS (preliminary):
    - Efficiency: >99%
    - Time resolution: O(10ns)
    - Radiation hardness: OK for ALICE
    - Spatial resolution: O(3-4 µm)



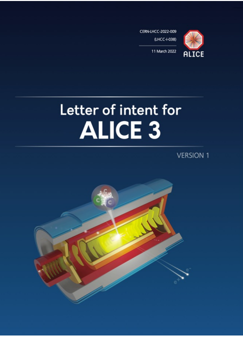
expect O(300) dies per wafer

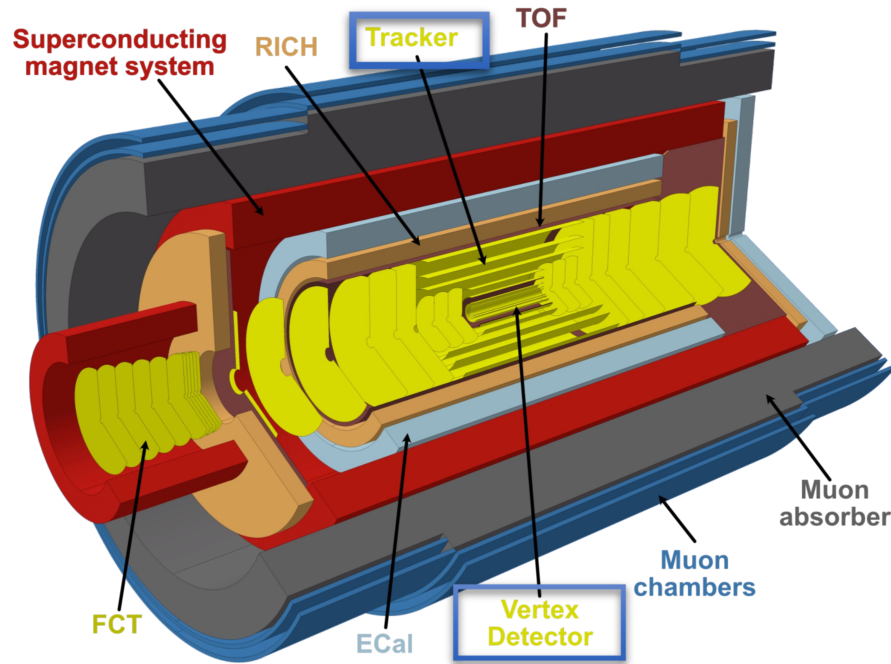


process optimisation:
charge collection/sharing

- **Stitching: ER1 submission in summer 2022**
  - Stitched prototypes to develop stitching know-how
  - Focus on power distribution, signal routing, yield

ALICE 3: tracker + vertex detector





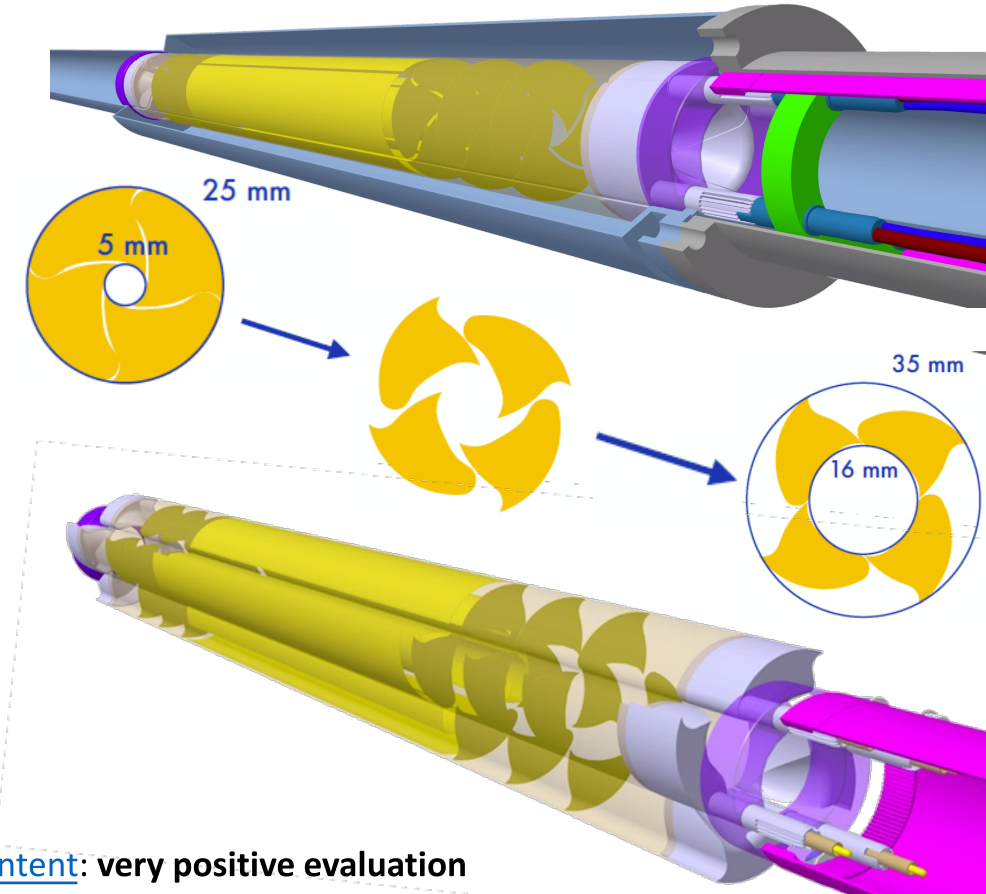
- **Conceptual study of iris tracker**
  - wafer-sized, bent MAPS (leveraging on ITS3 activities)
  - rotary petals (thin Be walls) for secondary vacuum
  - match beampipe parameters (impedance, aperture, …)
  - feed-throughs for power, cooling, data
- **R&D programme** on mechanics, cooling, radiation tolerance

GOALS:

- Tracking and PID over large acceptance
- Excellent vertexing
- Continuous readout

REQUIREMENTS

- **Tracker:** low power, large surface **60 m²** (challenges: yield, fill factor)
  - Monolithic CMOS sensors with timing (4D tracking)
- **Vertex detector:** very close to IP (challenges: high rate, high radiation load)
  - Retractable detector (iris tracker) $R_{in} \approx 5$ mm
  - Wafer-scale monolithic CMOS sensors



[CERN-LHCC-2022-009] LHCC review of Letter of Intent: **very positive evaluation**

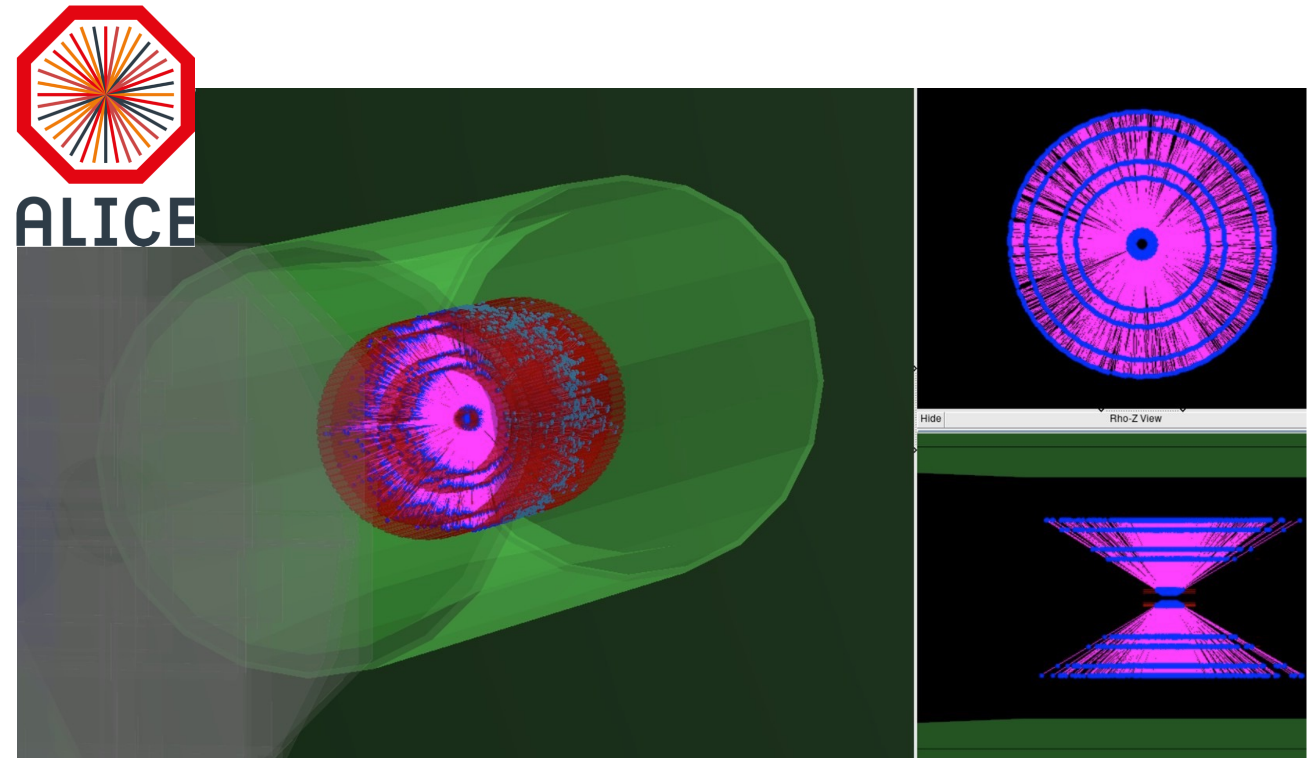
Conclusions

Present achievements:

- Amazing progress in hybrid technologies:
  - Rad Hard sensors and ASICS (up to >500Mrad)
  - fast readout (up to 1MHz)
- CMOS pixel detectors used to build a full tracking system
  - low material budget (down to 0.1% X0)
  - reasonable cost for large areas
- Massive R&D campaigns for all components
- Synergies among experiments

Future goals:

- Wafer scale, rad hard, fast response MAPS
- timing information in hybrid and MAPS to build 4D trackers



Event display of a PbPb collision (emulated in ALICE ITS)

BACK UP SLIDES

HL-LHC Upgrade schedule

LHC | HL-LHC

Run 1 | Run 2 | Run 3 | Run 4 - 5...

LS1 | EYETS | LS2 | EYETS | LS3

7 TeV | 8 TeV | 13 TeV | 13.6 TeV | 13.6 - 14 TeV | energy

splice consolidation
button collimators
R2E project

cryolimit
interaction
regions

Diodes Consolidation
LIU Installation
Civil Eng. P1-P5

pilot beam

inner triplet
radiation limit

HL-LHC
installation

2011 | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 | 2026 | 2027 | 2028 | 2029 | 2040

experiment
beam pipes

ATLAS - CMS
upgrade *phase 1*

ALICE - LHCb
upgrade

ATLAS - CMS
HL upgrade

75% nominal Lumi | nominal Lumi | 2 x nominal Lumi | 2 x nominal Lumi | 5 to 7.5 x nominal Lumi

30 fb^{-1} | 190 fb^{-1} | 450 fb^{-1} | integrated luminosity 3000 fb^{-1} 4000 fb^{-1}

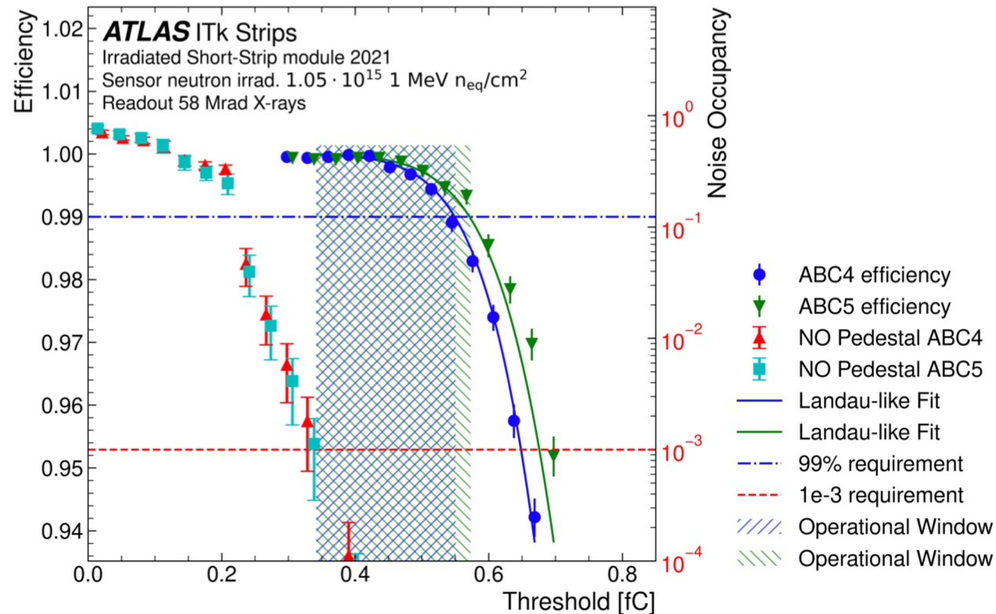
- Peak luminosity: 5-7.5 x 10^{34} cm^{-2}s^{-1} → ~× 5-7
- Average pile-up (PU): up to ~200 → ~× 5
- Integrated luminosity: 4000 fb^{-1} → ~× 10

- Particle multiplicity
  - About 10 times more track density
  - Needs better tracking granularity
- Radiation damage
  - Radiation dose becomes critical closer to the beam line
  - Total Ionizing Dose (TID) up to 1 Grad
  - Particle fluence up to 2 x 10^{16} n_{eq}cm^{-2} in the vertex region (x 20)

ATLAS: strip sensors and chips

STRIPS - 8 sensor geometries:

- 2 for the barrel, 6 for the end-caps
- 320 µm thick n-in-p silicon
- 75.5 µm strip pitch barrel
- From 70 to 80 µm pitch in the petals
- Bias voltage: -100 V to -500 V



Three chips all made in 130 nm technology

- ABCStar (Front End (FE) chip)
  - Binary readout: 256 channels
  - High yield in pre-production, 92%, some concerns on SRAM corners tests
- HCCStar (FE Interface Chip)
  - Controller chip on hybrid
  - Interface between ABCStar chips and off-detector
- AMACStar (Power control and environment monitoring)
  - Monitoring and control chip on Powerboard

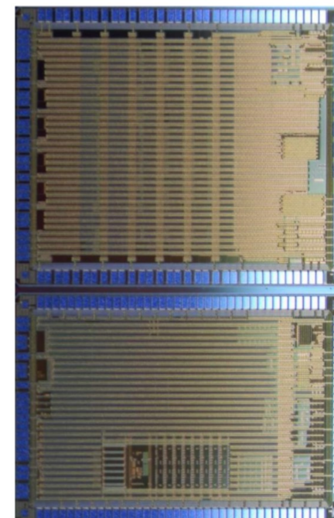
Production order placed: first wafers delivered

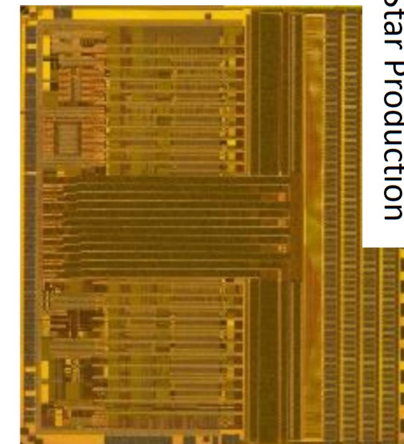
pre-production available

All three chips were extensively modified to improve SEE protection

- Tested in heavy-ions and protons with excellent performance
- Pre-production ABCStar with triplication enabled had no measured Single Event Upset (SEU)

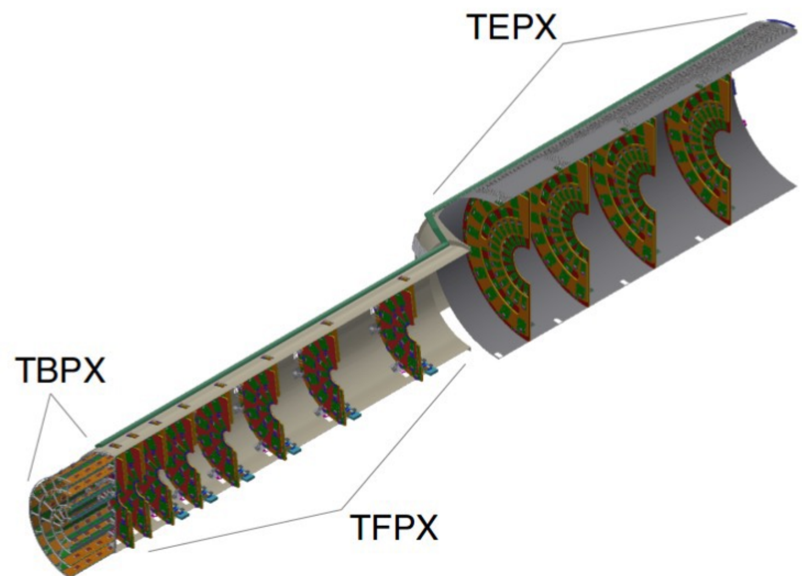
HCCStar + AMACStar Pre-Production

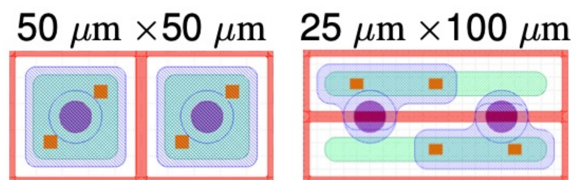




ABCStar Production

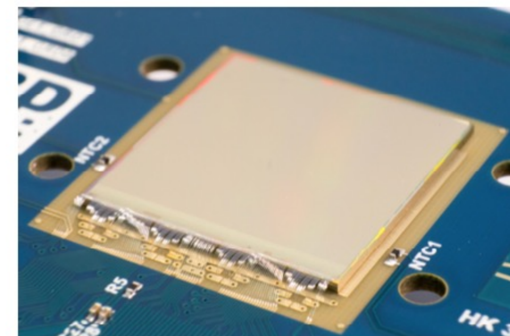
CMS: inner tracker (pixels)





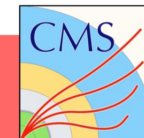
- Increased granularity (x6 smaller pixels, 2500 μm^2)
  - Hybrid technology. Total active surface of ~4.9 m^2 - 3892 modules - 2G pixels
- Increased detection coverage ($|\eta| \leq 4$)
- Reduced material budget (CF mechanics, serial powering, CO2)
- Lower detection threshold (new readout chip)
- Simple installation and removal

- n in p type Si sensors of 150 μm thickness
  - segmented into pixel sizes of 25 x 100 μm^2 or 50 x 50 μm^2 for better resolution
  - 1 x 2 modules (with 2 chips) in inner 2 layers and inner 2 rings.
  - 2 x 2 modules (with 4 chips) in outer 2 layers and outer 2 and 3 rings
- 65 nm C-ROC developed in CMOS 65nm technology within the CERN RD53 project

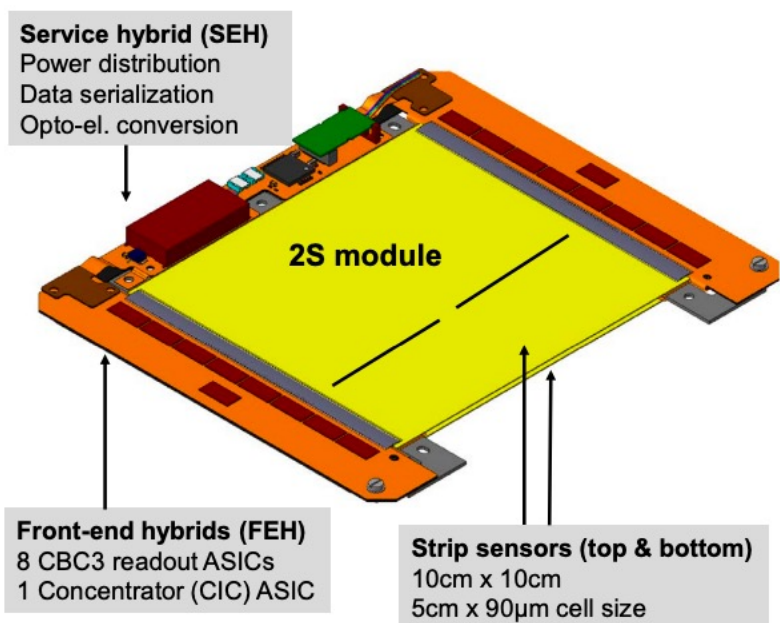


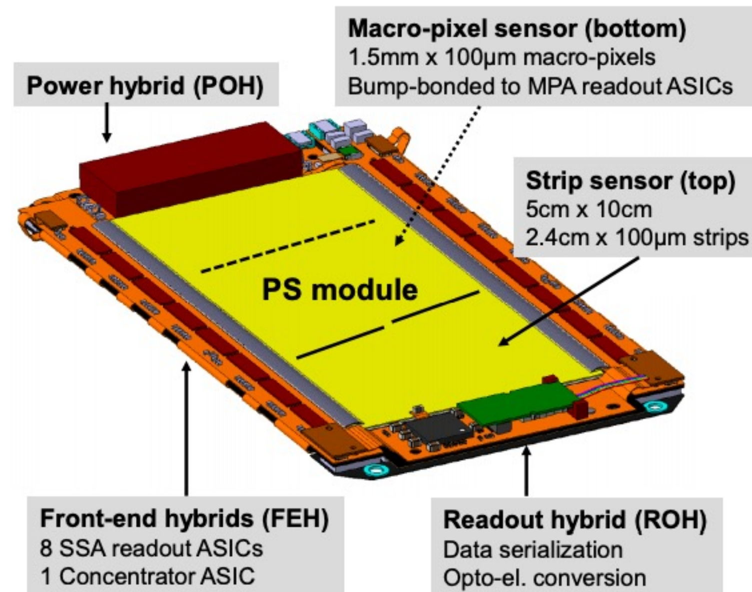
RD53B on single-chip test card

CMS outer tracker: 2S & PS modules



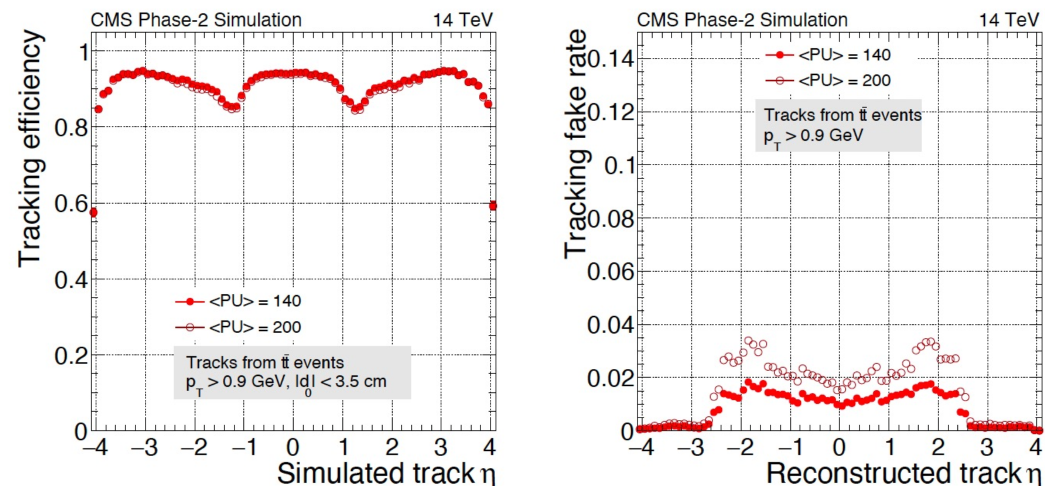
- Electrically, the basic building block is the module
  - no common service boards
- Each 2S module contain
  - Front-end hybrids (FEH): readout and concentrator ASICs
  - Service hybrids (SEH): power and opt. comm.
  - AlCF-bridges: high thermal conductivity and similar CTE as silicon
  - HV isolation and HV connection
- Each PS module contain
  - Front-end hybrids (FEH): readout and concentrator ASICs
  - Power Hybrid (POH): power connections
  - Readout hybrid (ROH): data serialisation + Opto-el. conversion
- Each module is connected with 3 wires and 2 fibers directly to the back-end





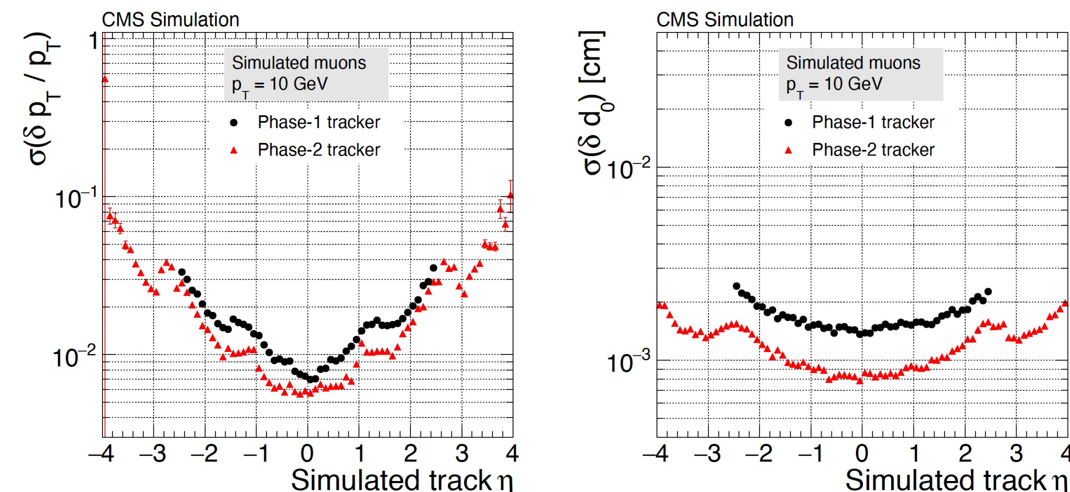
CMS Tracker performance

TRACKING EFFICIENCY AND FAKE RATE



- The tracking efficiency is around 90% in the central region, dropping off at $|\eta| > 3.8$
- Fake rate is < 2% in the entire range of η for 140 pileup events (< 3% for PU=200).
- track selection: p_T>0.9 GeV/c, $|d_0|$<3.5 cm

TRANSVERSE MOMENTUM AND IMPACT PARAMETER RESOLUTION



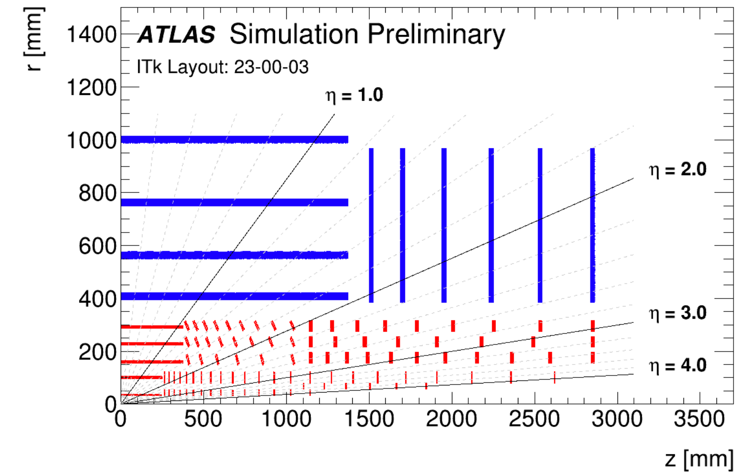
Better hit resolution of the Phase-2 tracker and the reduction of the material budget results in:

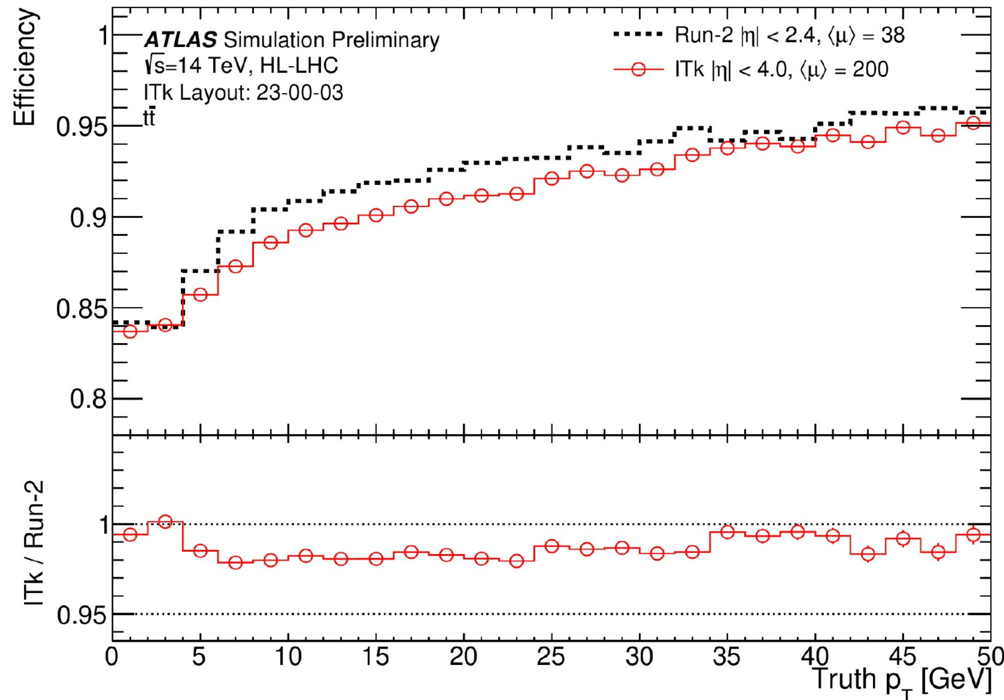
- Transverse momentum resolution significantly improved
- transverse impact parameter resolution improved: ranging from below 10 μm in the central region to about 20 μm at the edge of the acceptance
- track selection: single muons with p_T = 10 GeV

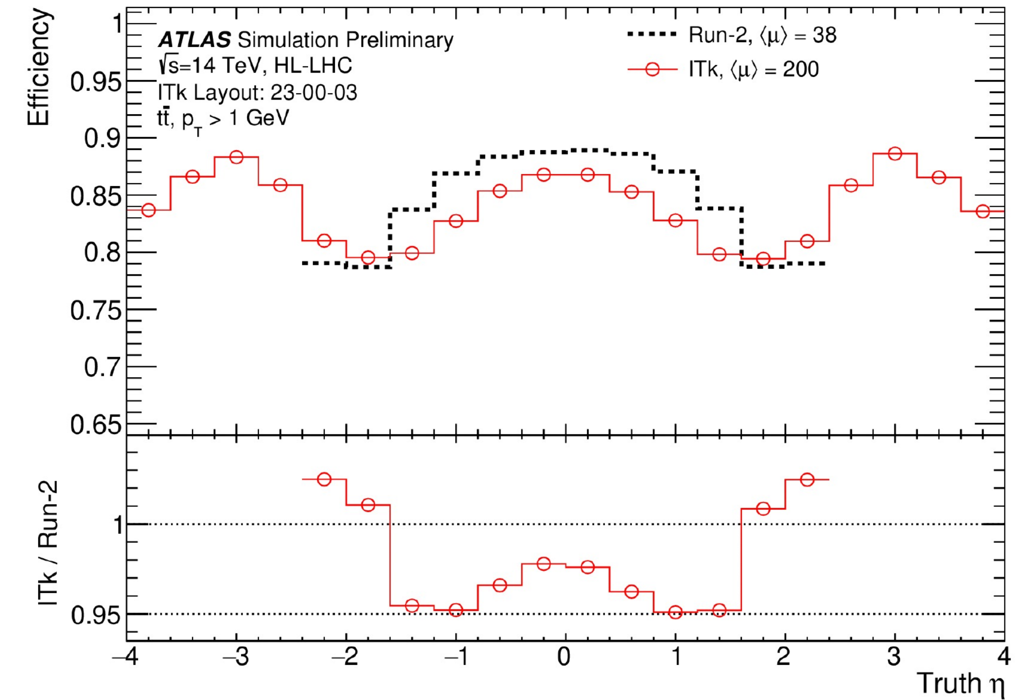
ATLAS ITk tracking performance

Tracking efficiency at 200 pileup (5x compared to Run-2)

- Similar performance to Run-2 in the barrel
- Improved efficiency (over 85%) at high-η
- Improved fake rate even considering the increased in pile-up





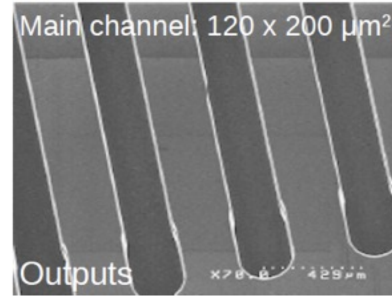


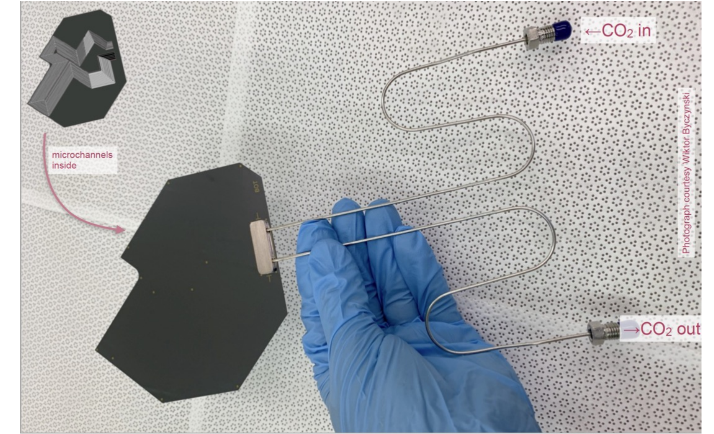
ATL-PHYS-PUB-2021-024

LHCb: VELO Upgrade cooling and ASICs

Cooling:

- Solution provided by the novel technique of evaporative CO2 circulating in 120 µm x 200 µm channels within a silicon substrate. Total thickness: 500 µm
  - High thermal efficiency
  - CTE match to silicon components
  - Minimum and uniform material
  - radiation hard





Foil:

- The VELO is separated from the primary vacuum by the 1.1 m long thin walled "RF foil"
- At just 3.5 mm from the beam and 900 µm from the sensors
- The final foil
  - withstands 10 mbar pressure variations,
  - leak tight
  - final thickness of 250 µm
  -