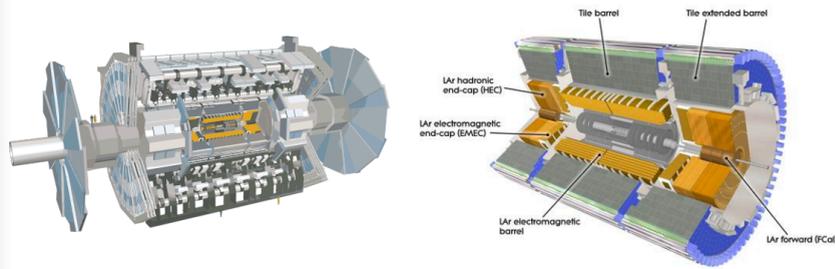


Maeyer J. Shroff

on behalf of the ATLAS Liquid Argon Calorimeter Group

ATLAS and the LAr Calorimeter...



- ATLAS is a general-purpose detector used to study particles produced by high-energy proton-proton collisions at the LHC.
- Consists of a sampling calorimeter with liquid argon as the sampling medium. Made up of 182,468 channels.
- Signal is amplified, shaped and digitized at 40 MHz.

... and the HL-LHC

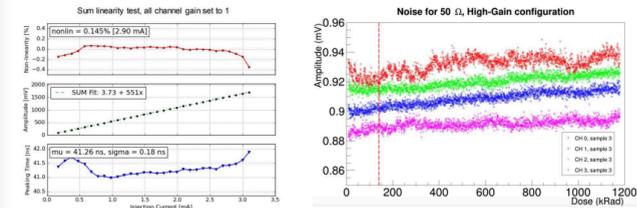
- The LHC is scheduled to undergo an upgrade during LS3 in 2026-2028 \Rightarrow **HL-LHC**.
- Instantaneous luminosity up to $5 - 7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ (5 to 7 x nominal) with pileup up to $\langle \mu \rangle \approx 140 - 200$
- To differentiate signal from noise, higher granularity shower information needs to be sent to the trigger.
- ATLAS TDAQ system will evolve to a trigger rate of 1 MHz, increasing the latency time for the LAr Calorimeter
- High radiation dose to front-end electronics is expected, exceeding current electronics limits.
- As a result, the LAr Calorimeter's on-detector and off-detector components need to be upgraded

On-detector Upgrades

Preamplifier - Shaper

- Objective:**
- Amplifies and applies a CR-(RC)² shaping function and produces 2 overlapping gains
 - Large dynamic range (10 mA for 25 Ω channels), low noise 350 nA for 10 mA channels

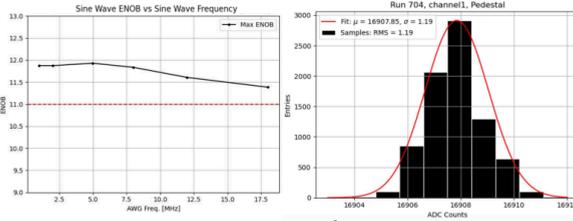
- Status: ALFE2 ASIC**
- Based on 130 nm CMOS technology
 - Cross-talk, linearity and noise exceeding specifications
 - TID tests demonstrated sufficient radiation tolerance



ADC

- Objective:**
- Digitizes analog signals at 40 MHz on two gains
 - 14-bit dynamic range with >11-bit precision

- Status: COLUTAv4**
- 40 MHz pipeline ADC MDAC in combination with a 12-bit pipeline SAR ADC
 - ENOB > 11 bits for up to 18 MHz input sine wave frequency
 - Pedestal noise: 1.2 ADC Counts RMS



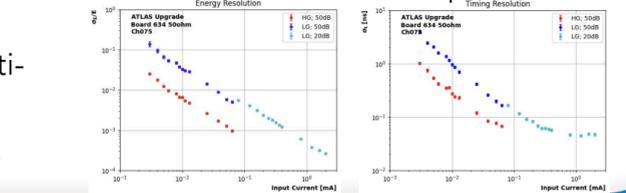
Calibration Board

- Objective:**
- Injects a pulse of known amplitude and shape directly on calorimeter cells for 128 channels
 - Must cover full dynamic range: 320 mA, up to 7.5 V output: requires HV-CMOS

- Status: Pulser and DAC ASICs**
- CLAROCv3 Pulser ASIC**
 - Based on XFAB HV-CMOS 180 nm technology with 4 calibration channels
 - LADOCv1 16-bit DAC ASIC**
 - Based on TSMC 130 nm CMOS technology

New prototypes LADOCv2 and CLAROCv4 submitted, expecting improved linearity and radiation tolerance

- Energy resolution < 0.1%, timing and multi-channel cross talk all within specification



Integration - Front End Board (FEB2)

- Objective:**
- Integrates PA/S, ADC and optical links
 - 1 FEB2 board handles 128 channels



- Status: Prototype - FEB2 slice testboard**
- 32 channels test with same FEB2 channel density
 - Functionality of full readout chain and multi-channel performance demonstrated with noise, sine wave, and pulse measurements

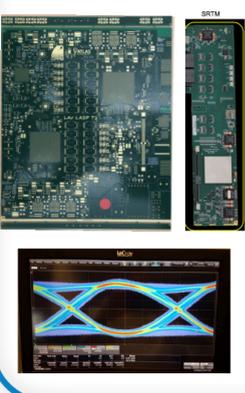
Off-detector Upgrades

LAr Signal Processor

- Objective:**
- Receives digitized waveform from 8 FEB2s
 - Determines energy and timing of signals for up to 1024 channels at up to 1.8 Tbps
 - Output data at 200 Gbps to the Global Event Processor and to the fFEX at up to 1 Tbps
 - Sends data, energy and timing to the DAQ at 60 Gbps upon receiving a trigger accept

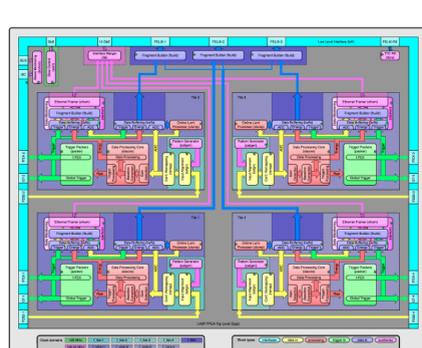
Status: LASP Test Board + SRTM

- Implemented using 2 Intel Stratix-10 FPGAs
- Optical testing of transceivers produces >65% open eye-diagrams



Status: LASP Firmware (FW)

- A more modular redesign of the FW brings about 1 tile/FEB2 option
- Successful injection of external data to test functionality
- Deep testing underway



LAr Timing System

- Objective:**
- Distributes trigger, timing and control (TTC) signals to FEBs and Calibration boards

Status: LATOURNETTE

- One central and 12 matrix Cyclone10 GX FPGAs
- Currently testing IpGBT interfaces: I2C, GPIO, and FMC Elinks
- Testing optical integrity with SFP+ links

