

The performance of the ATLAS Inner Detector tracking trigger in high pileup collisions at 13 TeV at the Large Hadron Collider (Run-2) and plans for Run-3



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ATLAS Inner Detector Trigger Tracking in A Nut Shell

ATLAS Inner Detector (ID)

The ATLAS Inner Detector tracker comprises three different detectors:

- the Silicon Pixel Detector (Pixel), including the Insertable B-Layer (IBL)
- the Silicon SemiConductor Tracker (SCT)
- the Transition Radiation Tracker (TRT)



Track Reconstruction in High Level Trigger (HLT)

- Rol (Region of Interest) derived from the L1 Trigger or Full-Scan
- Clustering: Associate neighbouring hits to form a cluster
- Create 3-Dimension Space Point (3D SP)
- Building triplets seeds using 3D SPs
- Constructing Track candidates
- Veto tracks not meeting pre-set criteria

High pile-up tracking in Run-2

Trigger Tracking Performance in Run-2

The Run-2 ATLAS Trigger system [1] consists of two level: Level 1 and High Level Trigger (HLT)., which is merged from the dedicated L2 Trigger and EF part. The L1 accepted rate is 100 kHz, while the HLT will reduce this to an average of 1 kHz and the averaged process time is 200ms per event. The tracking efficiency for leptons are close to 100% over the whole pile-up range.



What's going on in Run-3 high pileup tracking?

Tracking Speed-up with Dynamic Rol Z-width

Fullscan Tracking in Run-3

A more powerful HLT farm will be available in Run-3, which allows the HLT to process 8-18 kHZ particle flow. ATLAS plans to use the HLT to run FullScan tracking for all Jet and Missing- E_T (MET) triggers. To improve physics performance, we need to speed-up the CPU times. In order to store more physics ideas, we need to speed up the fullscan tracking to save more CPU time. In Run 3, the z-direction beam spread (σ_z) is expected to be within 37mm to 43mm and the default half RoI z width is 225 mm. Thus we can change the z-width to be $3\sigma_z$ according to the beam spread information. This will be dynamically updated during the data-taking. The plot on the right [2] shows the dynamic z-width can avoid scanning unnecessary region to save at least 30% CPU cost.



Tracking Speed-up with Seed Generation Optimization

Seed generation is a vital process in tracking, thus optimizing seed generation can save large amounts of CPU time. Different seeds, such as the PPP (Pixel-Pixel-Pixel) seed, the PPS (Pixel-Pixel-SCT) seed and the PSS (Pixel-SCT-SCT) seed, have different cost. The plots on the right [2] show the PPS seed costs and we can reduce 47.7% CPU time with 1% efficiency loss if we disable the PPS seed.





In order to reduce the number of fake seeds constructed. A ML-based algorithm has been developed to predict if a pair of hits belong to the same track given input hit features, focusing on cluster width and inverse track inclination. The application of a ML-based classifier for seed selection in the ATLAS ID has provided significant CPU savings on trained MC data at various pileup levels. The plots on the left [2] shows the ML-based seed achieve a speed-up factor of 2.3 with 1.1% efficiency loss in pile-up (< μ >) = 80.

Summary

In Run-2 the ATLAS ID Trigger achieve close to 100% efficiency in lepton tracking over the whole pile-up ranges. In Run-3, with the more powerful HLT farm, FullScan tracking will be available for all Jet and MET triggers. Several tracking speed-up algorithms are implemented to save CPU time for the FullScan tracking.

Reference: [1] Eur. Phys. J. C 82, 206 (2022) [2] HLTTrackingPublicResults Contact: zuchen.huang@cern.ch