FONDAZIONE BRUNO KESSLER

3D-Double-side Double-Type Column detector status at FBK

E.Vianello[b], G. Giacomini[b], A. Bagolini[b], M. Boscardin[b], L. Bosisio[c], G.-F. Dalla Betta[a], C. Piemonte[b], M. Povoli[a], N. Zorzi[b]

[a] INFN and University of Trento, 38123 Povo di Trento (TN), Italy
[b] Fondazione Bruno Kessler (FBK-irst), 38123 Povo di Trento, Italy
[c] INFN and University of Trieste, 34127 Trieste, Italy

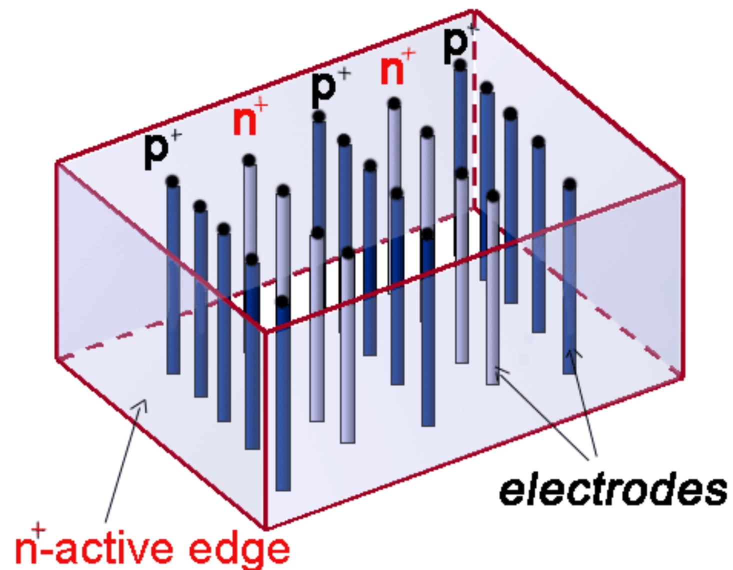
FONDAZIONE BRUNO KESSLER

Outline

- Introduction
- 3D DDTC detectors (non passing through columns)
- 3D-DDTC^{+} (passing through columns)
  - Technology
  - Preliminary results
- Conclusions

3D detectors – state of the art

First proposed by S. Parker et. al.
in NIMA 395 (1997), 328



Best result:
66% of the original signal after
8.8x10^{15} cm^{-2} 1-MeV $n_{eq.}$ fluence

C. Da Via et. al.
NIMA 604 (2009) 504

ADVANTAGES:

- Electrode distance and substrate thickness decoupled:
  - low depletion voltage
  - high speed
  - good charge collection efficiency
    → **High radiation hardness**

-Active edges:
  - Dead area reduced up to few microns from the edge

DISADVANTAGES:

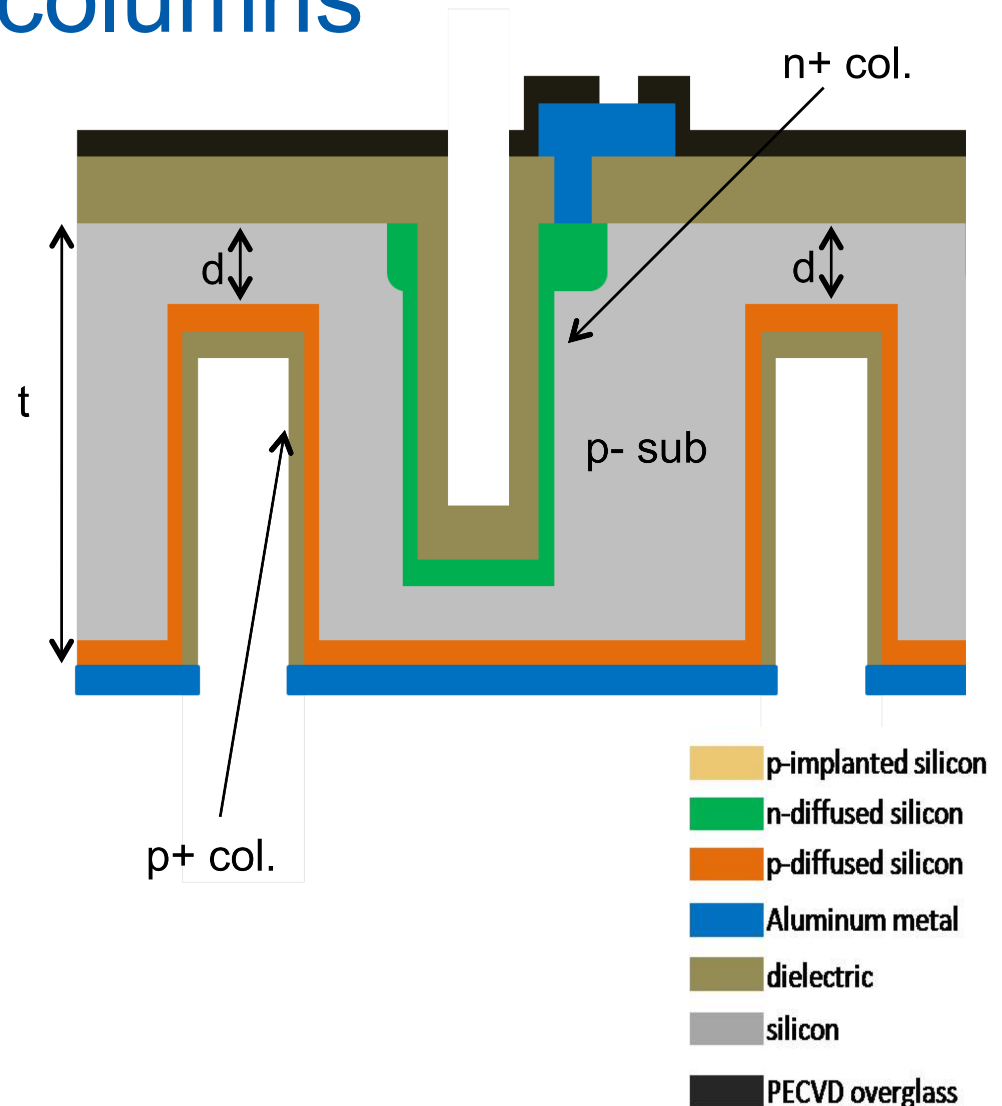
- Non uniform response due to electrodes
- **Complicated technology**
- Higher capacitance with respect to planar

3D-DDTC with non passing through columns

FONDAZIONE BRUNO KESSLER

SIMPLIFIED FABRICATION PROCESS

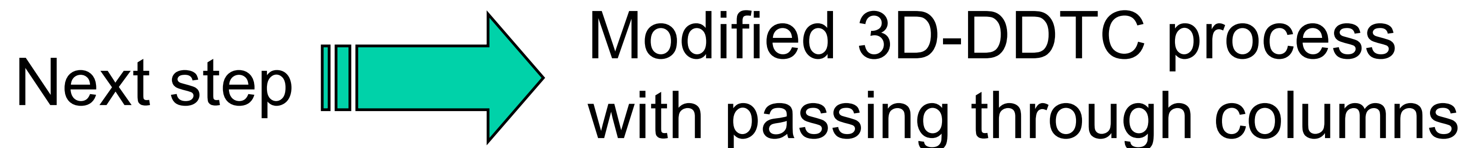
- **columns stop at a distance d from the opposite surface**
- no support wafers
- double-sided process
- holes (~10 μm diam.) are "empty" (no poly-Si)



3D-DDTC with non passing through columns: pros and con

- fabrication process reasonably simple
- good process yield
- even with non optimized gap "d", good performance up to irradiation fluence of 10^{15} n_{eq}/cm^2

- column depth difficult to control and to reproduce
- insufficient performance after very large irradiation fluences if "d" is too large

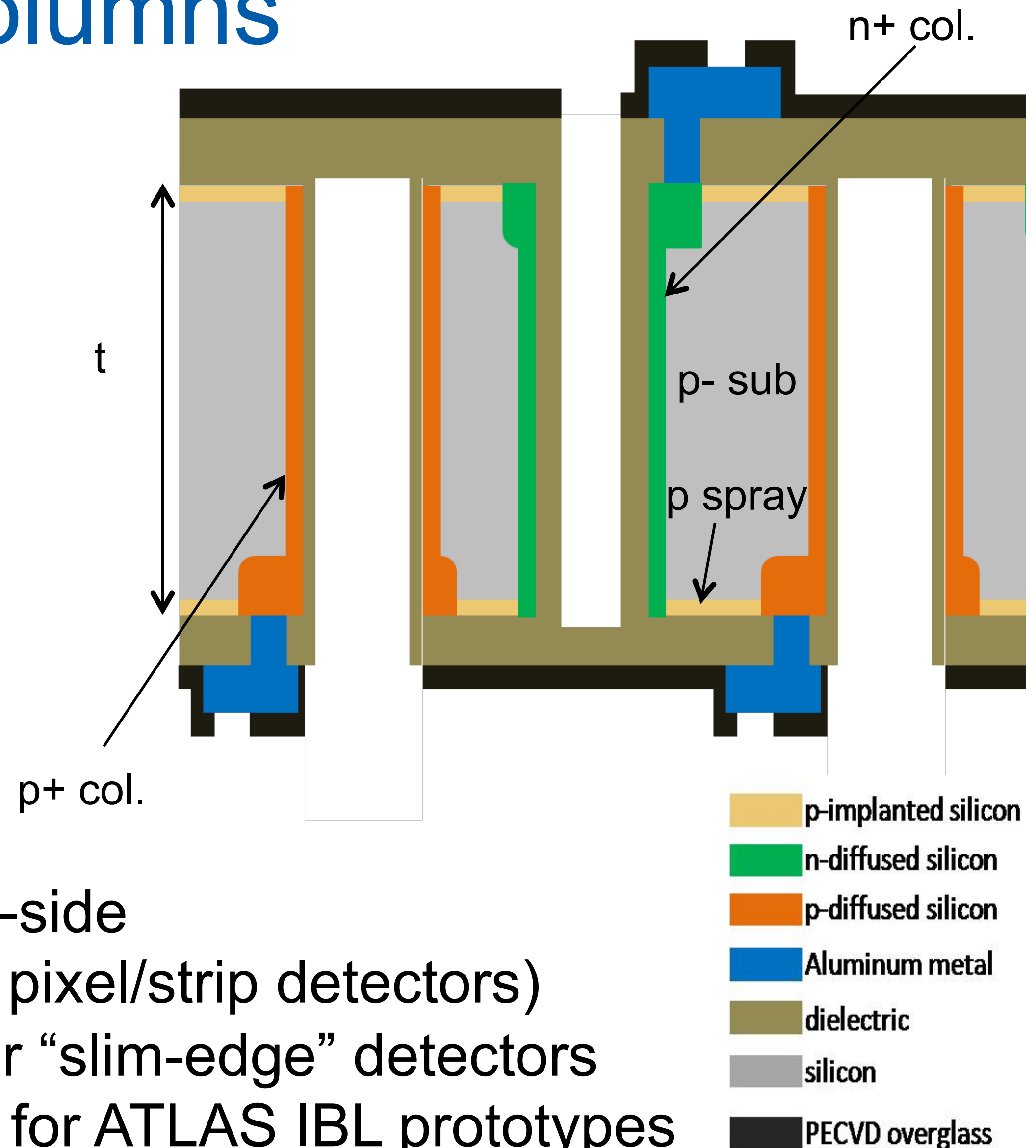


FONDAZIONE BRUNO KESSLER

3D-DDTC with passing through columns

Process aspects

- column depth equal to the wafer thickness
- full double side process
- no support wafer
- holes (~11 μm diam.) are "empty" (no poly-Si)

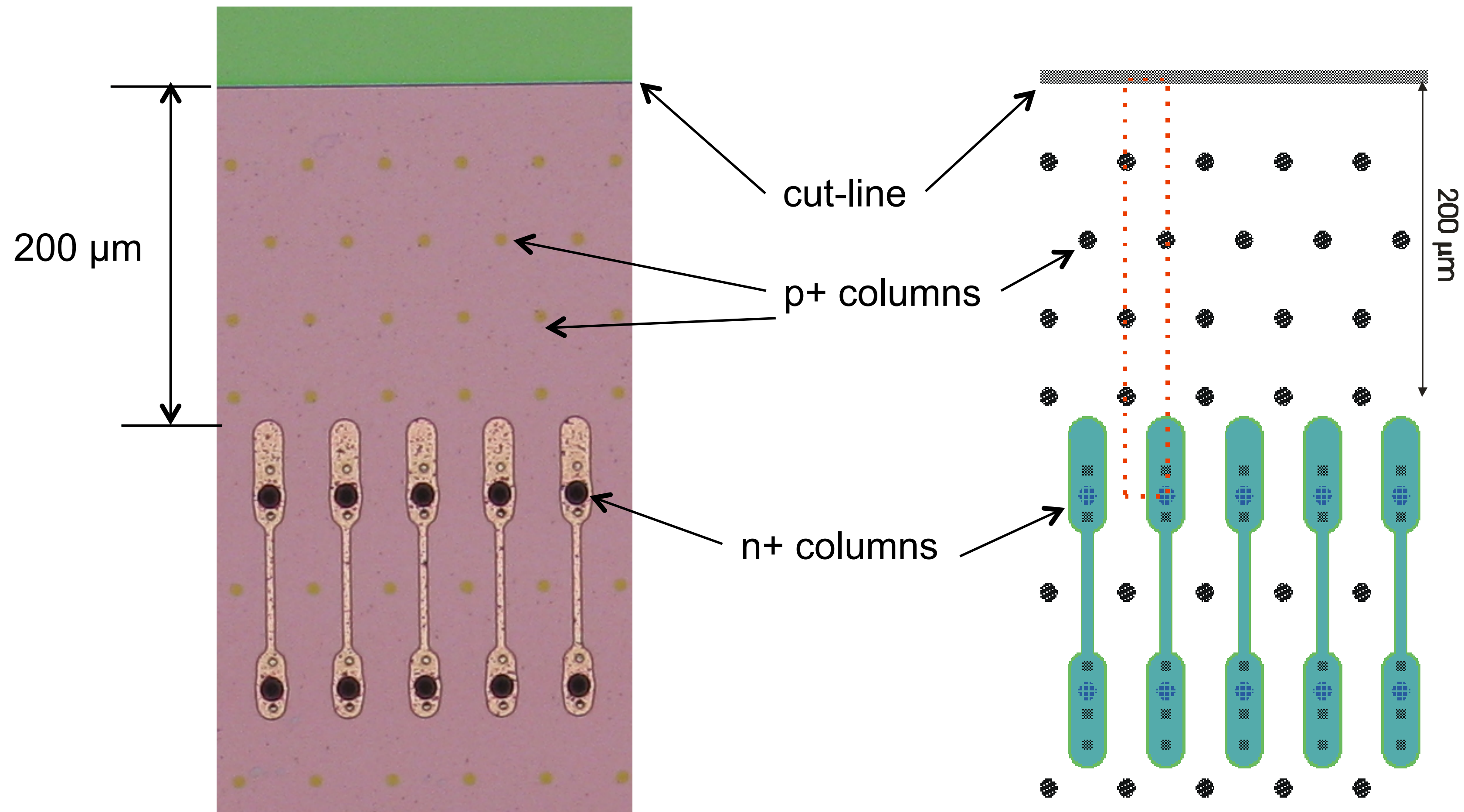


Main design options

- Substrate bias from the back-side (also suitable for dual-readout pixel/strip detectors)
- No active edge, but allows for "slim-edge" detectors
- Technology of choice at FBK for ATLAS IBL prototypes

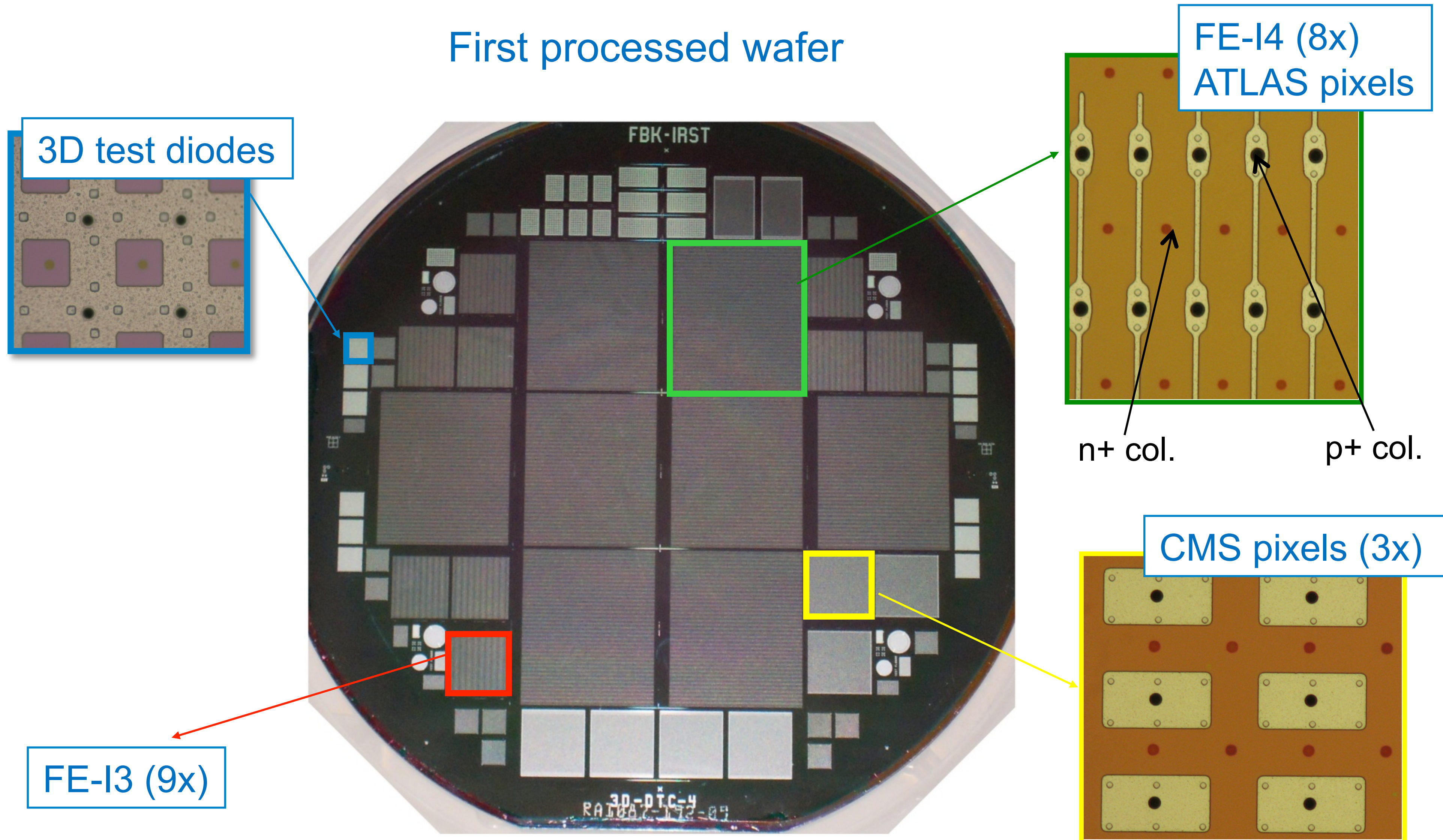
FONDAZIONE BRUNO KESSLER

Slim edge option



- multiple Ohmic fence termination
- dead area ~ 200 μm
- no leakage current drawn from highly damaged cut region

3D-DTC-4 some pictures

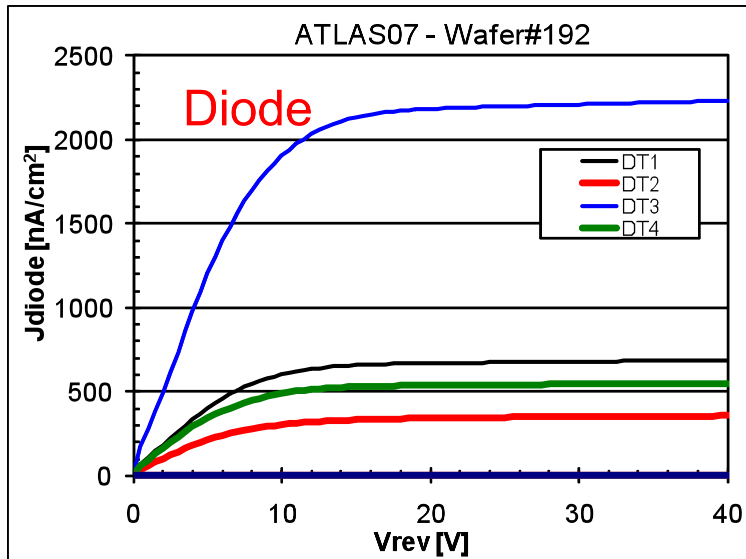


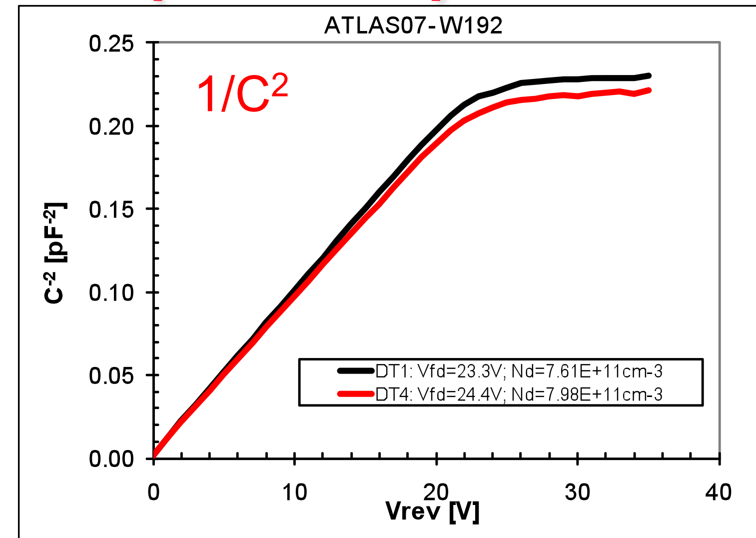
Future technological developments

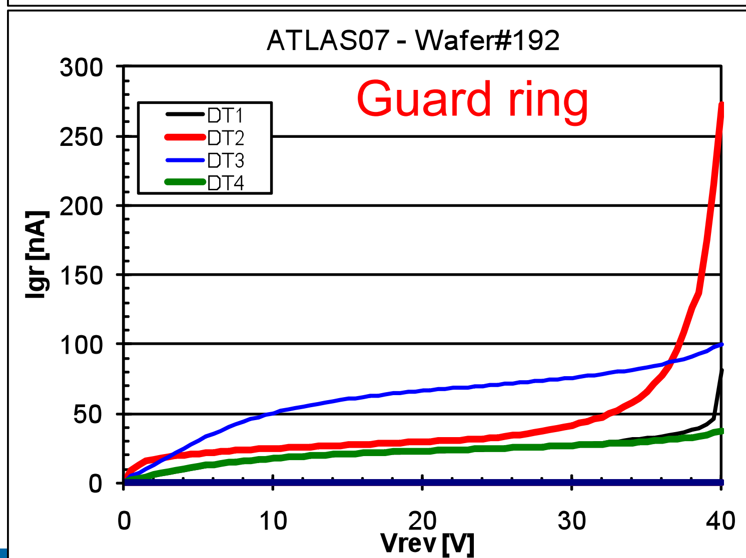
- We have 10 wafers almost ready for the electrical characterization (at the metal back)
- Process steps developments: new DRIE recipes for holes with higher aspect ratio, p-spray optimization, poly-Si filling of the holes
- Development of 3D detectors with passing through columns and active edge (with support wafer)

FONDAZIONE BRUNO KESSLER

3D-DTC-4: preliminary results (1)
Planar test diodes (4 mm^2)







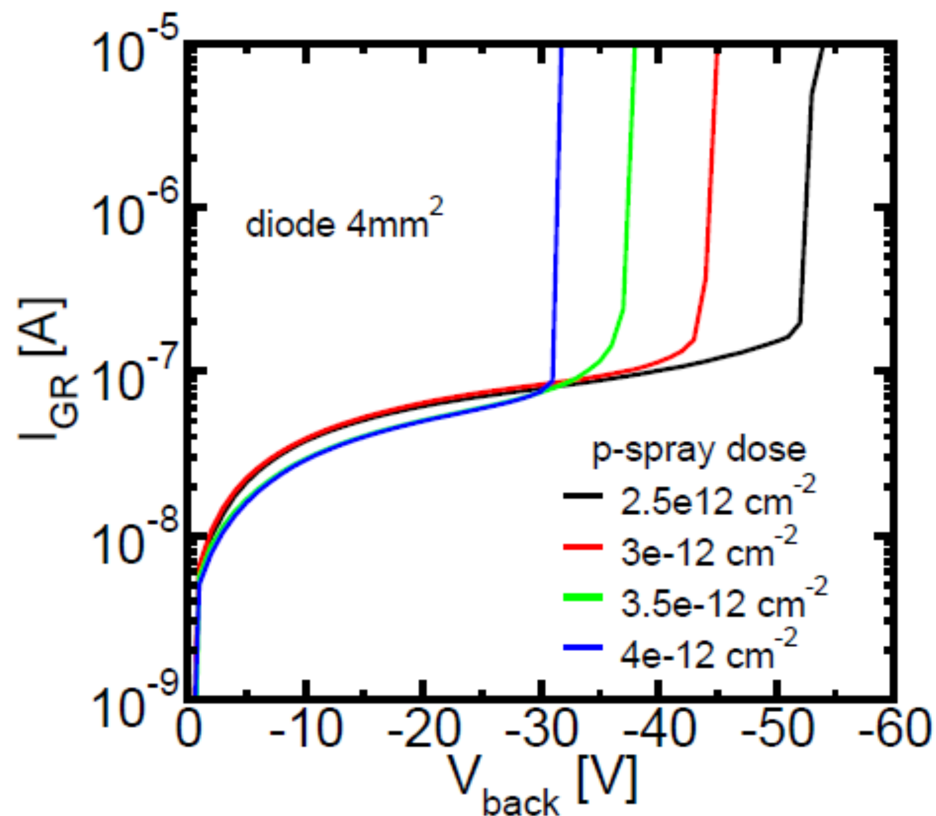
- J_{lk} ~ 500nA/cm^2 (higher than usual)
- V_{BD}~ 40-50V (p-spray)
- Vdepl ~20 V → ρ ~ 16 kΩ·cm
- Surface parameters ok:

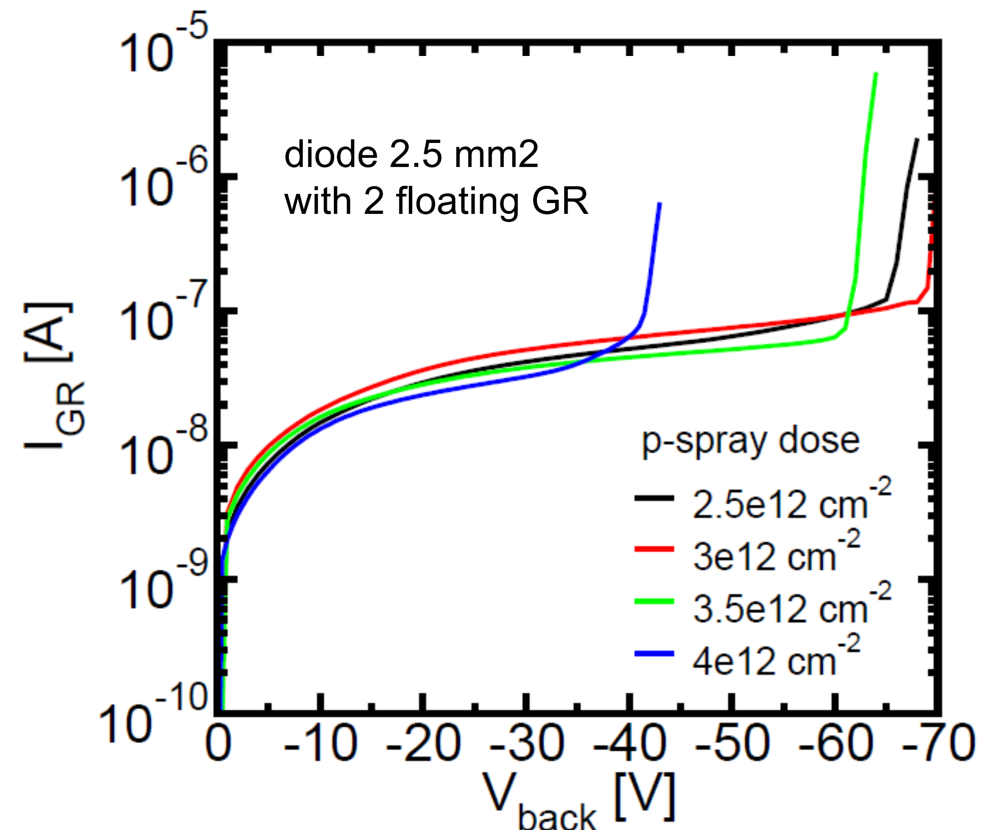
  s_0=10-30cm/s, N_{ox}=2-6x10^{11} cm^{-2}

FONDAZIONE BRUNO KESSLER

p-spray optimization studies

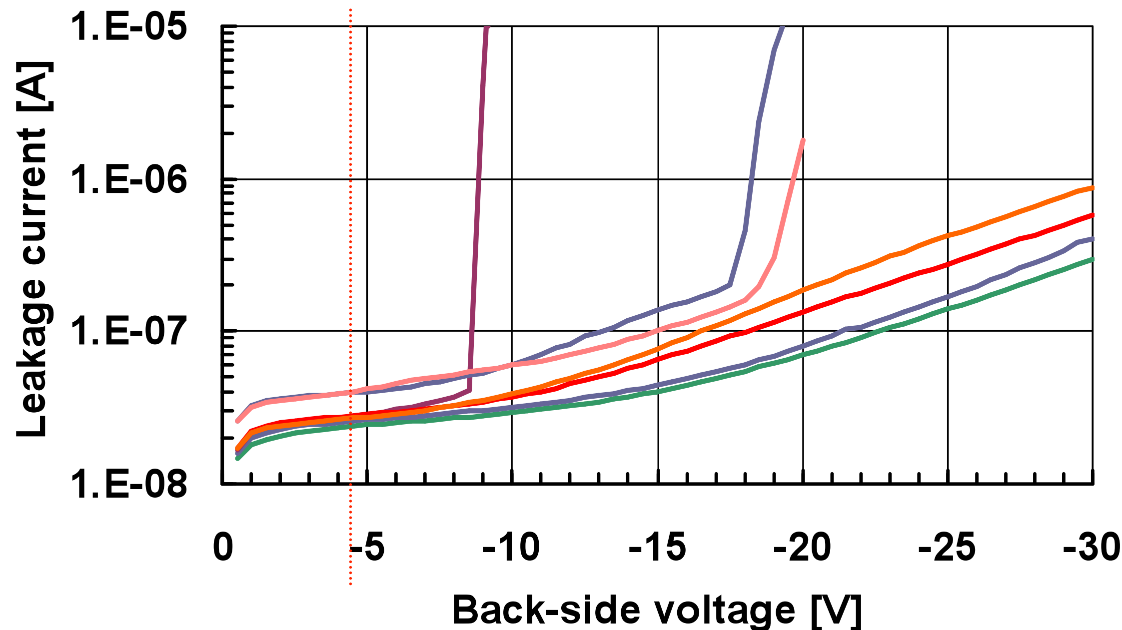
- Test batches of planar structures processed in parallel to 3D batches and using the same thermal budget
- Optimized p-spray doping profile and layout being investigated

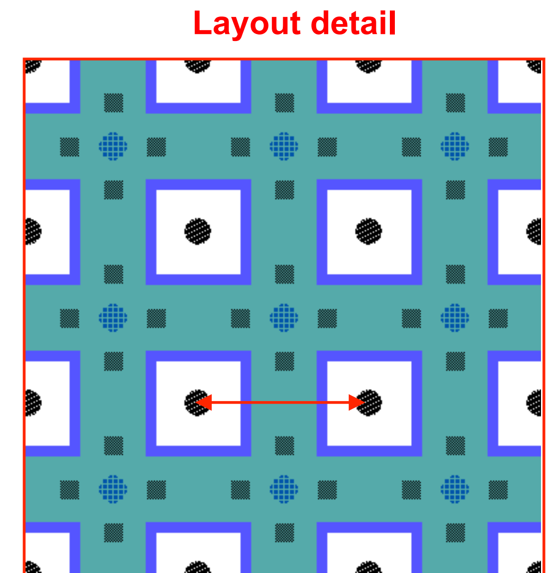




FONDAZIONE BRUNO KESSLER

3D-DTC-4: preliminary results (2)
3D test diodes (~10mm²), I-V curves



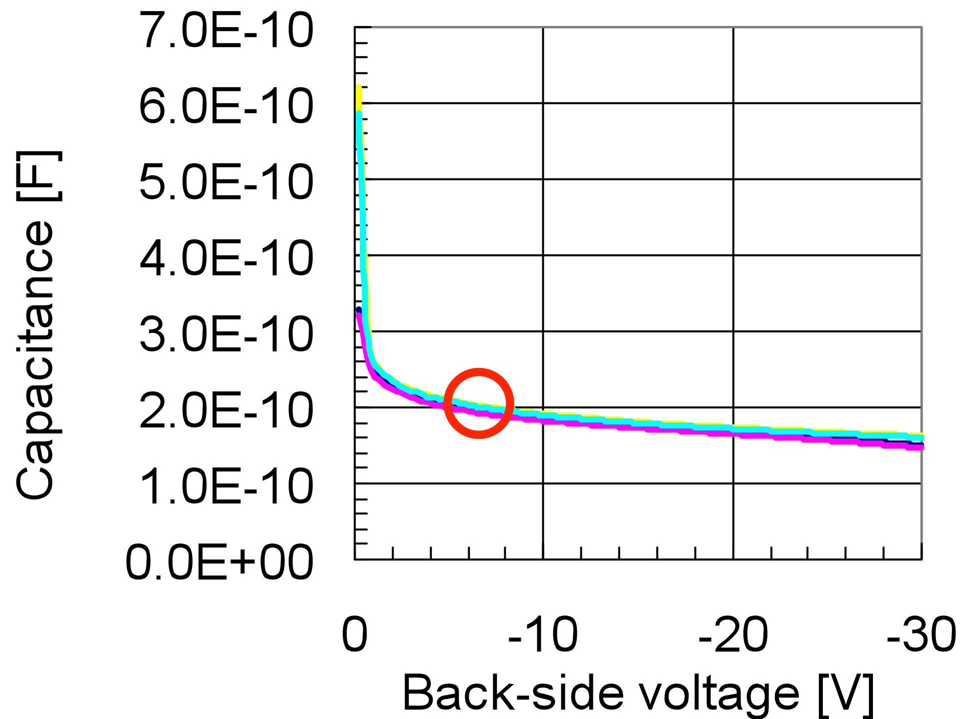


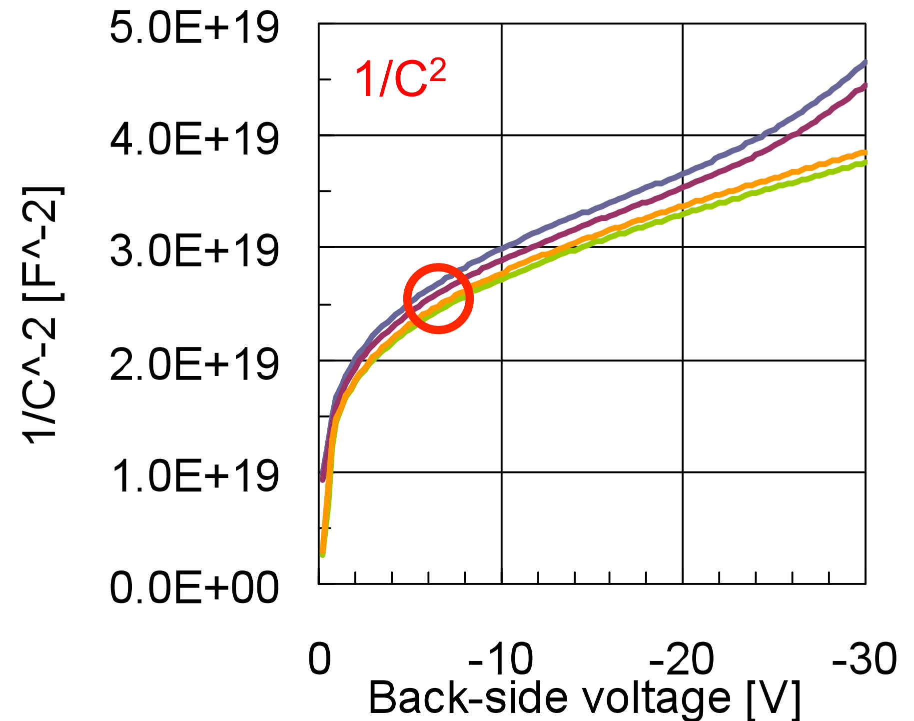
Array of 40x40 columns, pitch 80 μm

- J_{lk}~330 nA/cm² (~20 pA/col.) at V_{depl} (comparable to planar diodes)
- Leakage not degraded from DRIE but likely from mechanical stress
- Intrinsic breakdown (p-spray) + early breakdown due to defects

FONDAZIONE BRUNO KESSLER

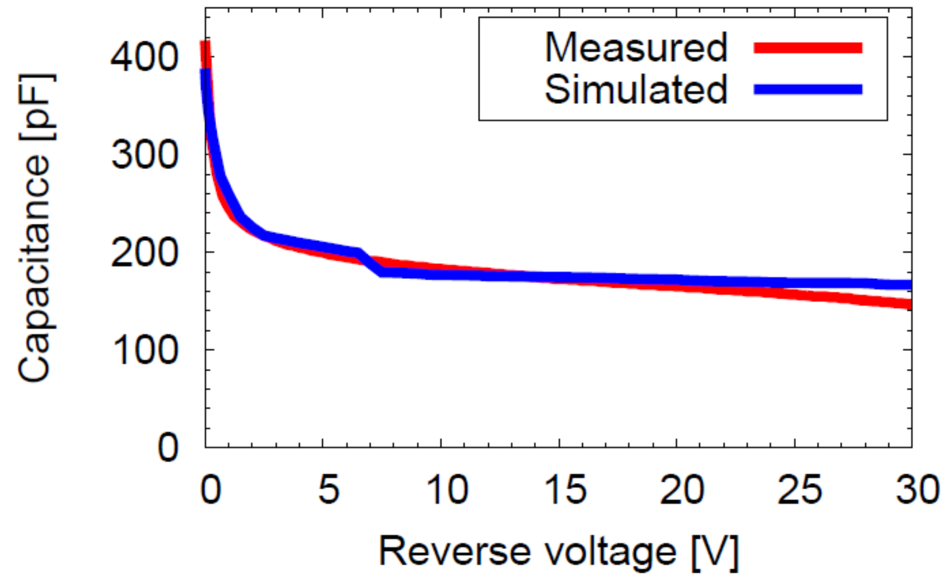
3D-DTC-4: preliminary results (3)
3D test diodes (~10 mm^2), C-V curves

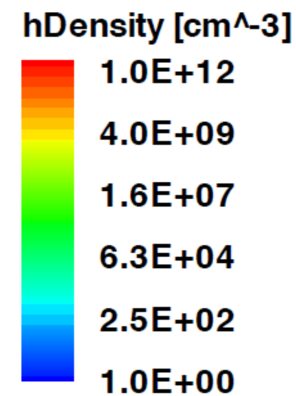


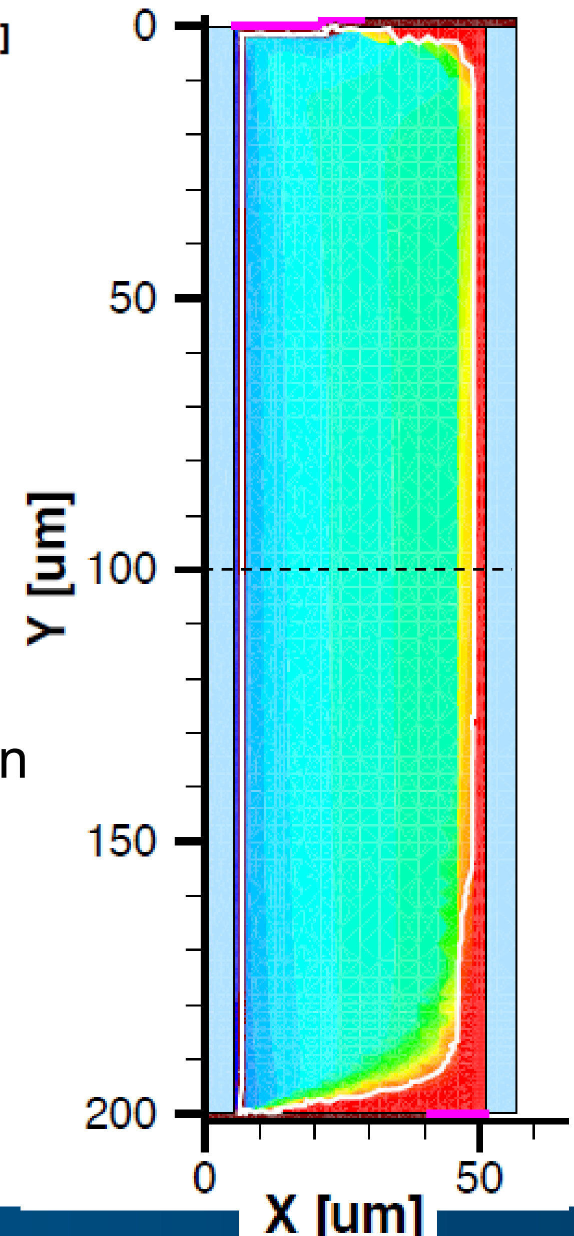


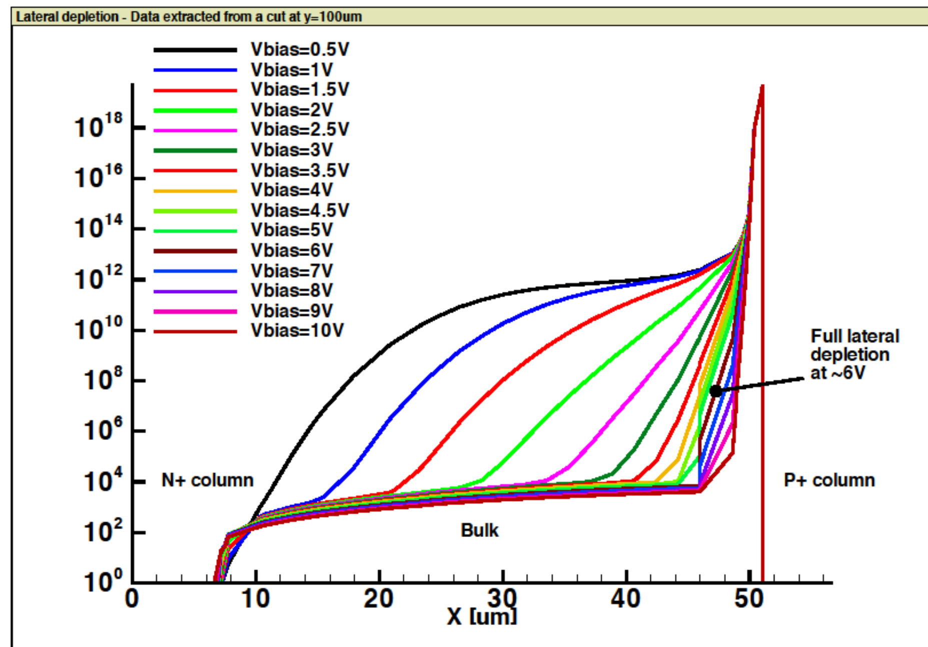
- Capacitance ~200pF (125 fF/col.) at V_{depl}
- Non negligible contribution from surface (p-spray)
- Depletion at a few V (see next slide)

3D diode: C-V simulation









- Lateral depletion at about 6V

- Corner at the bottom difficult to fully deplete

FONDAZIONE
BRUNO KESSLER

Conclusions

- The development of 3D detector technologies at FBK-irst is proceeding with encouraging results
- To further improve performance and process reproducibility, 3D-DDTC$^+$ detectors (with "passing through" columns) have been developed and preliminary results have been reported
- More wafers to come in a few weeks with an optimized fabrication process which improve electrical parameters

6th "Trento" Workshop on Advanced Silicon Radiation Detectors (3D and P-type Technologies)

FBK – irst, Trento, Italy
March 2-4, 2011

TOPICS:

- Design and simulation
- Fabrication Technologies
- Radiation Hardness
- Read-Out
- Applications

Organizing Committee:

M. Boscardin, C. Piemonte | FBK-irst, Italy

G.-F. Dalla Betta | Univ. Trento, Italy

H.F.-W. Sadrozinski | SCIPP, UCSC, USA

G. Casse | Univ. Liverpool, UK

Y. Unno | KEK, Japan

Contacts: piemonte@fbk.eu, dallabe@disi.unitn.it