ATLAS ITk Pixel Detector Overview

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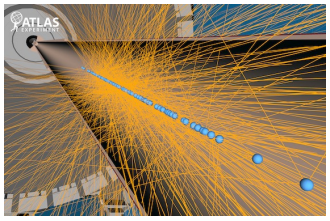
Introduction

https://twiki.cern.ch/twiki/bin/view/AtlasPublic/UpgradeEventDisplays



The Large Hadron Collider will upgrade to High-Luminosity LHC (HL-LHC) in 2027, with the physics motivations to largely expand the reach for Higgs physics e.g. the Higgs self-coupling measurement.

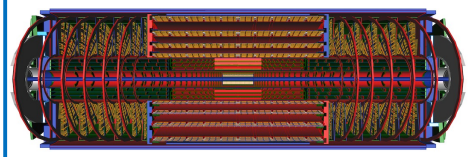
- LHC energy at 14 TeV and luminosity increase up to 7×10^{34} cm^{-2}s^{-1}, resulting in 200 proton-proton interactions (pileup) in a typical bunch crossing.

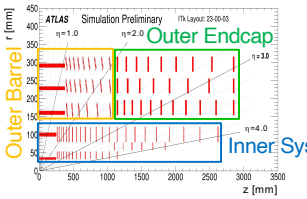
The ATLAS Inner Detector will be replaced by an all-silicon system, the Inner Tracker (ITk), to maintain or even improve physics performance in the harsher HL-LHC environment.

- Extended tracking acceptance, up to $|\eta| < 4$ to effectively reject pileup events.
- Increased granularity with smaller pixel size and optimized layout, to maintain occupancy below 1%.
- Increased radiation hardness, up to fluence of 2×10^{16} n_{eq}/cm^2 and TID of 1 GRad.
- Reduced material budget below 2.3 X_0 by innovative engineering e.g. module serial powering, carbon local support, and CO_2 cooling.

ITk pixel detector layout

ITk consists of 5 pixel (inner) and 4 strip (outer) layers, providing at least 9 hits per track in almost all |η|, with the innermost-layer location at 33 mm from the beampipe. The ITk pixel detector consists of 3 sub-systems.



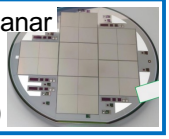


	Acceptance	Pixel area [m^2]	# of channels	# of modules
The current tracker	$\|\eta\|<2.5$	1.9	8×10^7	2k
ITk pixel detector	$\|\eta\|<4.0$	13	5×10^9	9k

ATL-PHYS-PUB-2021-024

Pixel sensors with larger granularity

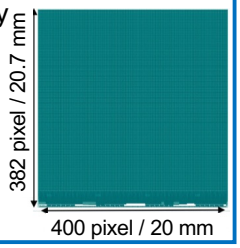
HPK planar



- Outer layers: n-in-p planar sensors (50x50 μm^2)
- Inner-most layer: 3D sensors with higher radiation tolerance (25x100 μm^2 and 50x50 μm^2)

Front-End ASIC in 65 nm CMOS technology

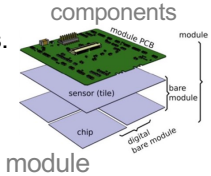
- Developed by RD53 Collaboration
- Radiation tolerance > 500 MRad
- 1 differential FE in 2x2 cm^2 (final design)
- 384 x 400 pixels with low pitch 50x50 μm^2
- Low threshold ~600e$^-$
- High bandwidth for 1MHz L1 trigger rate
  - 4 data links per chip at 1.28 Gb/s



Pixel Module Assembly: Sensor + ASIC + FLEX circuit

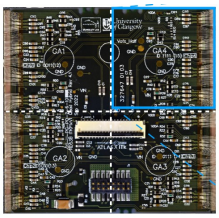
- Flip-chip assembly of silicon sensor with ASIC
- Flexible Printed-Circuit-Board (Flex PCB) glued on sensor, and wire bonded to ASICs.
- Two types of modules
  - Quad module: 1 planar sensor and 4 chips
  - Triplet module: one 3D sensor and 3 chips (for the innermost layer only)

Quad Module components



Ring triplet module

Quad module



Triplet module

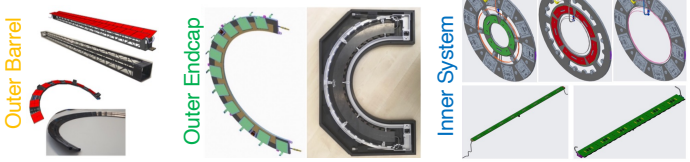
Stave linear triplet Flex

- About 200 module prototypes were built to validate ASIC design and hybridization process. Yield after metrology 97.5%.
- Consistent quality control e.g. by a series of visual inspections, metrology, electrical tests at operating low and room temperatures.
- 20 assembly sites are in ramp-up and prepare for the production rates. As site qualification, institutes are currently qualifying for the procedures of module assembly and test.

Local support

Prototypes use carbon fiber and carbon foam to minimize mass and maximize thermal performance.

- Different geometries optimized for the various layers and region of the pixel detectors.



- Modules are glued to local supports for integration.

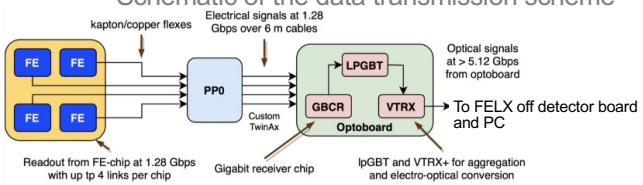
Services and Data Transmission

Electrical transmission at up to 4 x 1.28 Gbps/chip over 6m of custom twisted pairs

- Link sharing on the module with 1-4 ASICs as well as on all layers to reduce material.
- Serial powering chain → up to 16 quad modules

to reduce the material budget of the detector as well as power dissipation.

Schematic of the data transmission scheme



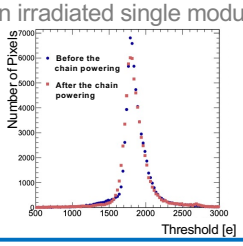
The result with demonstrators

ATL-ITK-PUB-2022-002

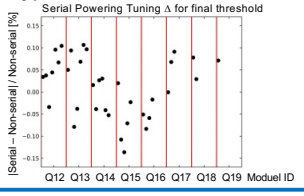
Prototypes loaded with 1st prototype ASIC (RD53A) readout, to test serial power chains, loading and mechanical integration.

→ No threshold significance before and after the chain powering.

for an irradiated single module



for the eight quad modules with 3rd prototype-ASIC (ITkPix v1.1)



Conclusion: The ITk Pixel system is finalizing an extensive R&D and prototyping phase, and has started (pre-)production of some components. Also finalizing production version of readout chips, systems, services and integration procedures. Large-scale production will start by the end of 2024.