Machine learning classifications on FPGAs

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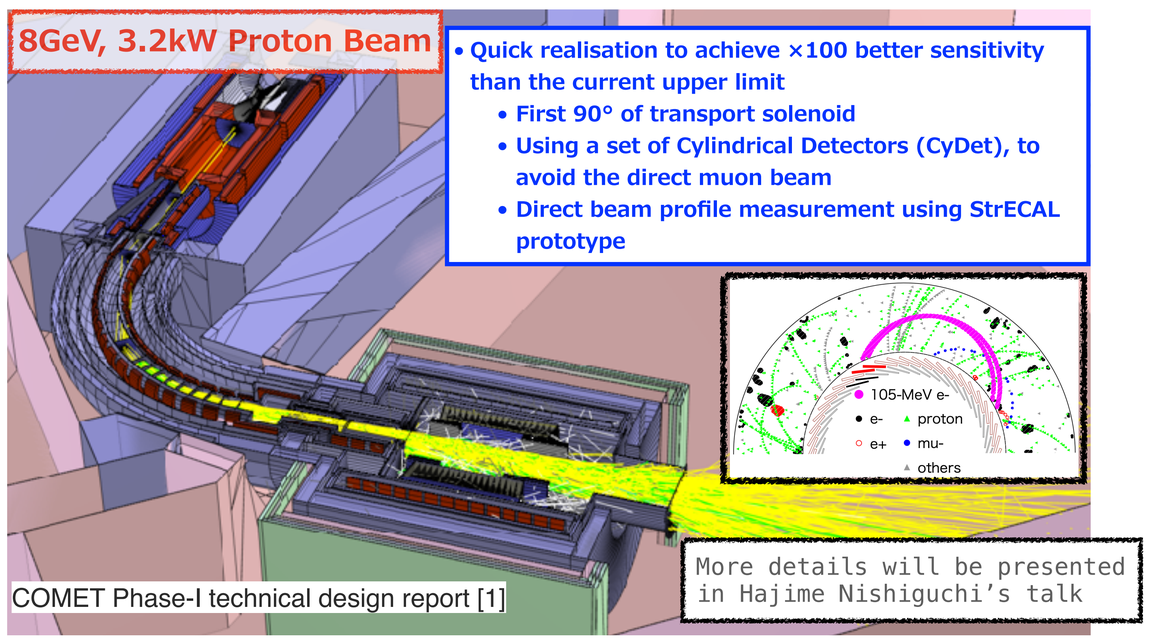
1. Introduction

The COMET experiment searches for the μ–e conversion with a sensitivity of O(10^{-15}) in its phase-I stage. Due to the extremely intense muon beam (10^{9} μ^-/sec) the timing detector faces 1–10 MHz single hit rate and the drift chamber cell's occupancy becomes around 40%.

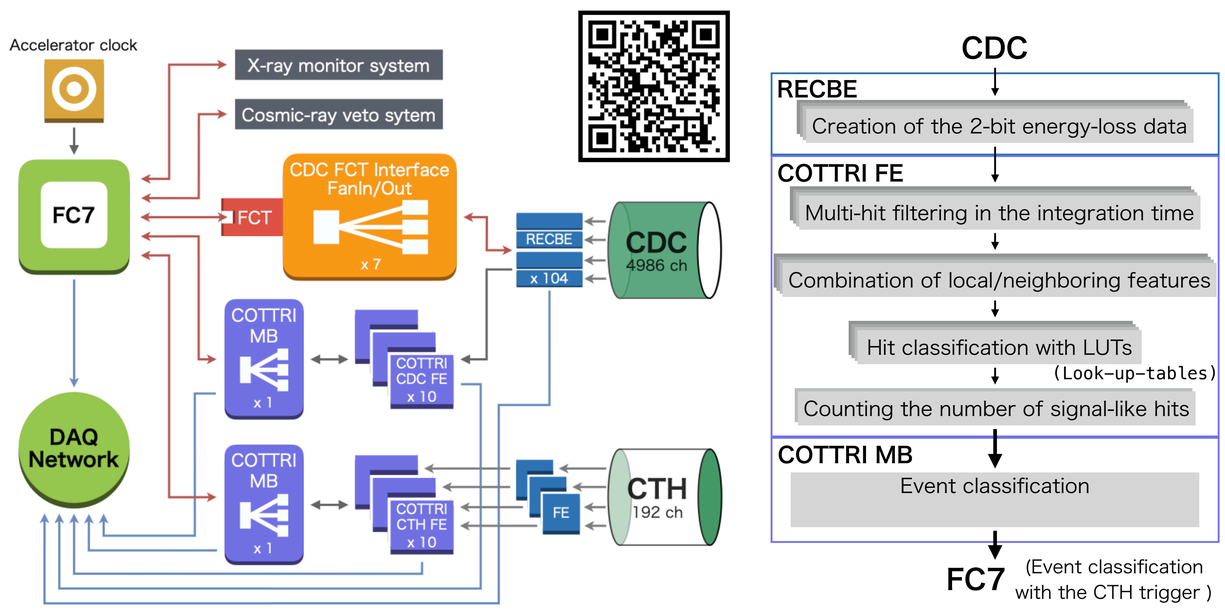
Key challenges;

- Finding the signal-like trajectories with high efficiency while suppressing the background rate
- Hardware limitations such as computing resources, data transfer rate, processing time, *etc*



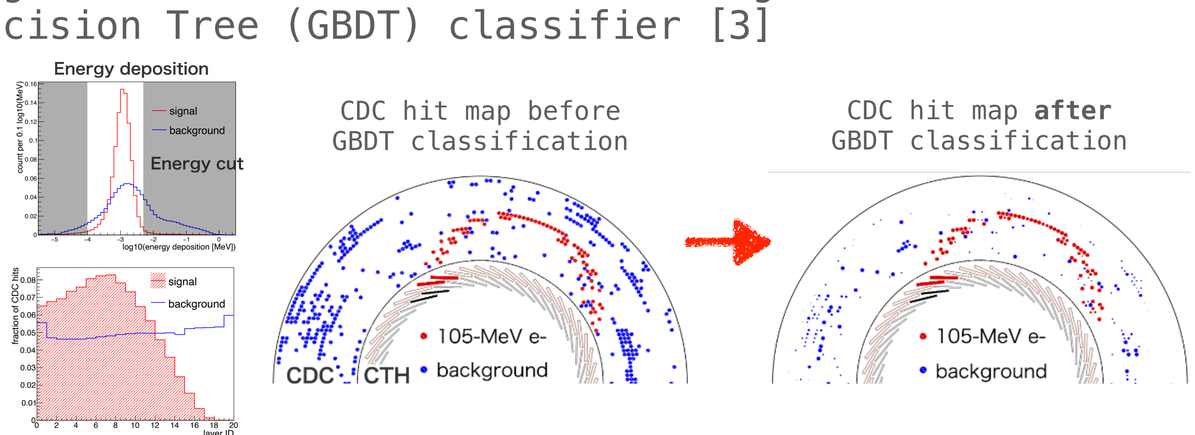
2. COMET Trigger System

The COMET trigger system consists of the central and front-end systems in COMET Phase-I
Due to the staging structure to cover the entire detector area without boundaries [2], **two stage classifications** are needed (**COTTRI Project**)



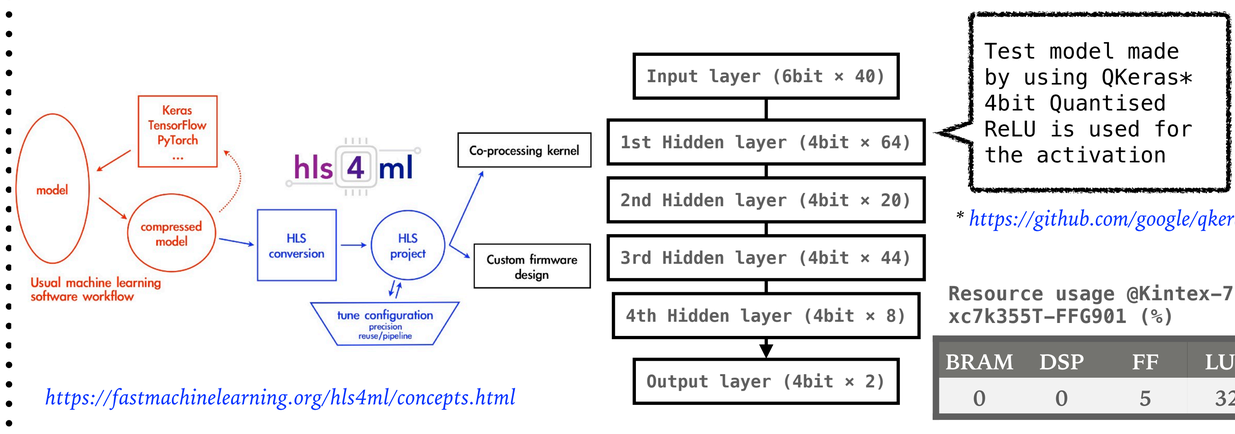
3. GBDT Hit Classification

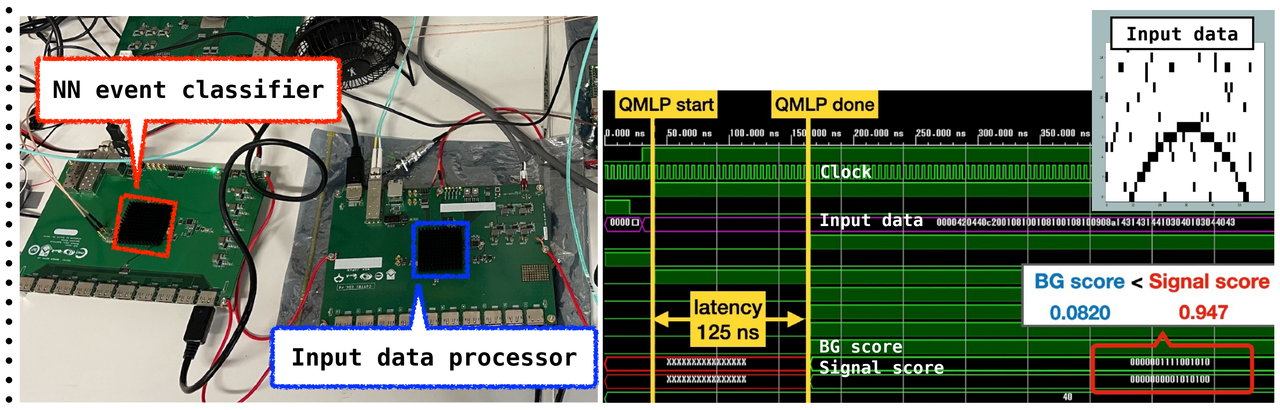
The hit classification performs by using the CDC hit local feature, namely, (1) compressed energy deposition, (2) wire position (3) the neighbouring wire info and (4) timing
➡ All of them are input data to calculate the signal-likelihood of each hit using Gradient Boosted Decision Tree (GBDT) classifier [3]



4. NN Event Classification

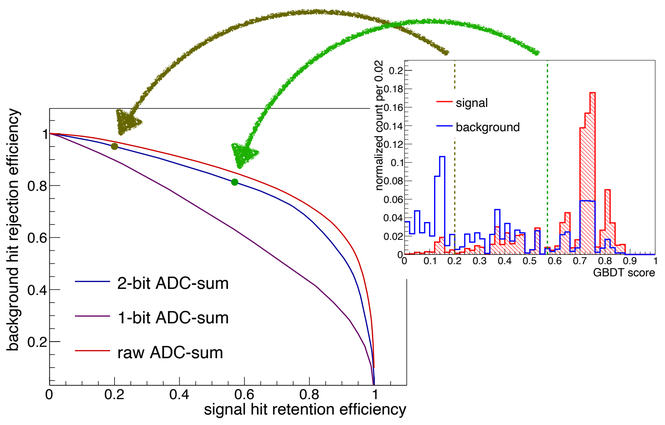
Neural network models can be converted to the FPGA firmwares by using high level synthesis (HLS).
A software called ***hls4ml*** [4] is used to simplify this step seamlessly from the model construction to the model evaluation using modern NN tools
To check the feasibility, quantised multilayer perceptron (QMLP) model has been tested.

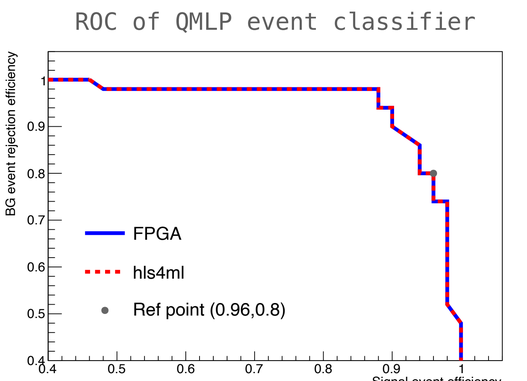




5. Results

- Reconfigurable LUTs were implemented into the FPGAs to perform the **GBDT hit classification**
  - Only 2 clock cycles required for processing
  - Reduce noise hits by **80%** while keeping more than half signal hits as for the trigger info
- **Neural network based event classification** is being considered as a fast and powerful event classifier
  - Simple QMLP has been implemented and tested
  - The FPGA board performs the event classification as expected from the hls4ml model prediction





7. Conclusions

We successfully **established the methods to develop and implement ML algorithms into FPGAs** for both hit classifications and event classifications.
The GBDT hit classification improves the online hit S/N by factor 2.5 – 5.
We confirmed that mid-class FPGAs can accommodate NN algorithms with good performance within **<150 ns.**
Together, **<13kHz** trigger rate is achievable

References

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[3] Y. Nakazawa, *et.al.*, https://ieeexplore.ieee.org/abstract/document/9443094
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