CMS L1 Track Trigger Upgrade

LeptonPhoton 2023

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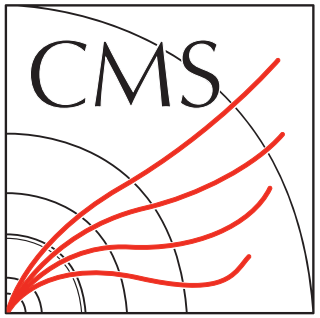
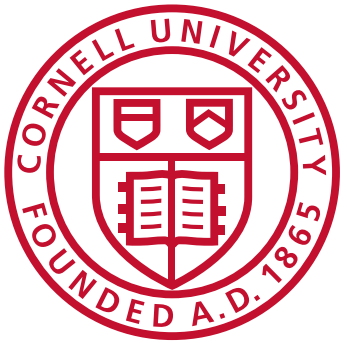


on behalf of the CMS Collaboration

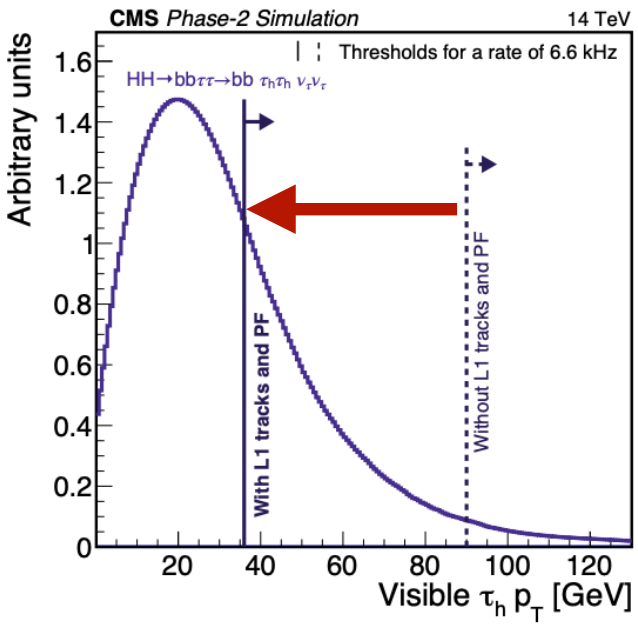
July 19, 2023

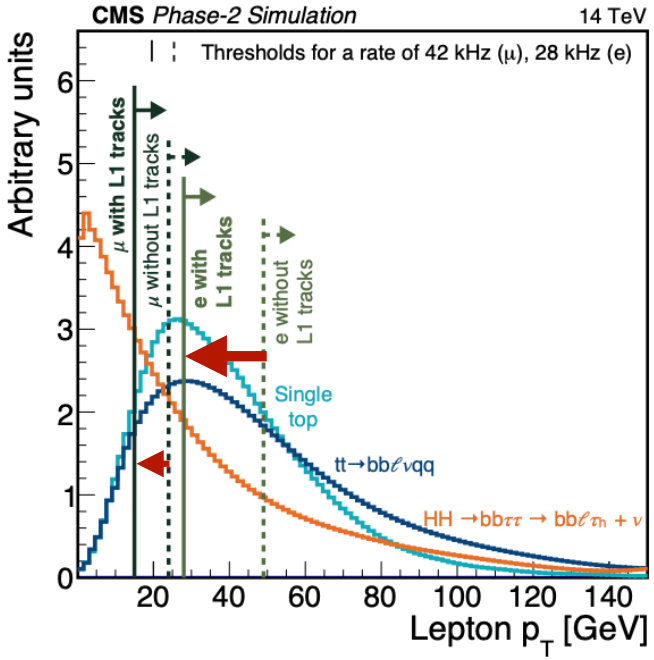


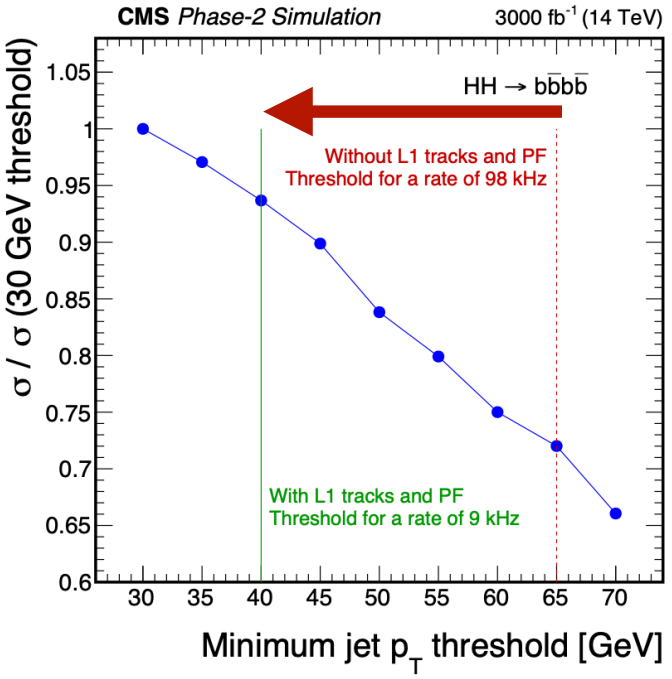
HL-LHC

- Rich physics but challenging condition at HL-LHC (pileup at 200!)
  - How to keep reasonable threshold at Level 1?

- Tracking!



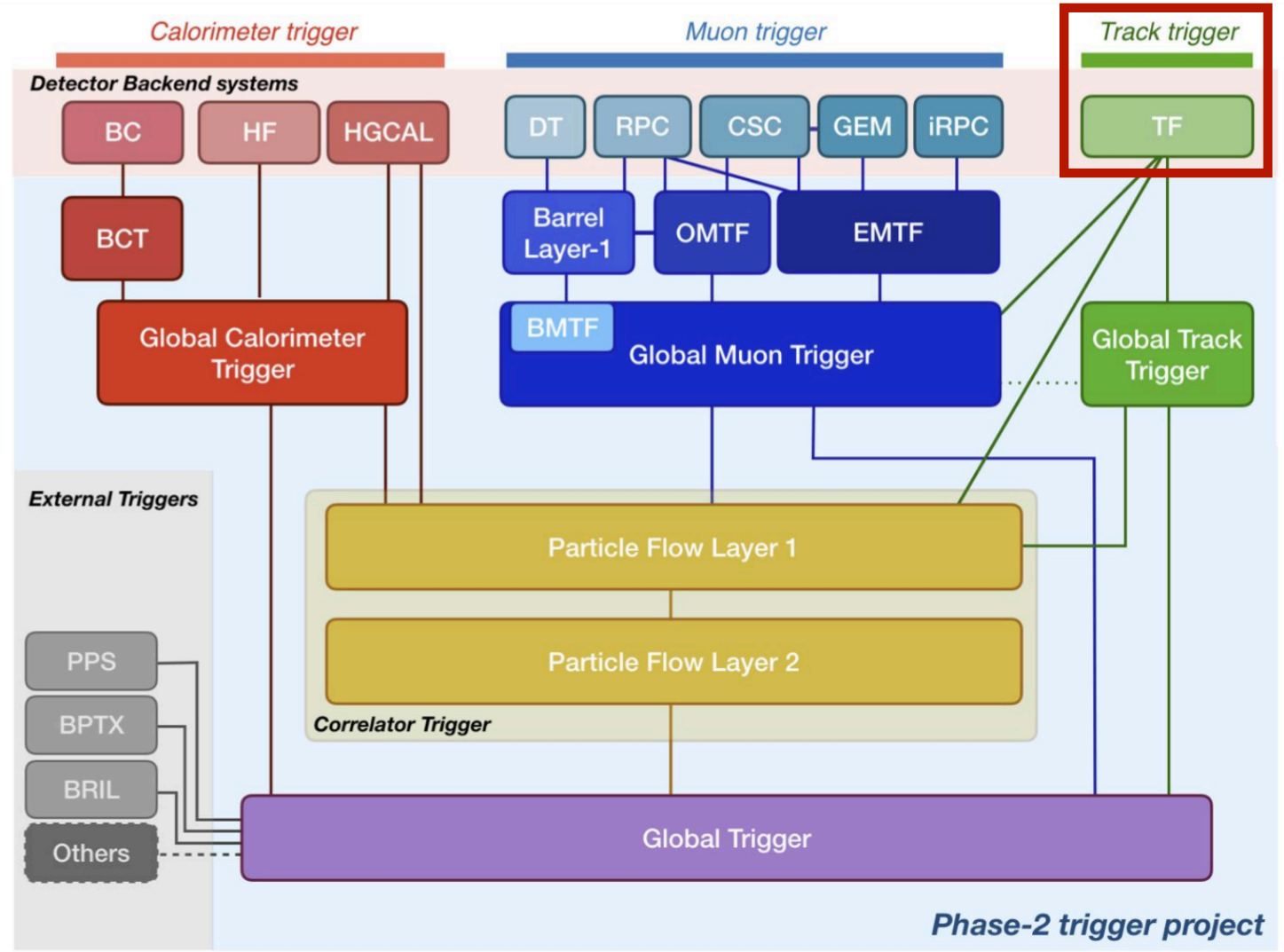




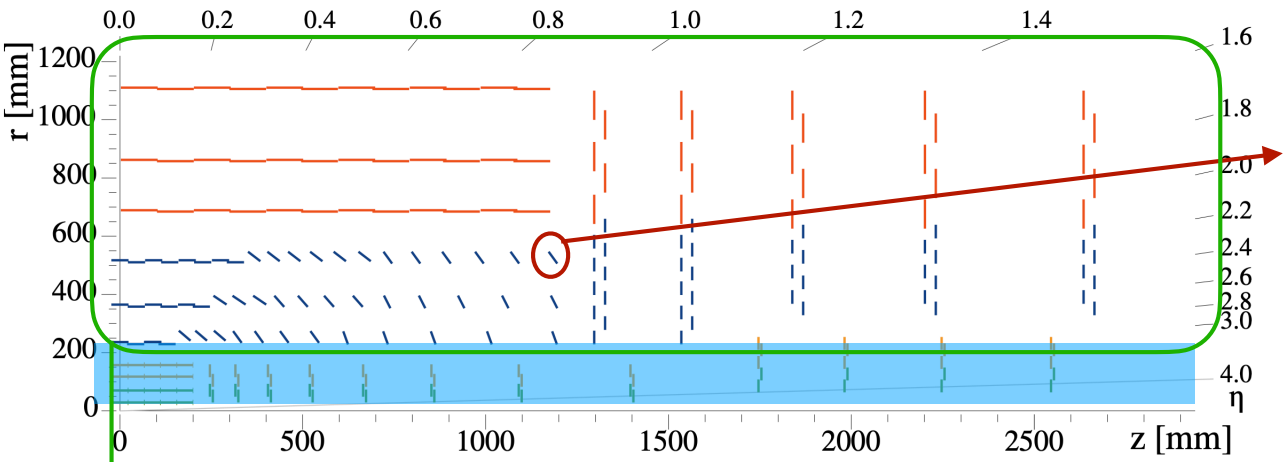
CMS-TDR-021

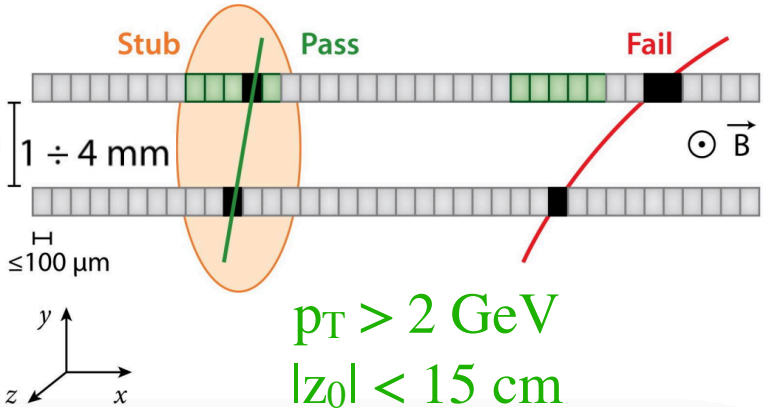
CMS Phase-2 Trigger Upgrade

- Tracking at L1 for the first time
- Challenging!



Phase 2 Outer Tracker





Data Trigger & Control

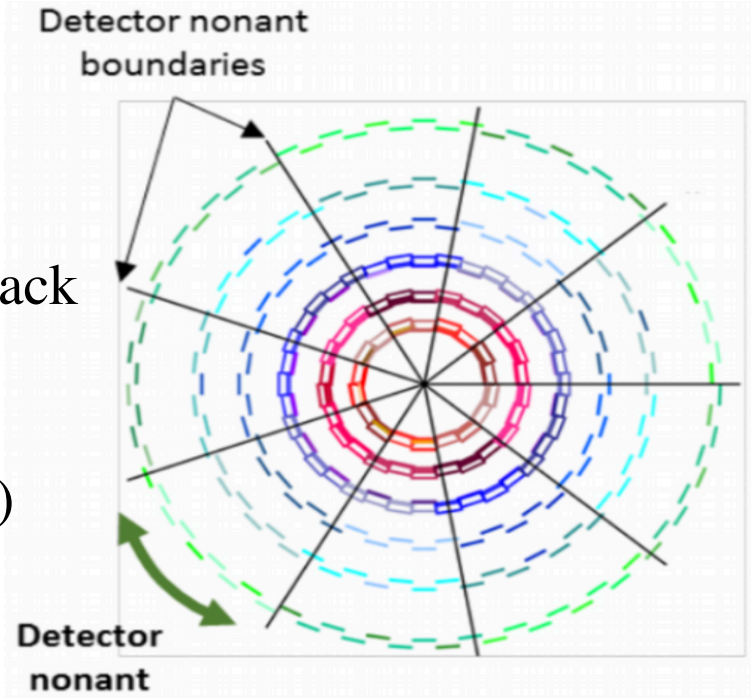
900 Gb/s/board

Track Finder

50 Gb/s/board

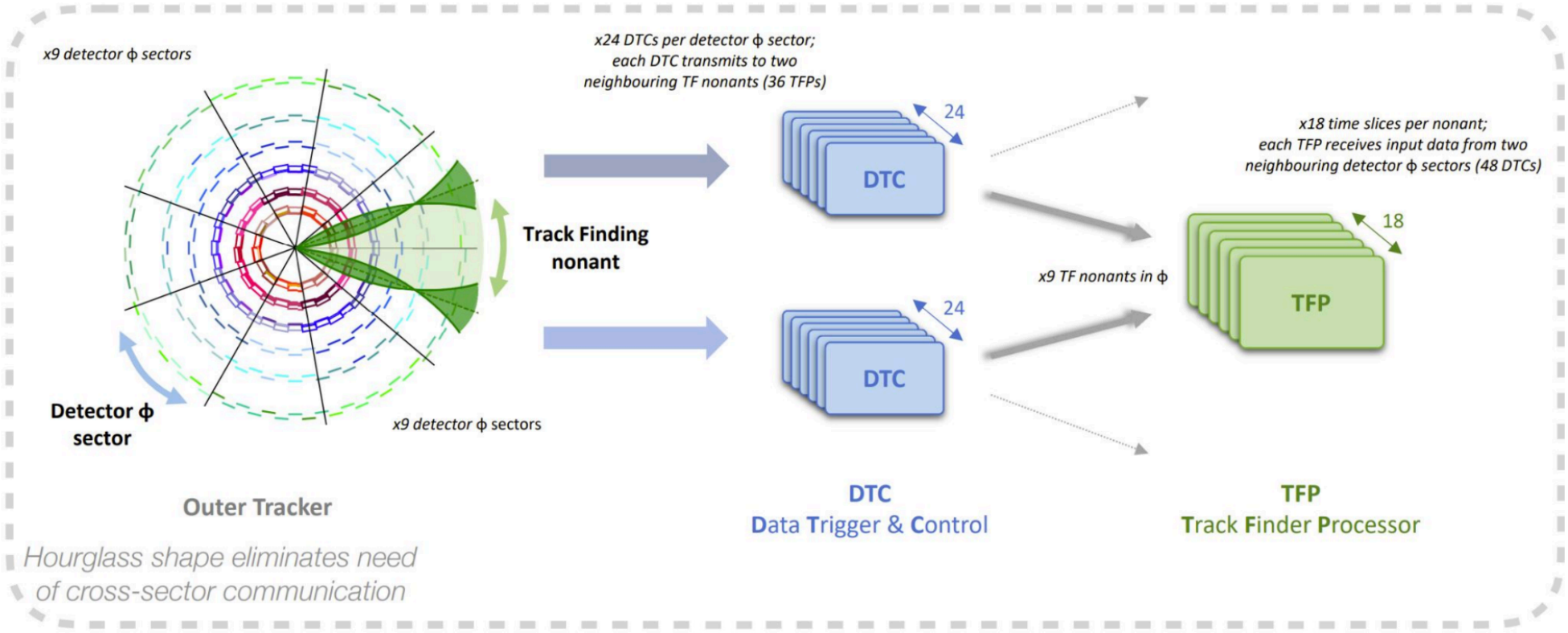
- p_T modules to reject low p_T tracks
  - Reduce data by factor 10-20
- Two stage processing:
  - Data Trigger & Control (DTC) → Track Finder

- 15k-25k stubs per bunch crossing (25ns)
- Need tracks within 5 µs after collision
- ~300 tracks with pT > 2 GeV

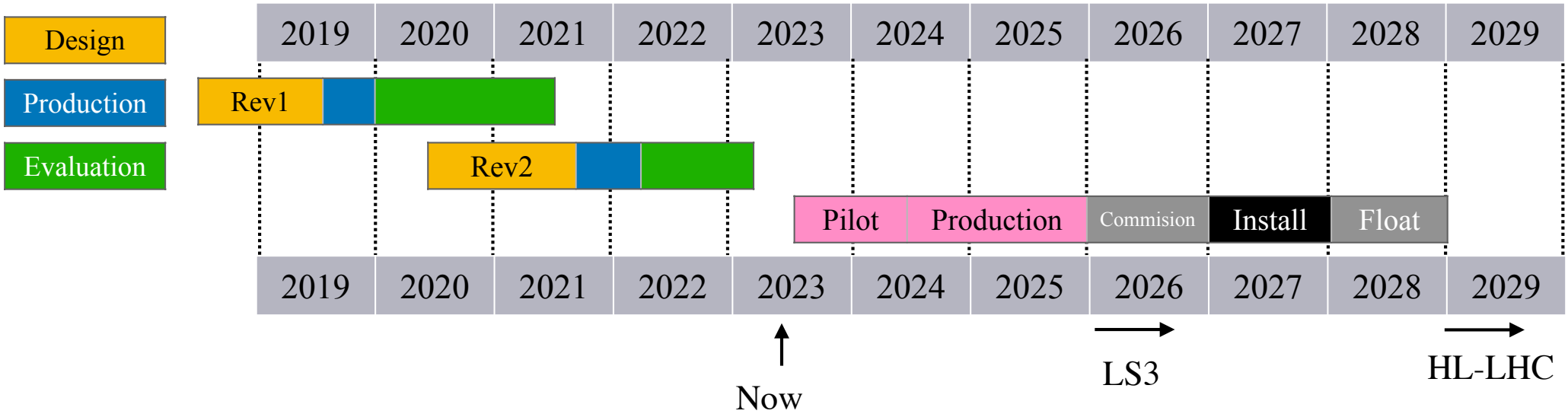


Parallelization

- Track Finder uses hourglass-shaped nonant
  - To avoid cross-sector communication
- 18 time slices per nonant: 9 x 18 = 162 TFP boards
- Each TFP board: 48 input, 6 output optical links @ 25 Gb/s



Hardware Plan



- Apollo ATCA platform will be used for TFP (talk, paper)
- Rev2 design fully evaluated
  - Clock related updates, upgraded components, Halogen-free material
  - 2 VU13P FPGAs, 100+ optical links @ 25 Gb/s (+52 inter FPGA links)
  - Link integrity tests, power/thermal performance
- Target optical engine (12 ch x25 Gb/s Firefly) still in prototype phase

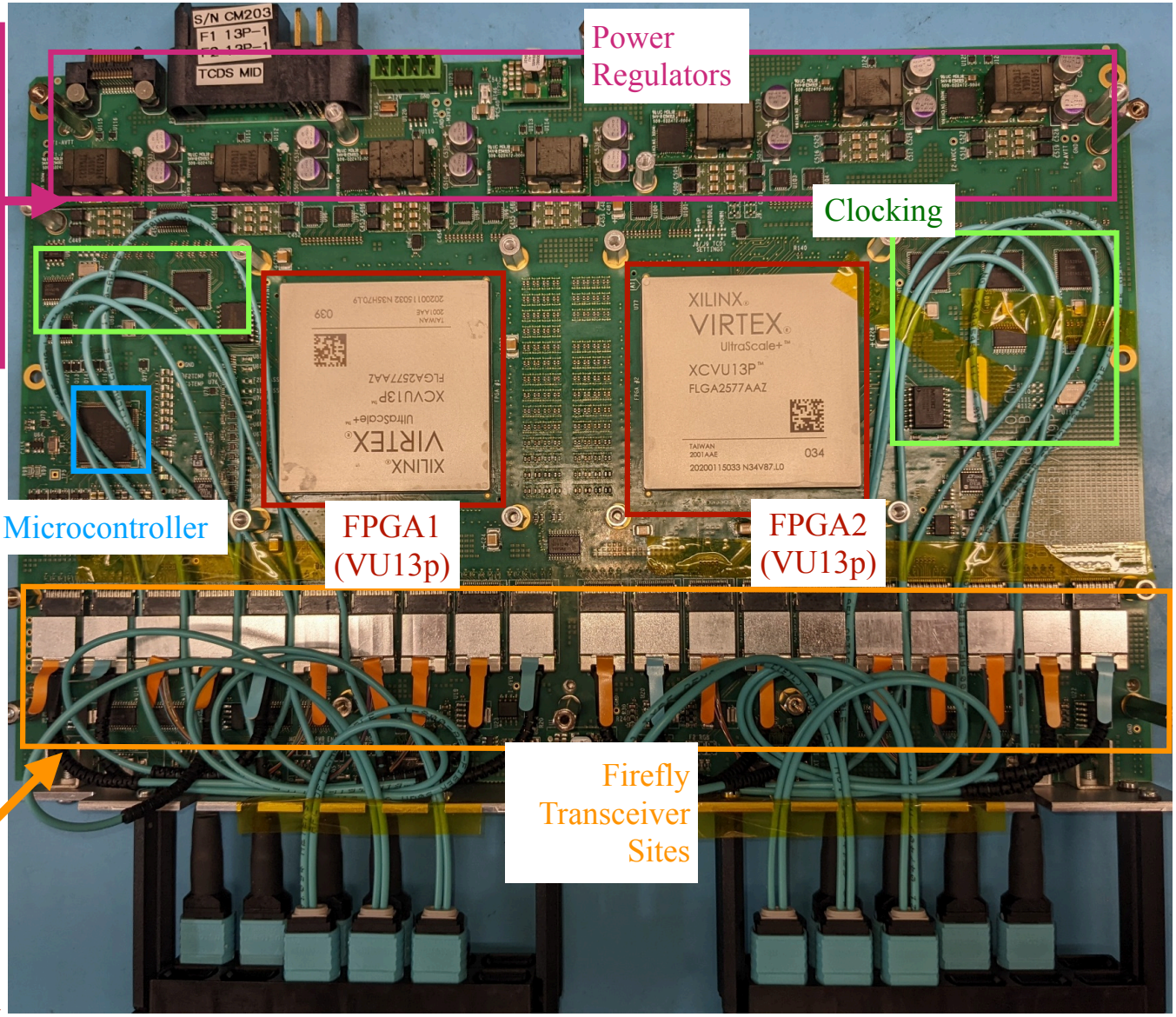
Apollo Rev2 Performance

With max FPGA temperature set @ 80 C (FF @ 35 C):

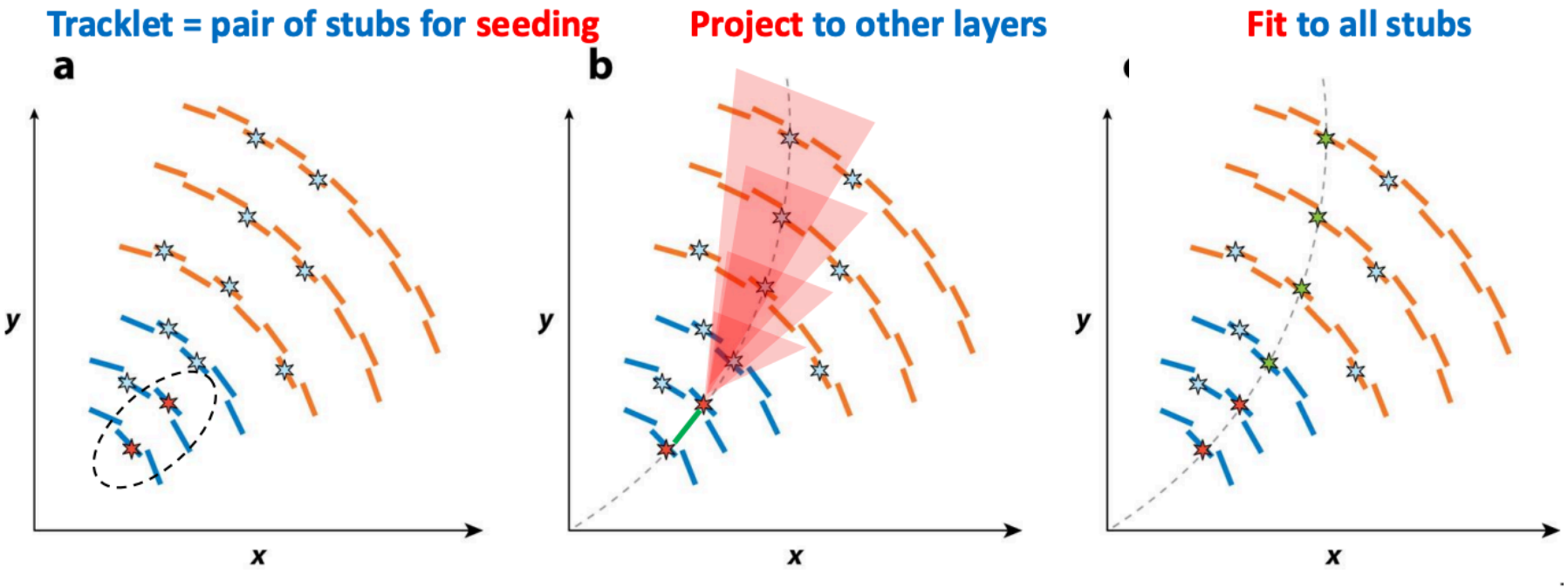
- Blade power reached ~300 W (max allowed)
- Net FPGA power ~200W

All Firefly links tested @ 25 Gb/s & achieved BER < 10^{-16}

Next: no major design change anticipated for pilot production



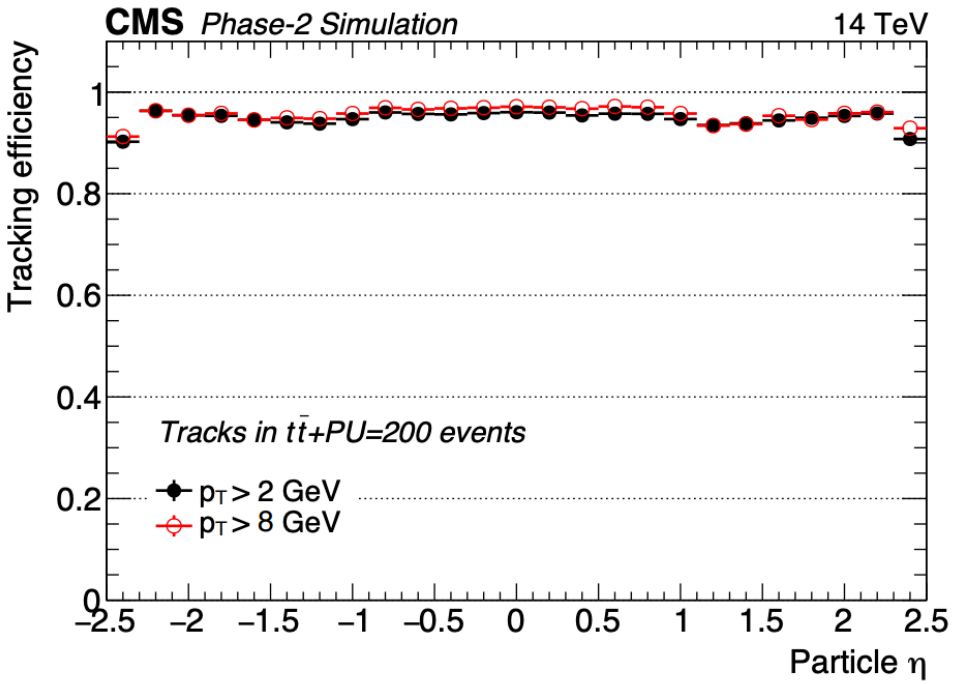
From Stubs to Tracks

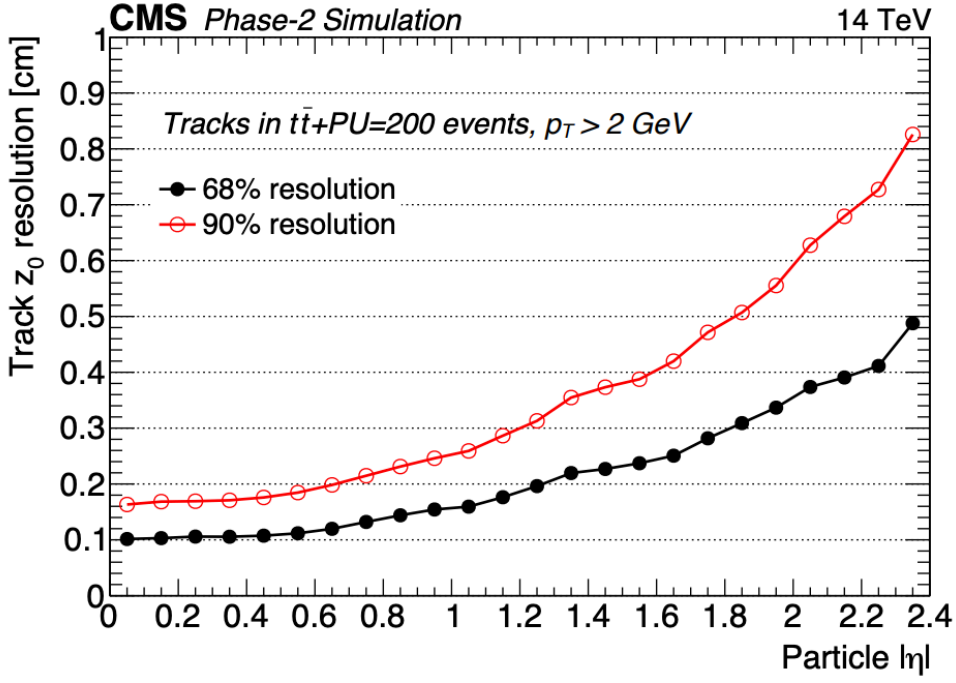


- Three major steps to tracks:
  - Seeding → Projection → Fitting

Tracking Performance

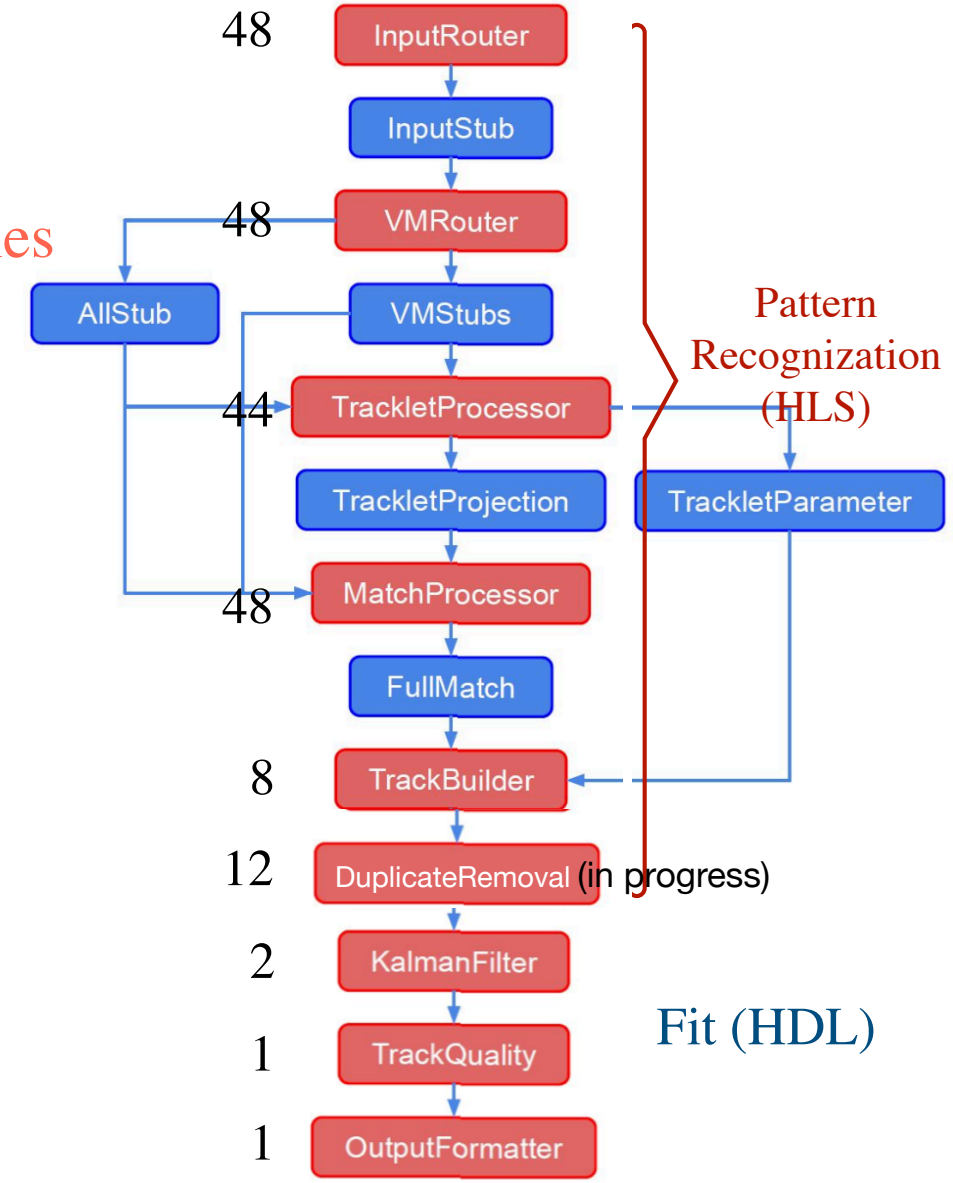
- Expected tracking performance based on simulation
  - High efficiency across p_T/η
  - Precise z_0 resolution for vertex association





Firmware Implementation

- Algorithm divided into HLS/HDL modules
  - Connected by RAMs when necessary
  - Each module tested individually
- Auto-generated HDL top level
- Feature:
  - Fixed latency target: 4 μs
  - New event received @ every 450 ns
  - Processing speed: 240 MHz

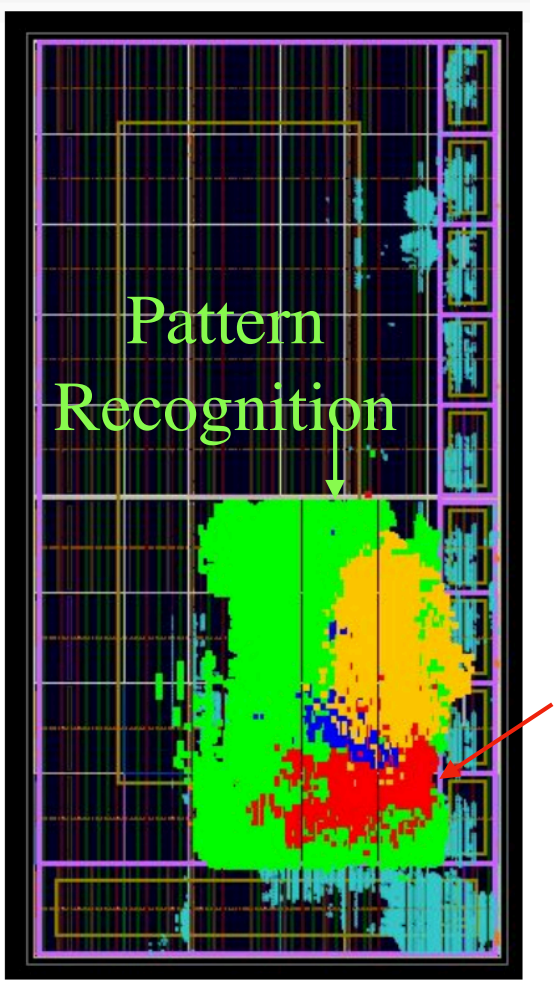


Firmware Integration

- Goal: build firmware for full detector step by step
- A ‘skinny’ chain was demonstrated on Apollo rev1
  - Covering a very small detector region
  - 1000 ttbar events + 200 PU

	Events in agreement (%)
Pattern recognition alone	98.1
Fit alone	100

- Moved on to full barrel project (2/3 of full) on Apollo rev2



VU7P

Full Barrel Project

- Seeding & stub matching only in barrel layers
  - Started with pattern recognization modules only

- Challenging to meet timing requirement (240 MHz)
  - Timing failure comes from routing issues

VU13P	LUTS	FF	BRAM	DSP
Total	364145	494844	923	1176
Available	1728000	3456000	5376	12288
Utilization (%)	21.1	14.3	34.3	9.6

- Machine learning based Vivado firmware <u>implementation strategy</u> helped

Setup

Worst Negative Slack (WNS):	-0.638 ns
Total Negative Slack (TNS):	-4295.708 ns
Number of Failing Endpoints:	25225
Total Number of Endpoints:	1230879

Timing constraints are not met.

Setup

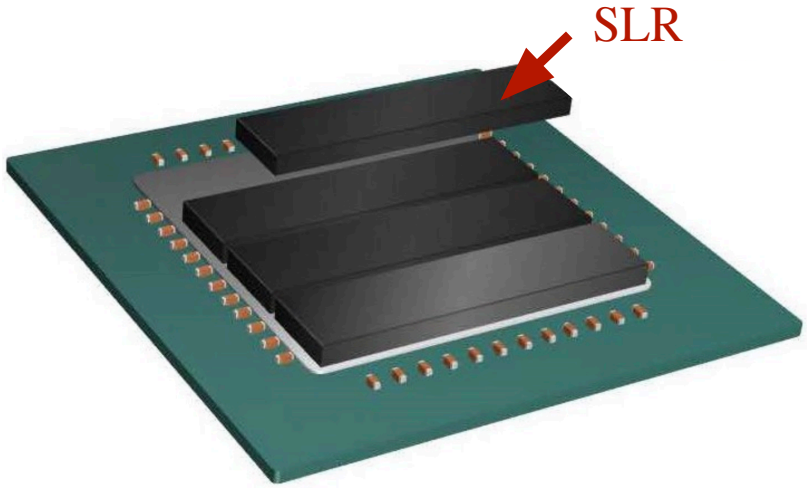
Worst Negative Slack (WNS):	-0.073 ns
Total Negative Slack (TNS):	-6.893 ns
Number of Failing Endpoints:	261
Total Number of Endpoints:	1088097

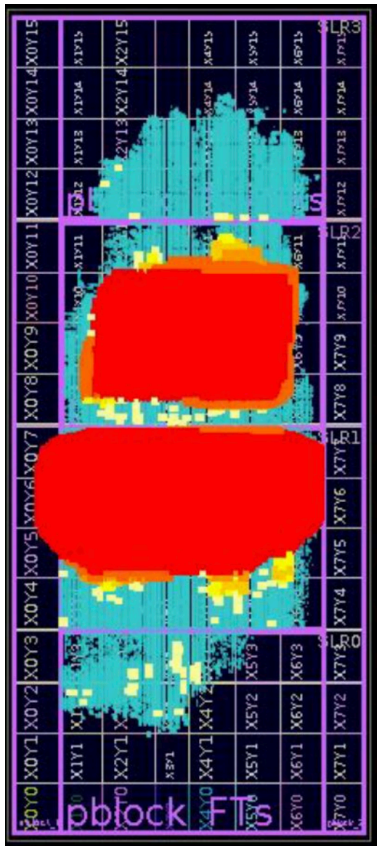
Timing constraints are not met.

Congestions & Solutions

- Lots of congestions between two modules (TP& MP)
  - Adding and optimizing pipelines helped

- Xilinx Ultrascale+ FPGAs use Stacked Silicon Interconnect (SSI) technology
  - Multiple silicon dies stacked and connected through an interposer
  - Each silicon die is called a Super Logic Region (SLR)
  - A lot of our issues come from signals crossing SLRs

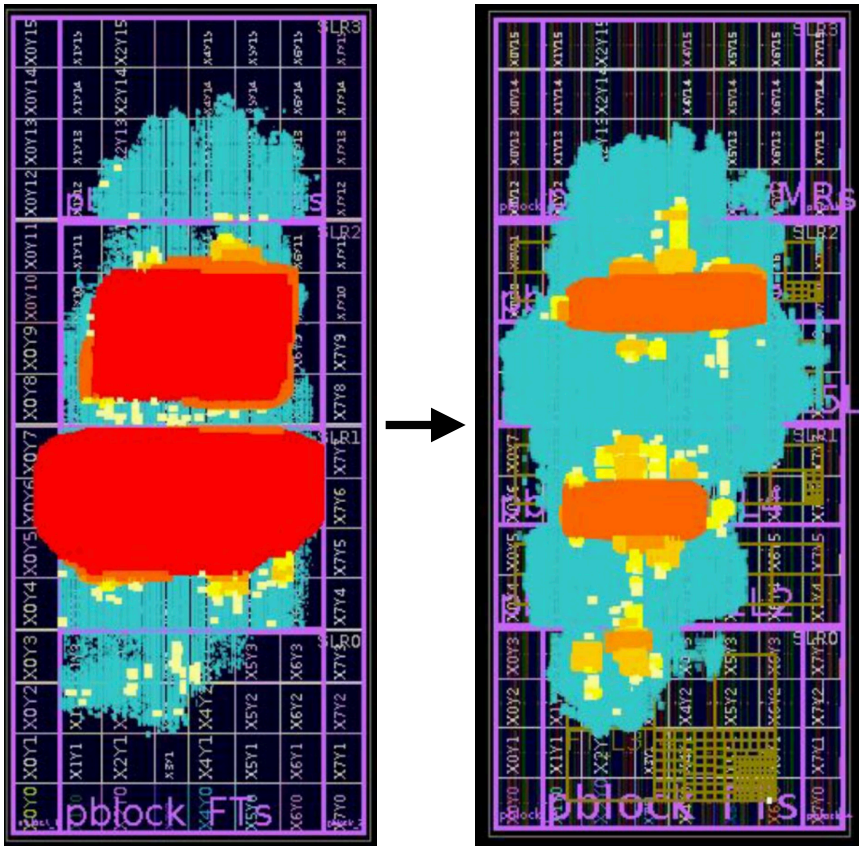




VU13P-2

Need to use floor planning to reduce SLR crossings!

Full Barrel Project Achieved



VU13P-2 VU13P-2

Floor planning reduced SLR crossings:
18503 → 7305

Setup

Worst Negative Slack (WNS):	0.015 ns
Total Negative Slack (TNS):	0.000 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	1095408

- Full barrel project passed timing!
  - Pattern recognization modules only
  - Pipelines, various trials of floor planning and implementation strategy
- Moving on to integrate with Kalman Fitter and test on Apollo rev2

Summary

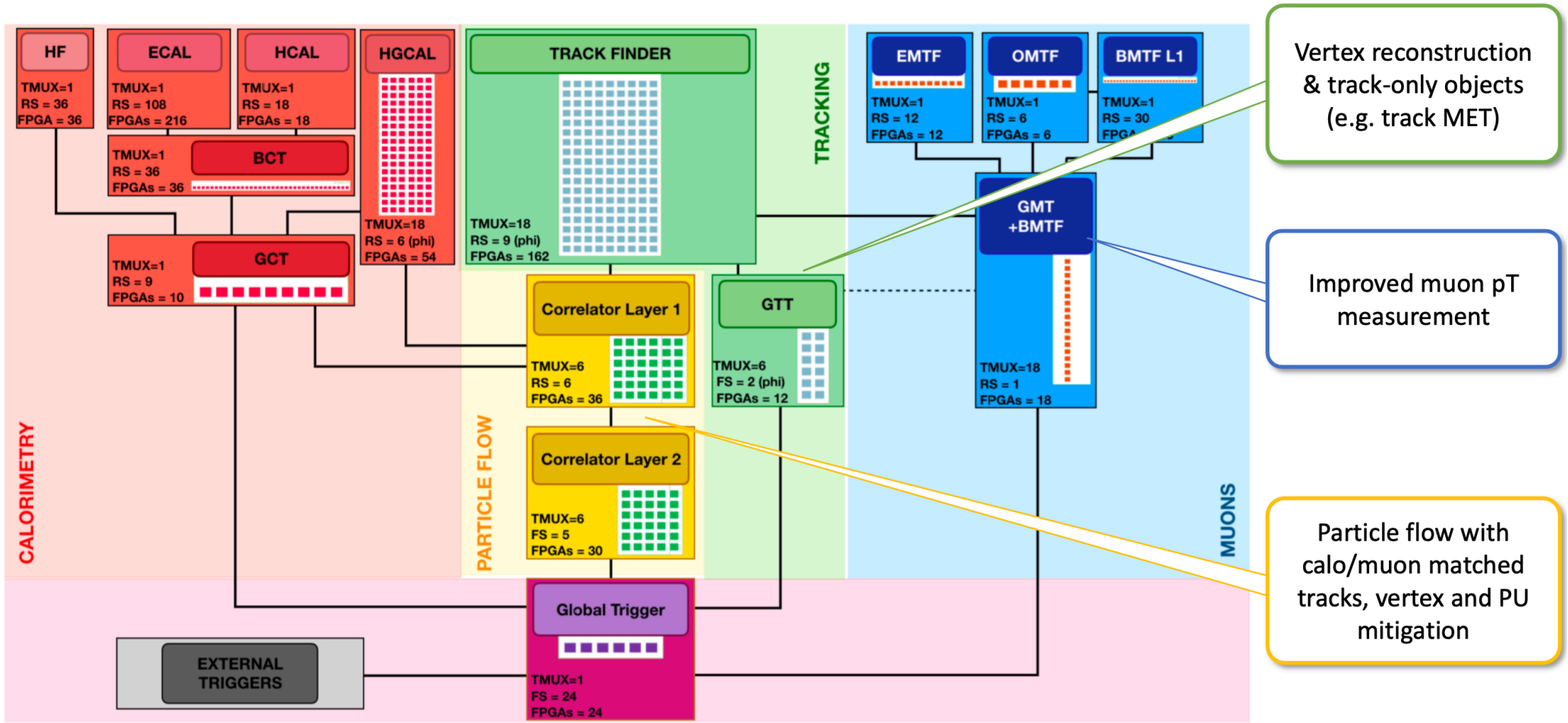
- L1 Track Trigger Upgrade: crucial to achieve physics goals

- Firmware Status:
  - Demonstrated full algorithm chain with narrow coverage on Apollo rev1
  - Full barrel project passed timing requirement
    - Learned a lot about timing optimization strategies
    - Moving on to test on Apollo rev2
  - Aim to demonstrate full detector coverage this year
    - Algorithm to be split between two FPGAs

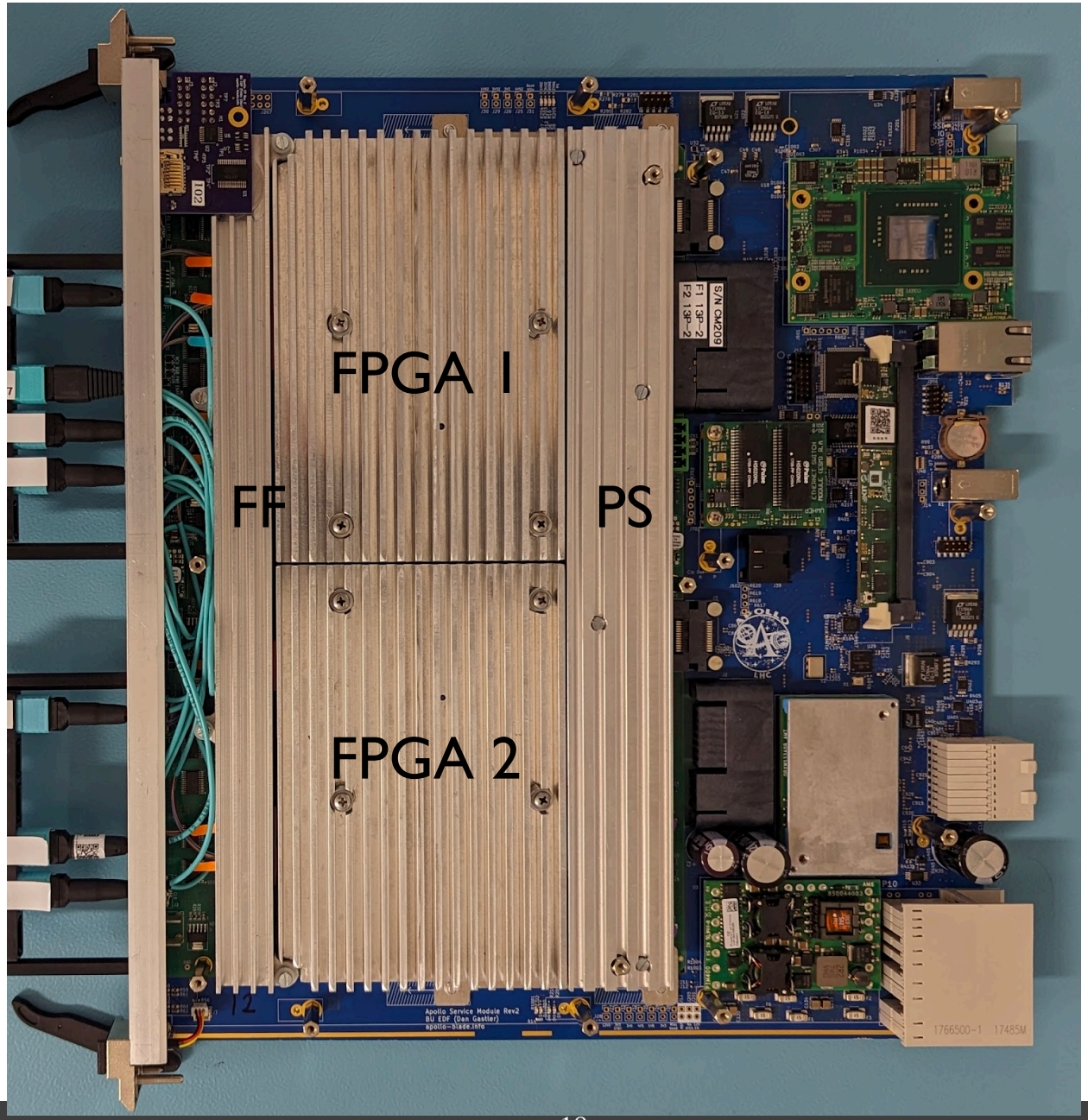
- Hardware Status:
  - Rev2 design fully validated
  - No major design change anticipated in Pilot production
  - Optical engine readiness the biggest uncertainty

Backup

Tracking Usage at L1

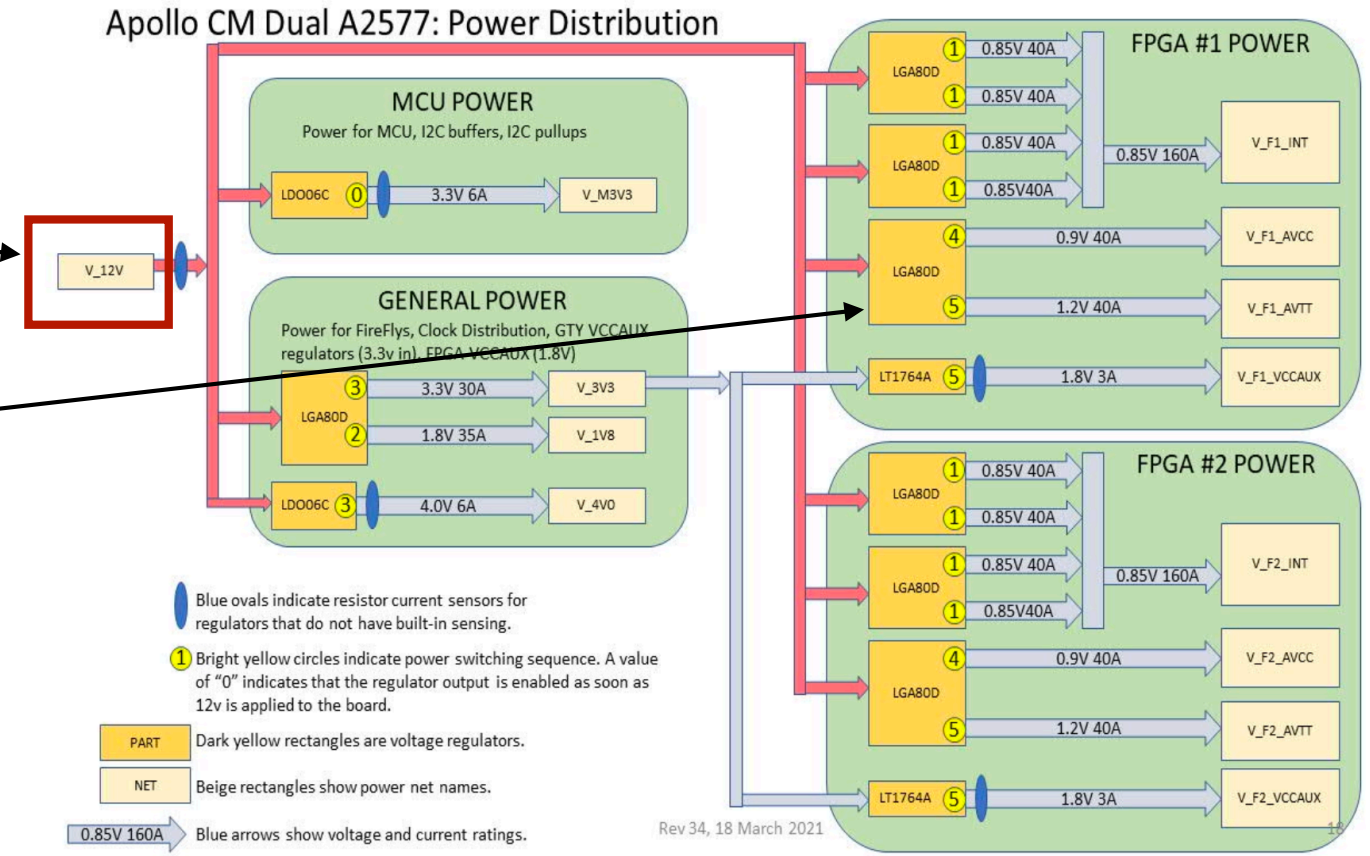


With heatsinks and SM



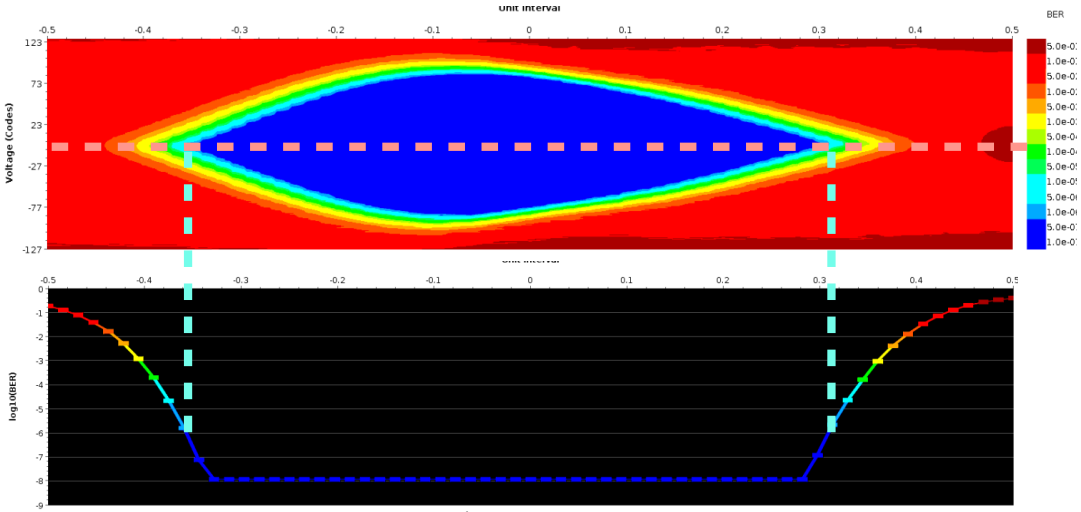
Power Measurement

- Read out current from the 12V
- Read out current from each regulator

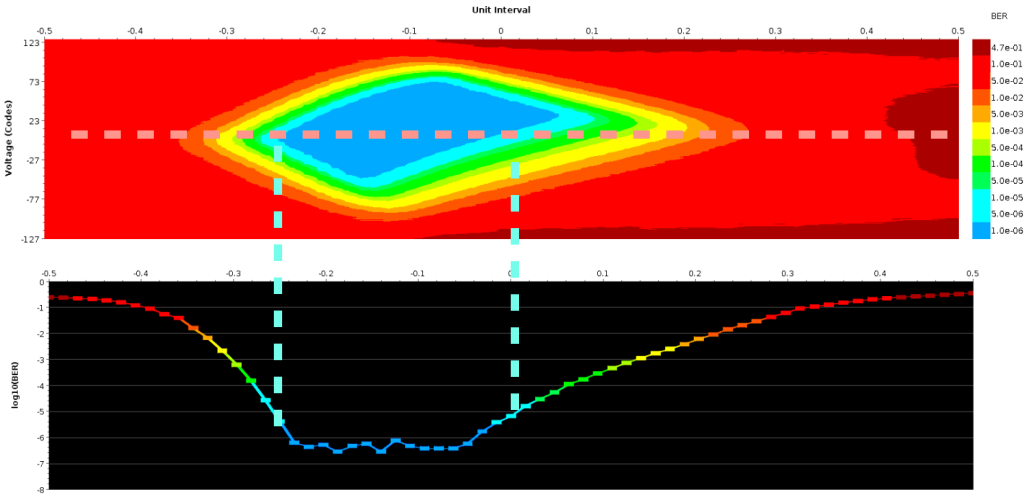


Link Quality Check

- Eye diagrams: 2D scan in Unit Interval (UI) and voltage
  - Qualitative check, takes longer time
- Bathtub curves: 1D scan in UI @ voltage midpoint
  - Extrapolatable
- Both measure jitter probability distribution function (PDF)
  - Deterministic jitter: systematic effects such as crosstalk, duty-cycle-distortion
  - Random jitter: accumulation of random process. Gaussian



Good eye



Bad eye

Link Integrity Tests

- All Firefly links tested @ 25 Gb/s and achieved BER < 10^{-16}
  - Eye diagrams performed to check margins: all big and open
    - Only reflect path between receiver & FPGA due to clock-data recovery

- Evaluated 12 ch 25 Gb/s Firefly prototype-2: satisfactory margin on Apollo rev2

PRBS tests in Vivado GUI

TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Cursor	TX Diff Swing	DFE Enabled
						Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
MGT_X0Y16/TX	MGT_X0Y16/RX	25.781 Gbps	1.083E16	0E0	9.237E-17	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
MGT_X0Y17/TX	MGT_X0Y17/RX	25.766 Gbps	1.083E16	0E0	9.237E-17	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
MGT_X0Y18/TX	MGT_X0Y18/RX	25.782 Gbps	1.083E16	0E0	9.237E-17	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
MGT_X0Y19/TX	MGT_X0Y19/RX	25.781 Gbps	1.083E16	0E0	9.237E-17	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
MGT_X0Y32/TX	MGT_X0Y32/RX	25.781 Gbps	1.083E16	0E0	9.237E-17	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
MGT_X0Y33/TX	MGT_X0Y33/RX	25.781 Gbps	1.083E16	0E0	9.237E-17	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
MGT_X0Y34/TX	MGT_X0Y34/RX	25.781 Gbps	1.083E16	0E0	9.237E-17	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
MGT_X0Y35/TX	MGT_X0Y35/RX	25.781 Gbps	1.083E16	0E0	9.237E-17	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	
MGT_X0Y36/TX	MGT_X0Y36/RX	25.781 Gbps	1.083E16	0E0	9.237E-17	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (00000)	950 mV (11000)	

A Typical Eyescan