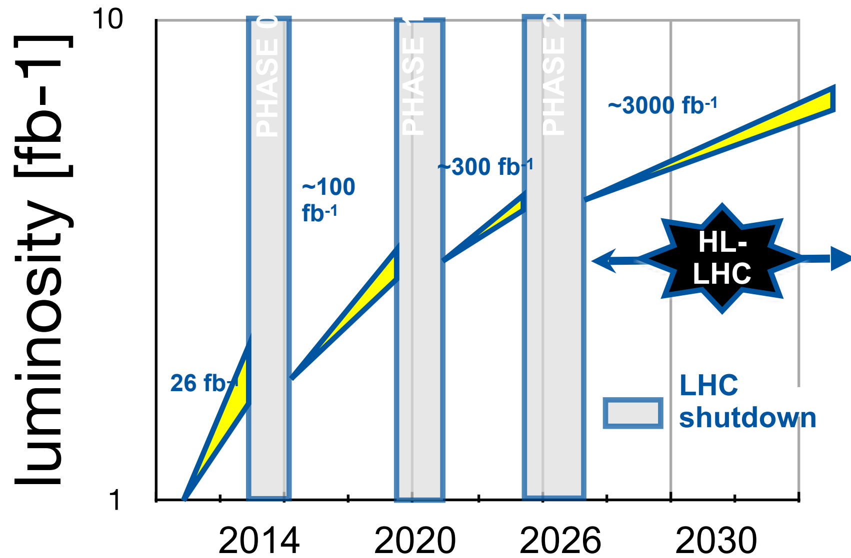
Development of radiation hard pixel detectors

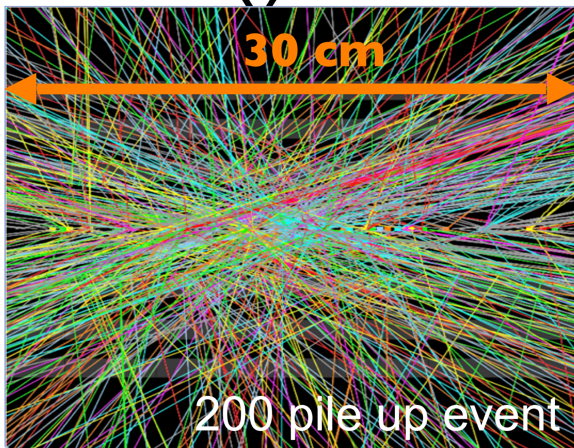
Heinz Pernegger / CERN EP Department

With many thanks to colleagues who kindly provided material
N. Cartiglia, P. Collins, A. Macchiolo, M. Moll, F. Reidt, P. Riedler, C. Solans, W. Snoeys

CERN

High Luminosity - LHC





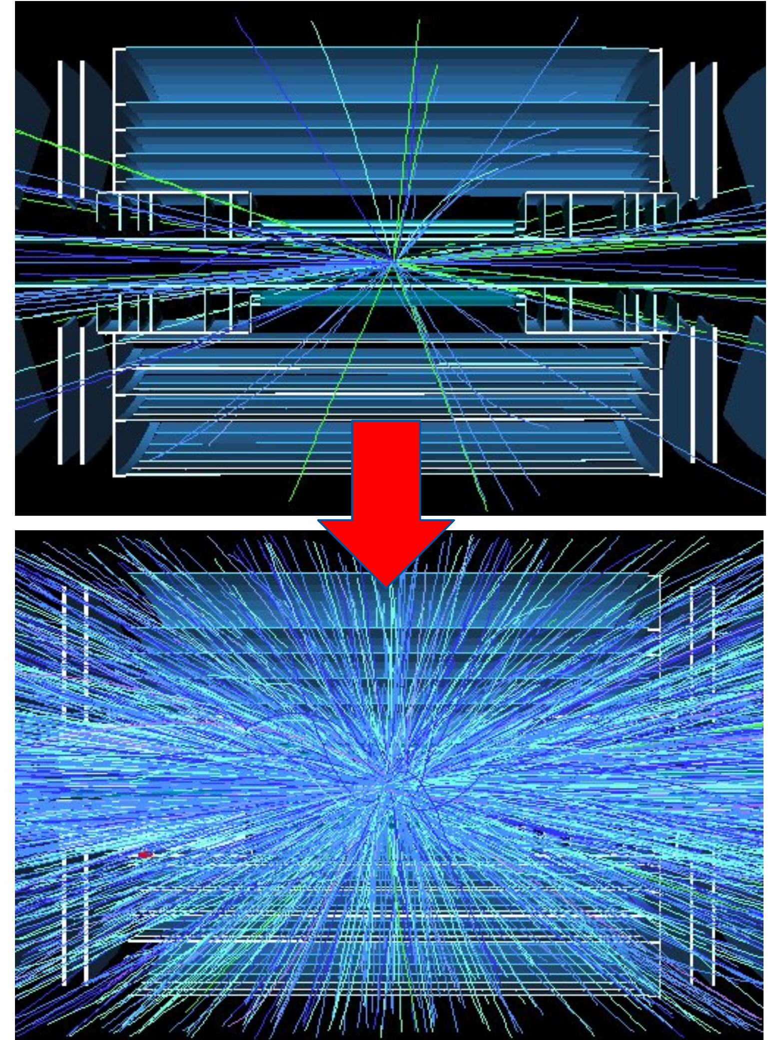
HL-LHC (High Luminosity LHC)

- Collisions to start after Long Shutdown 3 (2025-2027)
- ~4000 fb^{-1} Integrated luminosity to ATLAS/CMS over ten years
- 200 (mean number of) interactions per bunch crossing.
  - Original design for 25 interactions per bunch crossing
- Major upgrades of current silicon trackers for ATLAS & CMS in HL-LHC Phase 2 Upgrade projects as well as ALICE and LHCb in present shutdown

Challenges for the silicon detectors

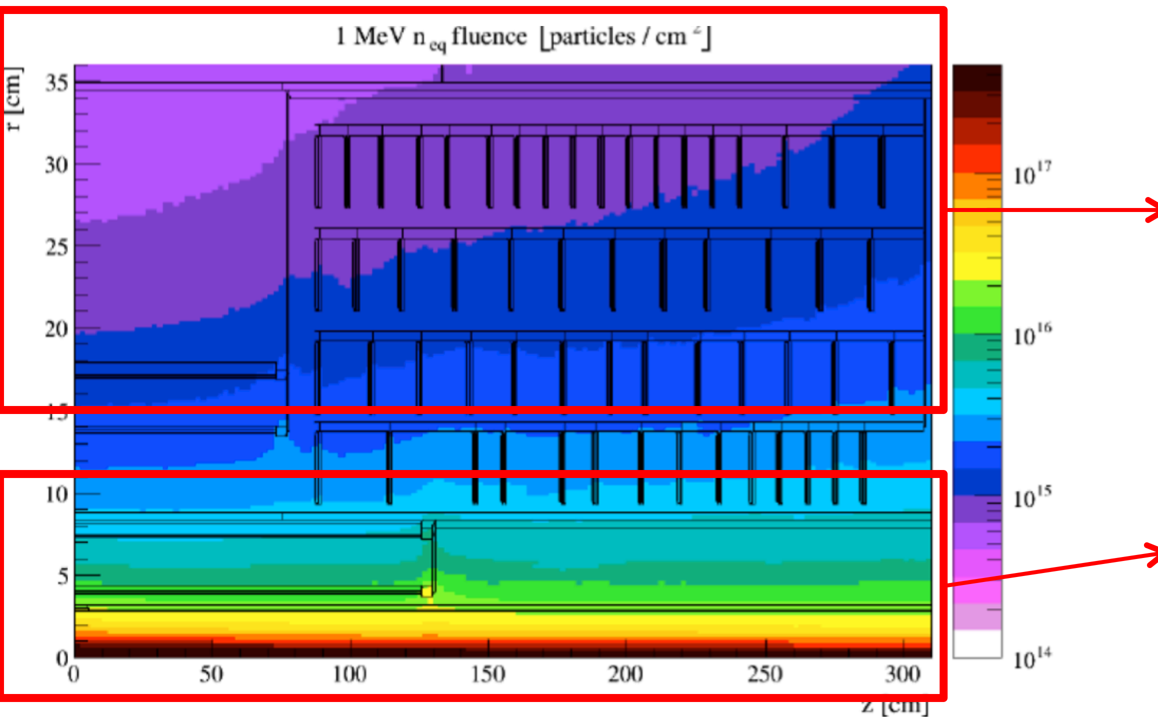
- Increased luminosity requires
  - Higher hit-rate capability
  - Higher segmentation
  - Higher radiation hardness
  - Lighter detectors

- Radiation hardness improvement compared to present trackers
  - factor 10 (HL-LHC) to factor 100 (FCC)



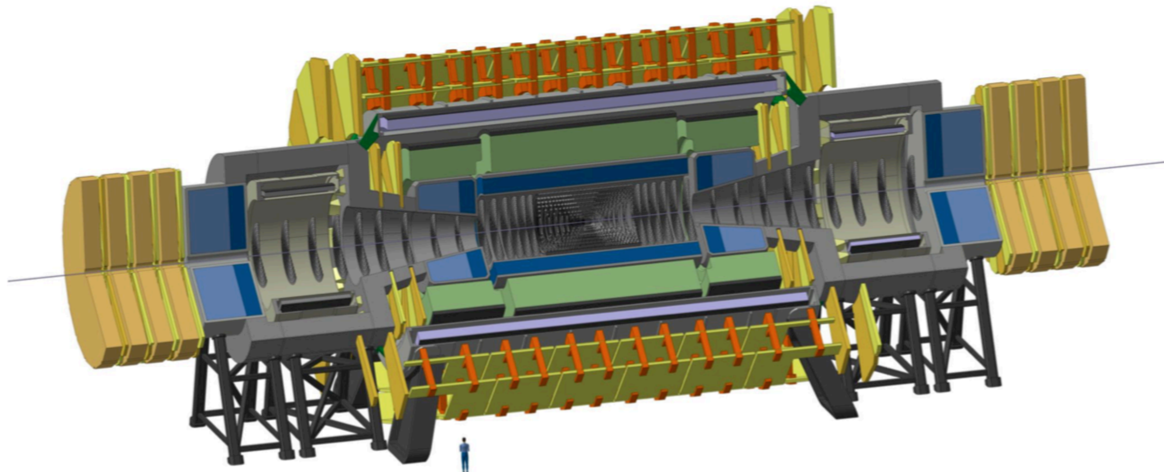
The environment at HL-LHC

- Radiation level, hit rates and bunch structure for silicon detector dominate the development of sensors and Front-end electronics
  - 25ns BC
  - L1 trigger rate (~1MHz)



- Strip layers (r > 30cm)
  - NIEL ~ 10^{14} n_{eq}/cm^2
  - TID ~ 10Mrad
  - Larger area O(100m^2)
- Outer pixel layers (10<r<30cm)
  - NIEL ~ 10^{15} n_{eq}/cm^2
  - TID ~ 50Mrad
  - Larger area O(10m^2)
- Inner layers (r<10)
  - NIEL ~ 5x10^{15} to 10^{16} n_{eq}/cm^2
  - TID ~ 1Grad
  - Smaller area O(1m^2)

Beyond LHC: FCC/hh



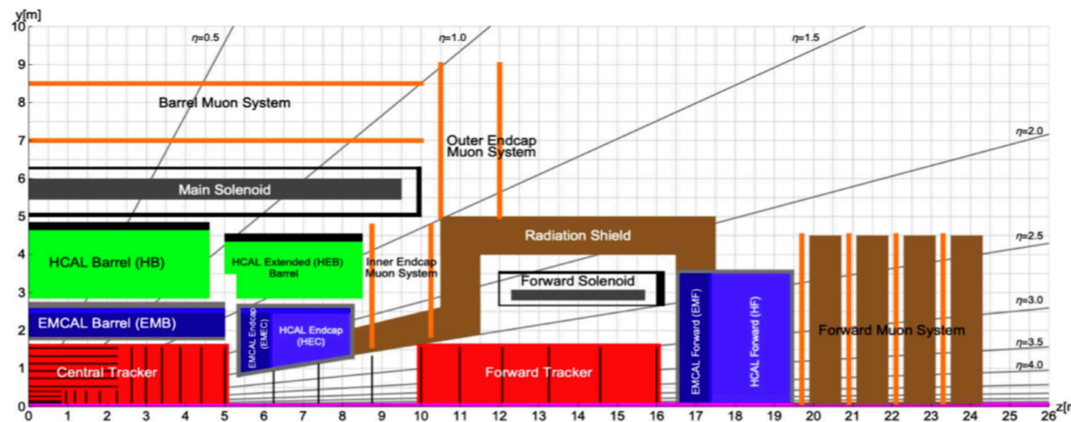
- 4T, 10m solenoid, unshielded
- Forward solenoids, unshielded
- Silicon tracker
- Barrel ECAL LAr
- Barrel HCAL Fe/Scint
- Endcap ECAL/HCAL LAr
- Forward ECAL/HCAL LAr

50 m long, 20 m diameter

‘general’ purpose detector with very large η acceptance and extreme granularity

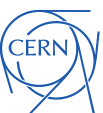
Muon detection up to η = 4 ($\theta \approx 2°$) Calorimetry up to η = 6 ($\theta \approx 0.5°$)

FCC-hh slides, CDR



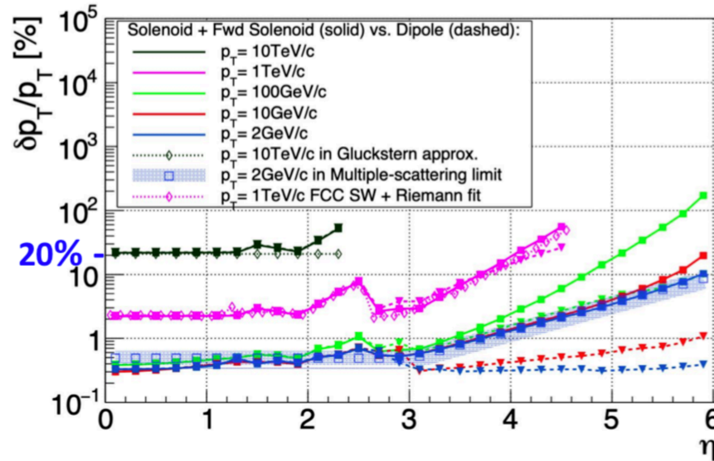
L. Linssen/CERN
Granada 5/2019

Linssen, Granada symposium 2019 5

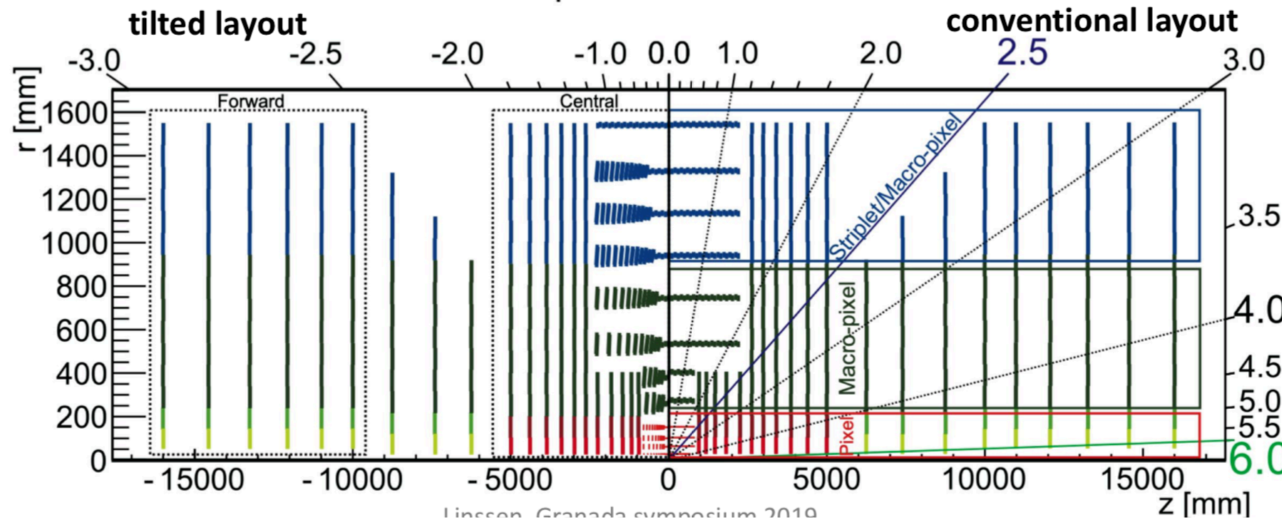


Tracker at FCC/hh

Tracker radius 1.6 m, half-length 16 m, initial baseline hit position resolution 7−9 μm in Rϕ



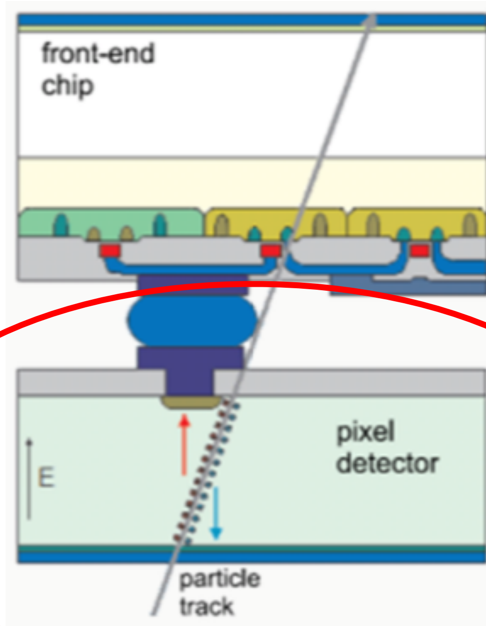
- High occupancies => **small cells sizes** (~25×50 μm^2 in inner layers)
- Two-track separation in boosted objects
  - **small cell sizes** + **better hit resolution** <5 μm
- **Tilted layout** to minimize multiple scattering
- High-E => **significant fraction of displaced vertices outside acceptance**
- **Radiation ×100 higher than present technologies**



FCC-hh slides, CDR

L. Linssen/CERN
Granada 5/2019

Hybrid pixel sensors



Special sensor for e.g. extreme radiation hardness, timing

Dedicated FE-chip eg. for very high hit rates, digital functionality (memory, TDC,…)

- Front-end chip
  - Depending on application we need specialized FE-ASIC
  - Complexity of designs are driven by experimental needs
  - Increasing functionality on chip drives the development towards 65nm and smaller node size CMOS processes
- Sensor developments
  - For very high radiation and track density (e.g. 3D sensors, active edge planar)
  - Sensors for 4D tracking, i.e. spatial and time information (e.g. pixel sensors with trench electrodes)

Future Trackers at ATLAS and CMS

Sensor active thickness 100 - 300 μm

CERN-LHCC-2017-021 ; ATLAS-TDR-030

Technical Design Report for the ATLAS Inner Tracker Pixel Detector

Einsweiler, Kevin; Pontecorvo, Ludovico

Collaboration, ATLAS

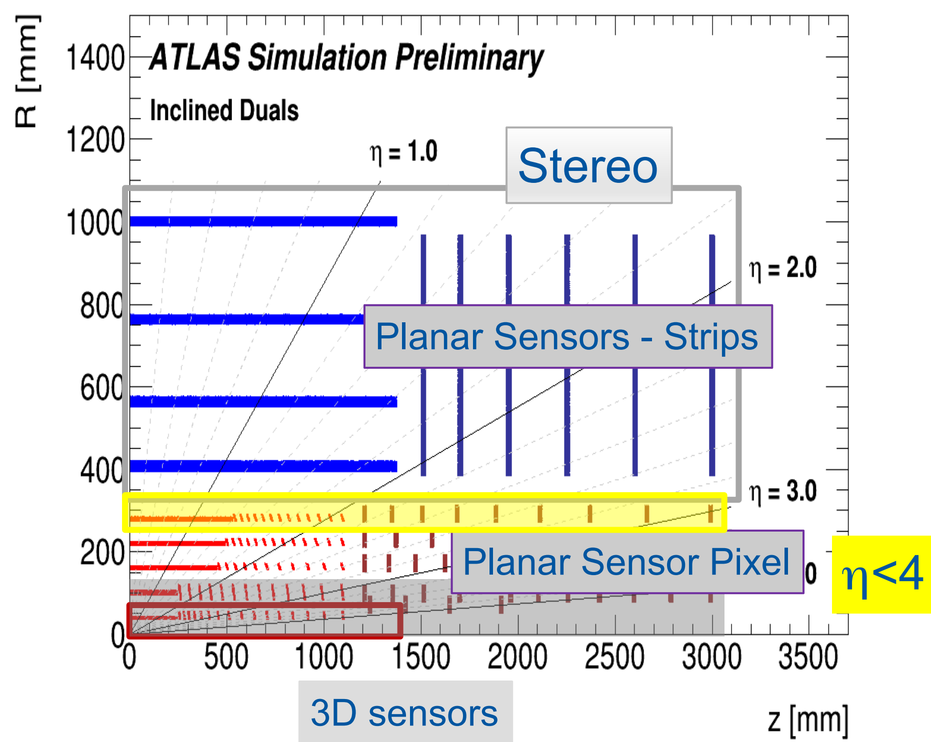
CERN. Geneva. The LHC experiments Committee ; LHCC

(technical design report)

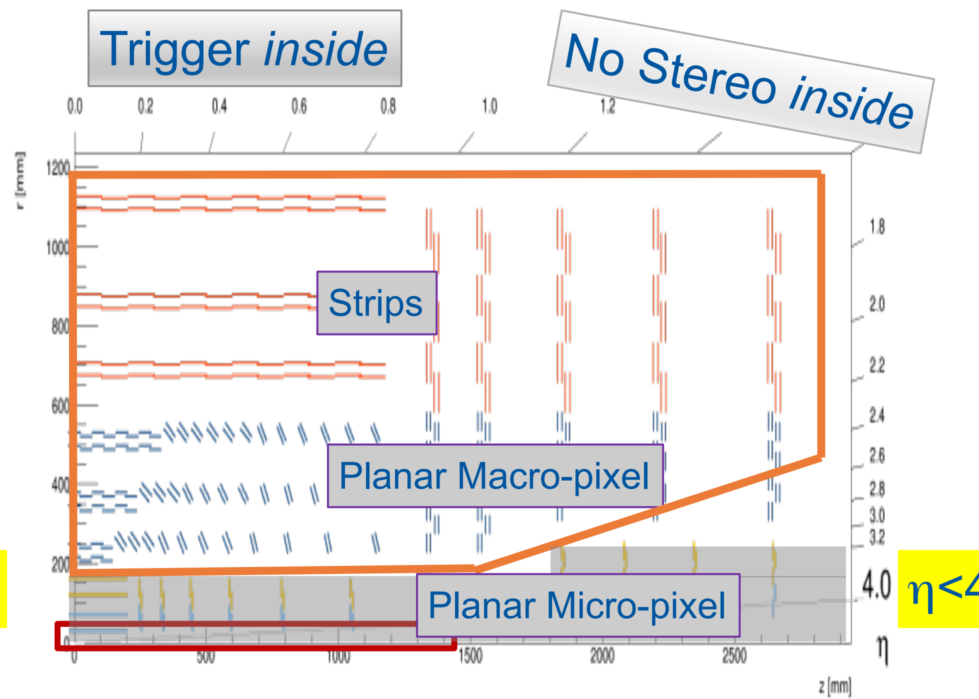
k_einsweiler@lbl.gov on 23 Sep 2017

Detectors and Experimental Techniques

This is a placeholder for the final document.

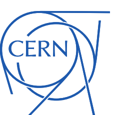


η<4



F. Hartmann HST 2018

All n-in-p sensors *inside* with different thicknesses



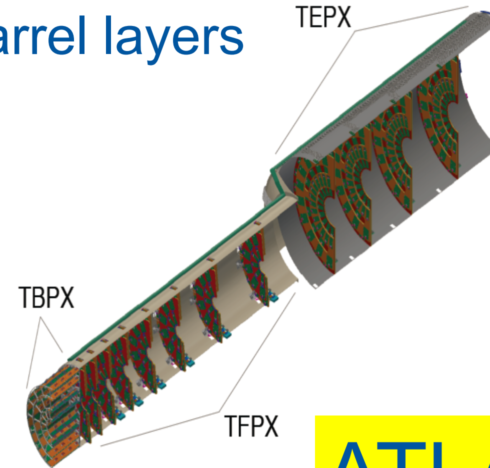
Next generation Pixel Detectors

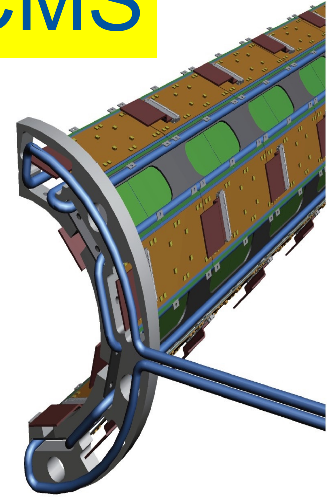
CMS

Many commonalities ATLAS – CMS lead to RD53 Developments

- “Classical” hybrid pixel detectors with bump-bonding
  - **THIN** Planar n-on-p or 3D detectors (inner layers)
  - Common R&D on chip **RD53**A– 65nm TSMC
  - Modules: Single to Quads chip arrangments
- Common design of pixel FE-IC implemented with different matrix size and FE design (TSMC 65nm)
  - Sensor 50 x 50 µm pitch
  - Sensor 25x100 µm pitch
- Serial Powering (part of **RD53**)
- Both detectors up to η=4
- **Surface: 2*CMS < 1*ATLAS**

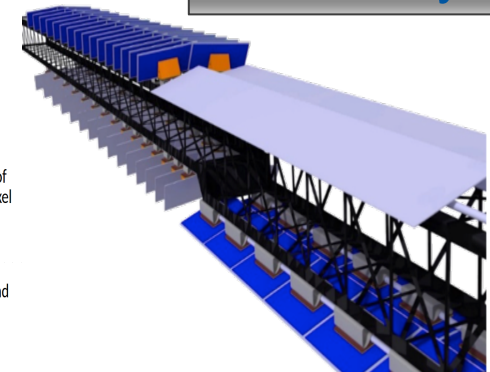
4 barrel layers



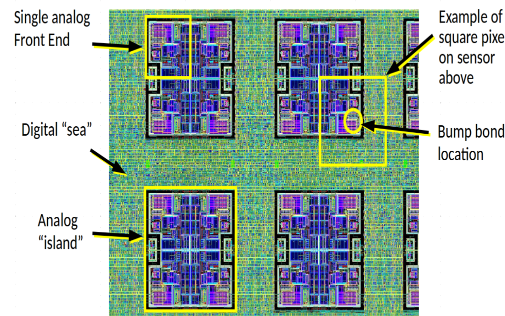


ATLAS

5 barrel layers



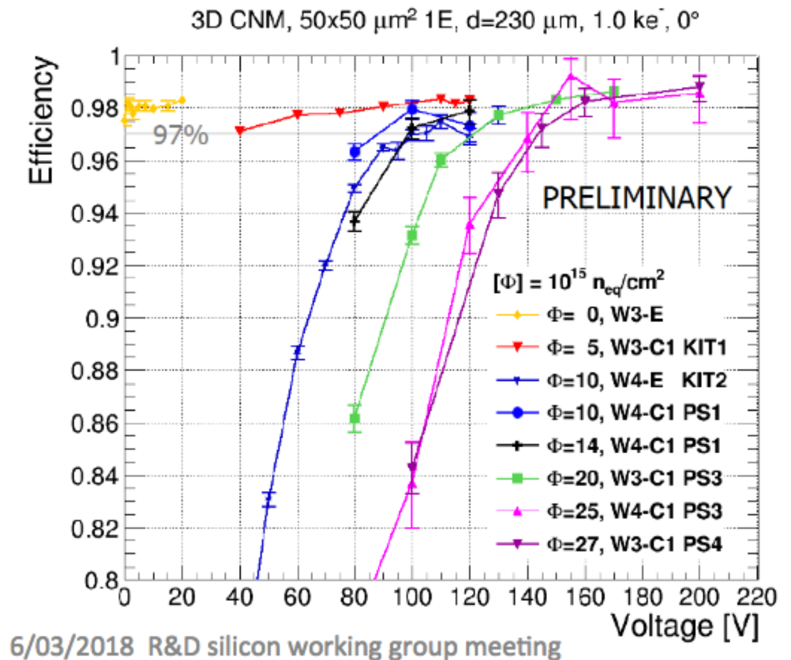
RD53



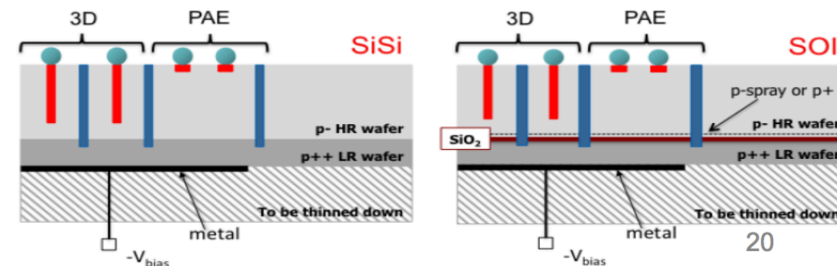
Sensors for hybrid detectors ATLAS/CMS

- 3D and Planar sensors developed to radiation hardness of $>10^{16}\ n_{eq}/cm^2$ for HL-LHC on 4”, 6”, 8” wafer
  - Further development focuses on
  - Better lithography for smaller pixels on 3D
  - Optimizing active edge on planar
  - Move to 8” wafers

ATLAS ITk 3D



6” wafers at FBK



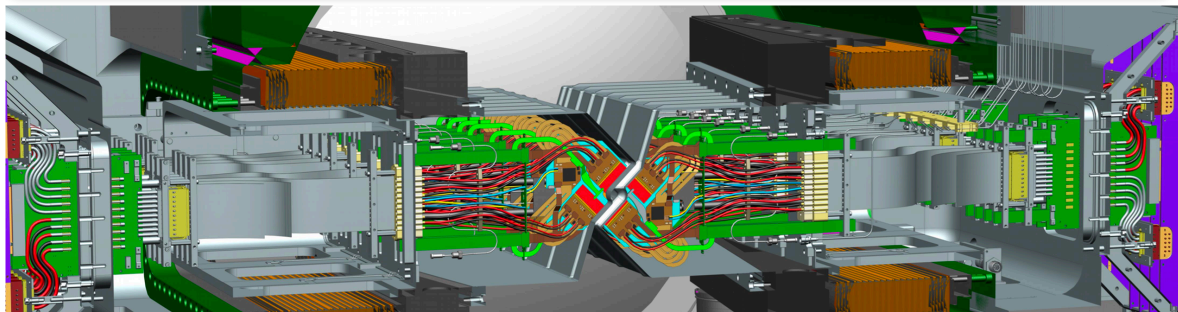
PixelVelo and Upstream Tracker for LHCb in LS2

Maintain Physics Performance in very high occupancy and pile up conditions
combinatorial complexity and fake tracks
Pile-up mitigated by **granularity, high readout speed** and **trigger** innovations (**timing** will be for Upgrade II)

Operate with detector elements exposed to very high radiation doses
Radiation hardness needed for all subdetectors

Cope with tremendous DAQ and data processing challenges

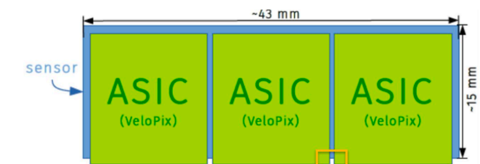
PixelVelo Stations assembled

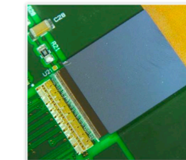


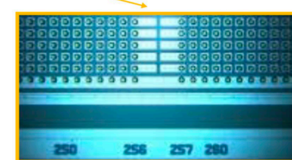
VeloPix for LHCb Upgrade 1

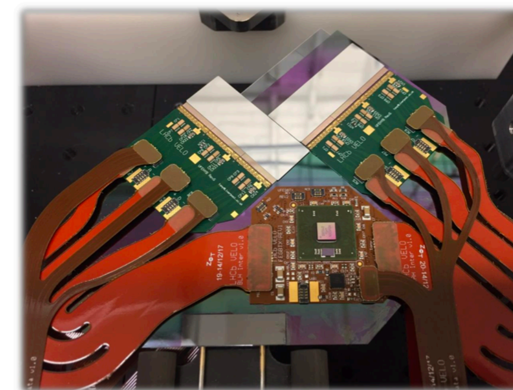
Derived from Timepix3 and dedicated to LHCb.

	Timepix3 (2013)	VeloPix (2016)
Pixel arrangement	256 x 256	
Pixel size	55 x 55 μm²	
Peak hit rate	80 Mhits/s/ASIC	800 Mhits/s/ASIC 50 khits/s/pixel
Readout type	Continuous, trigger-less, TOT	Continuous, trigger-less, binary
Timing resolution/ range	1.5625 ns, 18 bits	25 ns, 9 bits
Total Power consumption	<1.5 W	< 3 W
Radiation hardness		400 Mrad, SEU tolerant
Sensor type	Various, e- and h+ collection	Planar silicon, e- collection
Max. data rate	5.12 Gbps	20.48 Gbps
Technology	IBM 130 nm CMOS	TSMC 130 nm CMOS









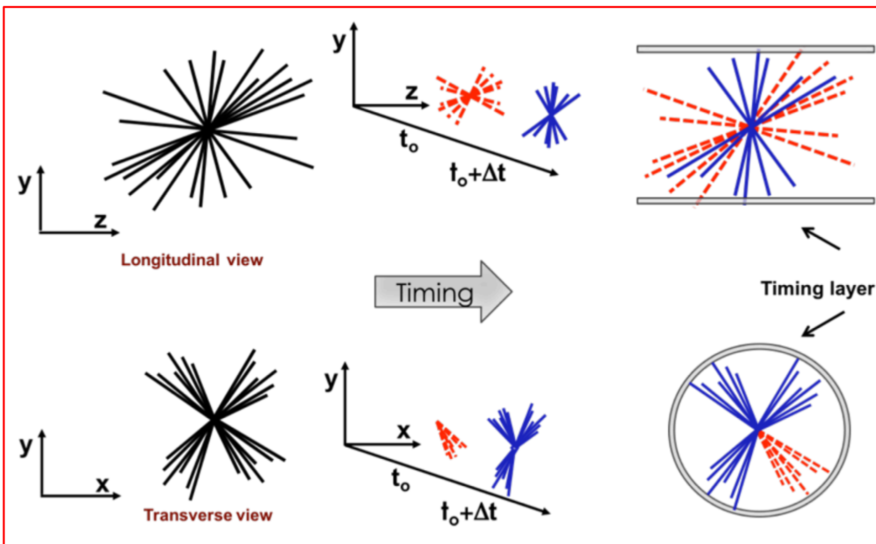
P. Collins CERN / LHCb Upgrade 1

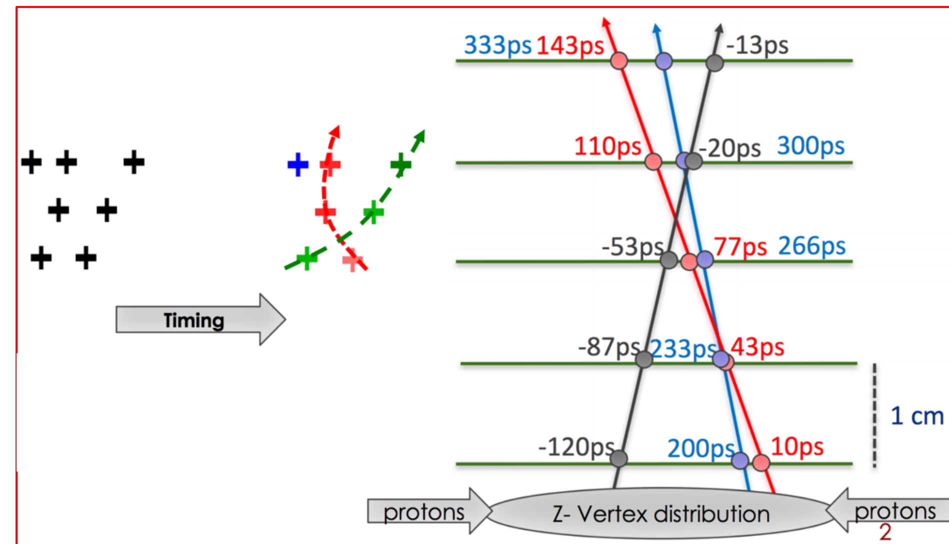
Timing for tracking

Need sub-nanosecond track time to suppress background in environments with large pile-up (HL-LHC, FCC) → **4D tracking**

Separate timing layers with coarser granularity
→ timing for reconstructed tracks
(e.g. HL-LHC upgrades **~30 ps**)

Timing within pixel layers
→ time info for pat rec
(e.g. LHCb Upgrade II **20-200 ps,** depending on pixel size, radiation)

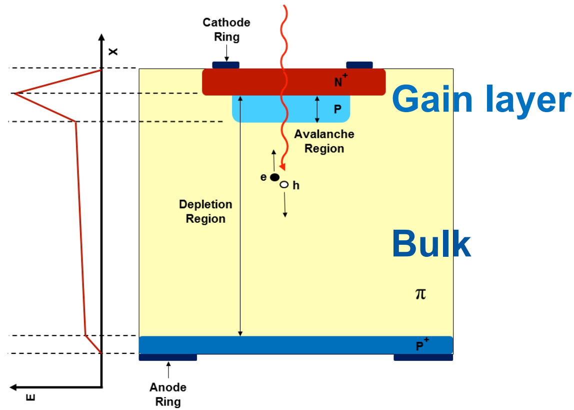




N. Cartiglia / INFN Torino

→ Trade-off between time resolution and pixel size / layer thickness
→ FCChh needs track timing at **5 ps** up to **$6x10^{17}$ n_{eq}/cm^2** fluences

LGAD timing sensors

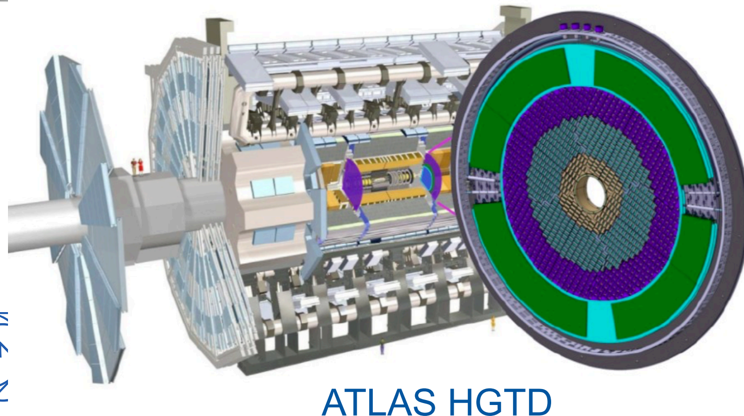


A vertex detector in time domain at 3 m from the interaction point

BTL: L(Y)SO bars + SiPM readout:
- TK/ ECAL interface ~ 45 mm thick
- $|\eta|<1.45$ and $p_T>0.7$ GeV
- Active area ~38 m^2 ; 332k channels
- Fluence at 3 ab^{-1}: 2×10^{14} n_{eq}/cm^2

ETL: Si with internal gain (LGAD):
- On the HGC nose ~ 65 mm thick
- $1.6<|\eta|<3.0$
- Active area ~14 m^2; ~8.5M channels
- Fluence at 3 ab^{-1}: up to 2×10^{15} n_{eq}/cm^2

CMS MIP Timing Layer



ATLAS HGTD

Low Gain Avalanche Detectors (LGAD):

Multiplication of charges (~10-100x) in thin gain layer → fast rise time, increased S/N

- Strong development through RD50 collaboration and ATLAS HGTD/CMS timing layer projects
- Several vendors: CNM, FBK, HPK
- Reached **~30 ps** for few mm^2 size sensors → used for HL-ATLAS & CMS **timing layers**
- Limiting factors for time resolution:
  - Weighting **field uniformity** → favors larger pixels
  - **Radiation effects** → ok up to ~10^{15}, mitigation measures under study for higher fluences
  - **r/o electronics + clock distribution** → IC work package
- R&D to achieve radiation hardness
  - Variation in doping to limit gain loss after irradiation
- RD for **larger fill factors** (minimal gap between electrodes) and concepts for sensors without gap

LGAD: Gain layer engineering

Defect Engineering of the gain layer

- **Carbon** co-implantation mitigates the gain loss after irradiation
- Replacing Boron by **Gallium** did not improve the radiation hardness

Modification of the gain layer profile

- Narrower **Boron doping profiles** with high concentration peak (Low Thermal Diffusion) are less prone to be inactivated
- Deep Gain Layer improves electric field after acceptor removal (see N. Cartiglia, Hiroshima 2019 HST12)

Gain layer fraction
1.2
1
0.8
0.6
0.4
0.2
0
1.0E+13
1.0E+14
1.0E+15
1.0E+16
Fluence n_eq/cm2
W6 B+C - <CV>
W15 Ga+C <CV>
W1 LD <CV>
W8 B <CV>
W14 Ga <CV>
Boron + Carbon
Gallium + Carbon
Boron (Low Diff)
Boron (High Diff)
Gallium

Boron profile
Doping Concenration (a.u.)
Silicon Depth (a.u.)
LOW DIFF.
x2 Peak conc.
FWHM = 0.7
HIGH DIFF.
FWHM = 1

RD50 Status Report 2019 - M.Moll - G.Casse and Vertex 2020 workshop

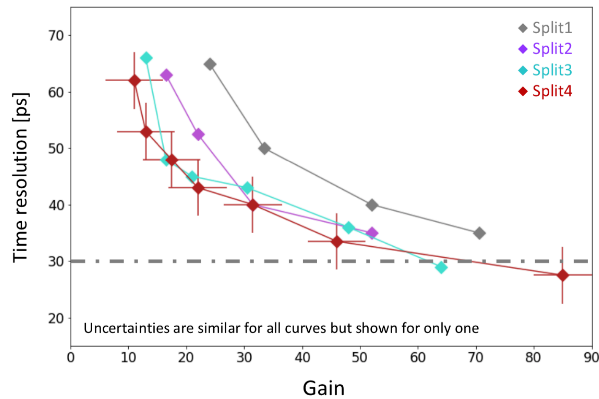
[G.Paternoster, FBK, Trento, Feb.2019]

CMS and ATLAS timing layers

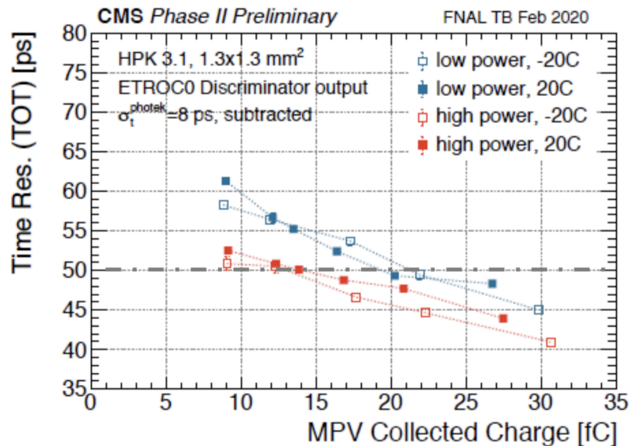
- Dedicated FE-chips bump-bonded to LGAD sensors

V Sola – presentation Vertex 2020

Sensor Lab measurement



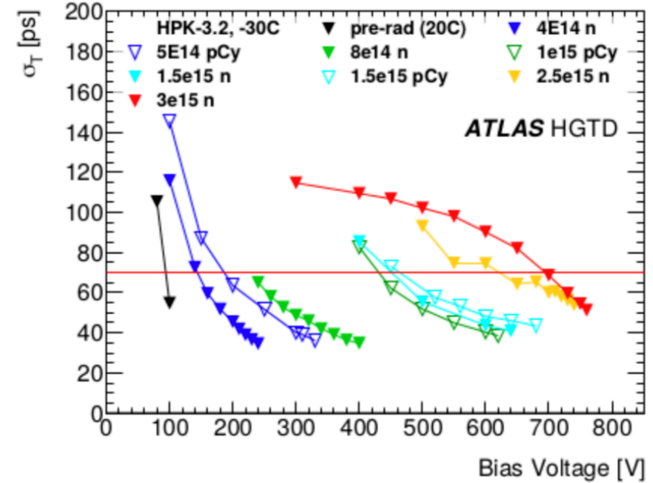
ETROC0 Module in TB



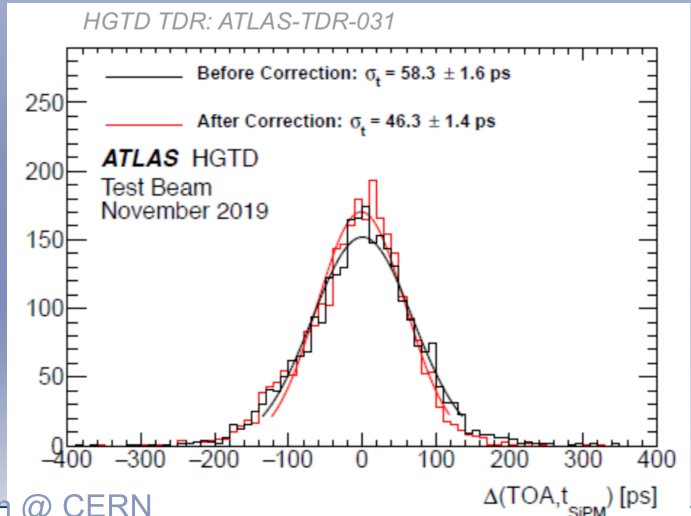
CMS MIP Timing Layer

ATLAS HGTD

Sensor Lab measurement



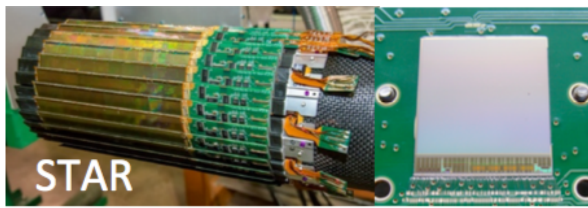
ALTIROC1 Module in TB



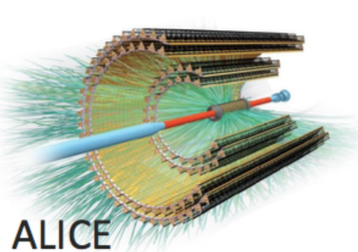
ATLAS HGTD TDR-031

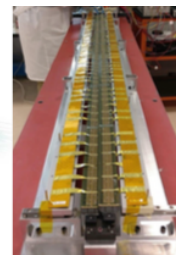
Monolithic Pixel Sensors for Future Trackers

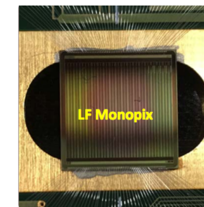
	RHIC STAR	LHC - ALICE ITS	CLIC	HL-LHC Outer Pixel	HL-LHC Inner Pixel	FCC pp
NIEL [n_{eq}/cm^2]	10^{12}	10^{13}	$<10^{12}$	10^{15}	10^{16}	10^{15}-10^{17}
TID	0.2Mrad	<3Mrad	<1Mrad	80 Mrad	2x500Mrad	>1Grad
Hit rate [MHz/cm²]	0.4	10	<0.3	100-200	2000	200-20000

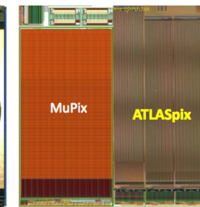


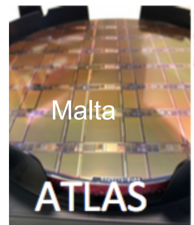
Ultimate Sensor




Alpide Sensor







Monopix & AtlasPix & Malta Sensor

- Advances in commercial CMOS technologies combined with dedicated designs allowed significant progress S in areas like radiation hardness, response time, hit rates
- **Strong interest for R&D to fully exploit potential of MAPS in future Trackers**
  - **High granularity, Low material budget and power, Large area at reduced cost (cf hybrid)**
  - **CMOS foundries offer substantial processing power to enable significant performance gains**

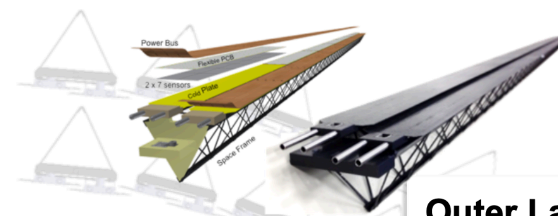
ALICE Inner Tracking System Upgrade at LHC

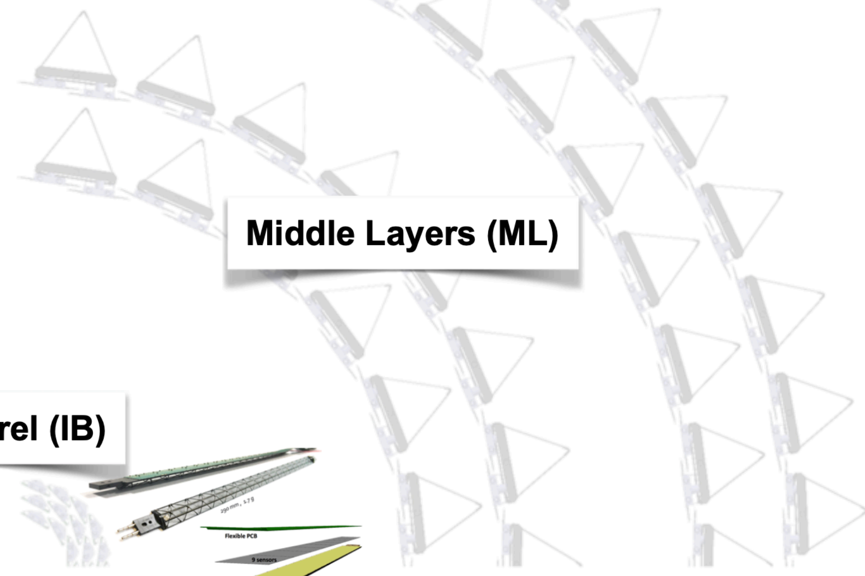
A Large Ion Collider Experiment

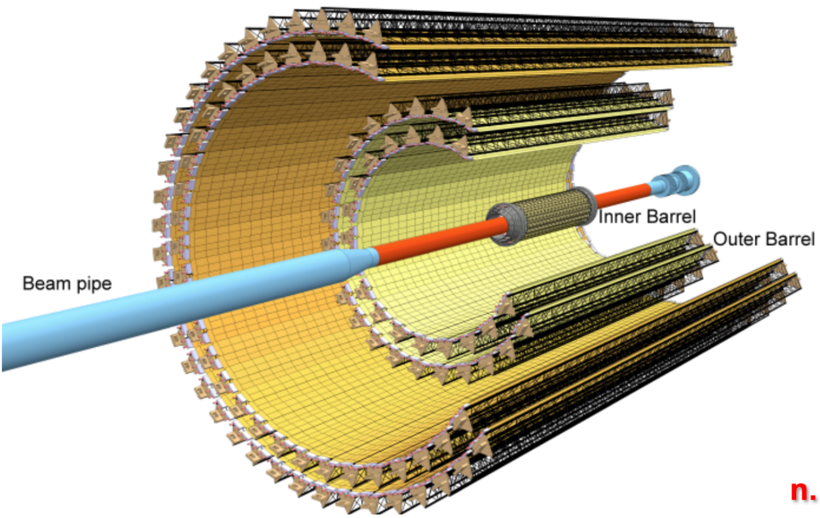
ITS2 Layout

- 7 layers (inner/middle/outer): 3/2/2 from R = 22 mm to R = 400 mm
- 192 staves (IL/ML/OL): 48/54/90
- Ultra-lightweight support structure and cooling

10 m² active silicon area, 12.5×10⁹ pixels



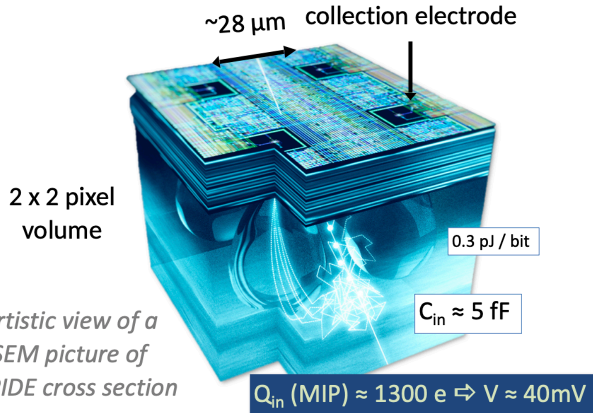


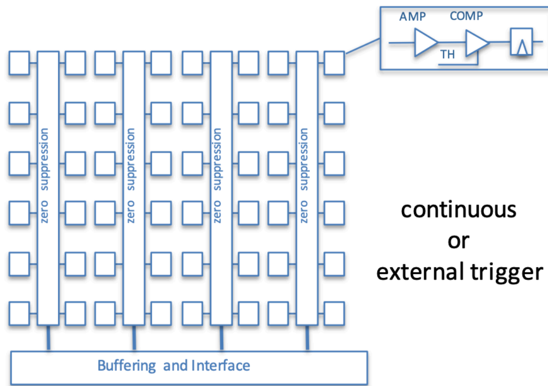


F. Reidt / CERN EP - Vertex 2021

MAPS for ALICE ITS2 : ALPIDE sensor

Pixel chip characteristics





- Based on the **ALPIDE Monolithic Active Pixel Sensor**
  - In-pixel amplification, shaping, discrimination and Multiple-Event Buffers (MEB)
  - In-matrix data sparsification
  - High detection efficiency: > 99% and low fake-hit rate: << 10^{-6}/pixel/event
  - Radiation tolerant: > 270 krad Total Ionising Dose (TID), > 1.7×10^{12} 1 MeV/n_{eq} Non-Ionising Energy Loss (NIEL)
  - Low power: < 40mW / cm^2

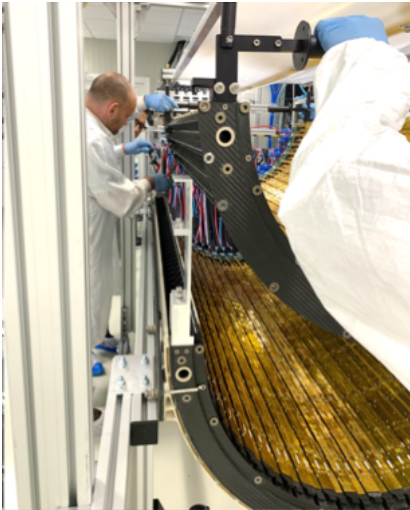
	Previous ITS	New ITS2
Distance to IP (mm)	39	22
X_0 (innermost layer) (%)	~ 1.14	~ 0.35
Pixel pitch (μm^2)	50 x 425	27 x 29
Readout rate (kHz)	1	100
Spatial resolution ($r\varphi$ x z) (μm^2)	11 x 100	5 x 5

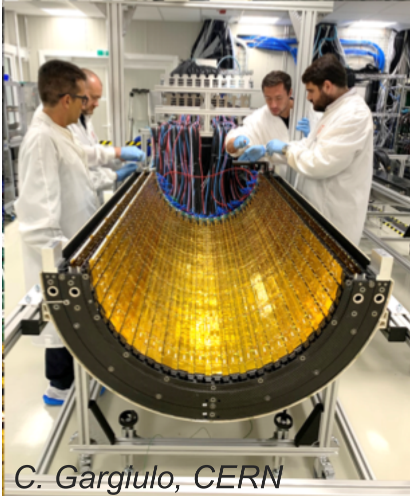
Improved resolution, less material, faster readout

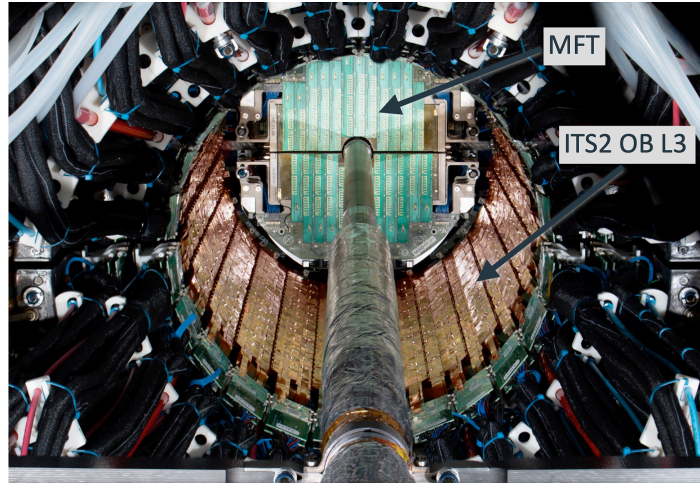
F. Reidt / CERN EP - Vertex 2021

ALICE ITS Layer Assembly

ALICE

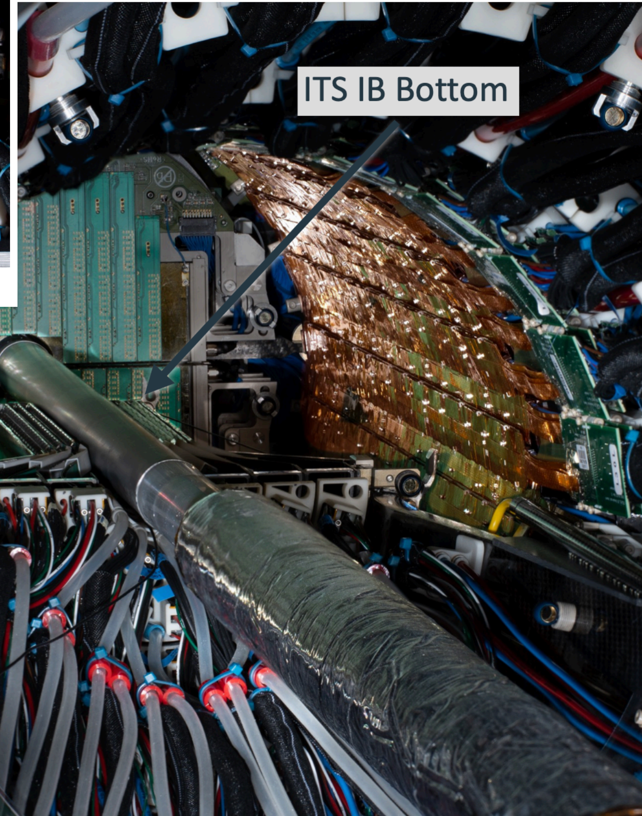






ITS Outer Barrel surrounding the beam pipe, MFT in the back

ITS2 assembled and installed in ALICE experiment

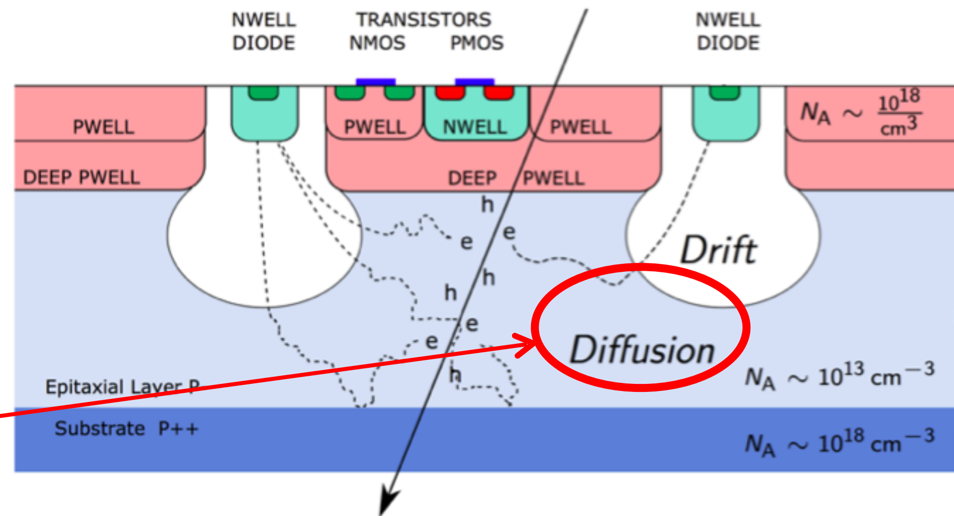


ITS Inner Barrel Bottom and Outer Barrel

F. Reidt / CERN EP - Vertex 2021

Towards radiation hard MAPS…

…there are several obstacles to overcome:



Depletion is key:

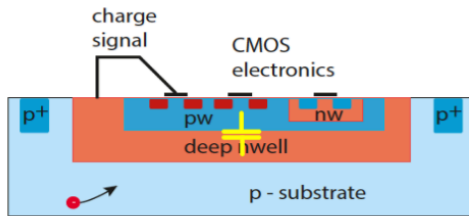
- At high radiation levels (>10^{16} n_{eq}/cm^2) the ionization charge is trapped in the non-depleted part
- Diffusion makes signal collection slower than typical requirements for pp-colliders

Readout architectures are low power but not designed for high hit-rates of pp experiments at LHC or future pp colliders

Different CMOS sensor designs

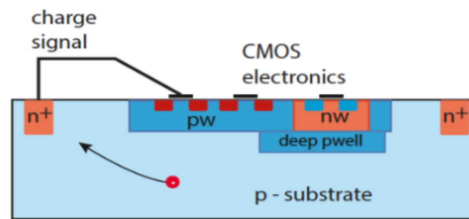
- Purse different design approaches for optimal performance

Large electrodes



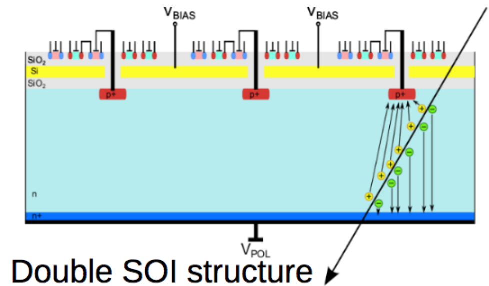
- Electronics in collection well
- No or little low field regions
- Short drift path for high radiation hardness
- Large(r) sensor capacitance (dpw/dnw) ->higher noise and slower @ given pwr
- Potential cross talk between digital and analog section

Small electrodes



- Electronics outside collection well
- Small capacitance for high SNR and fast signals
- Separate analog and digital electronics
- Large drift path -> need process modification to usual CMOS processes for radiation hardness

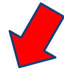
"Burried" electrodes (SOI)

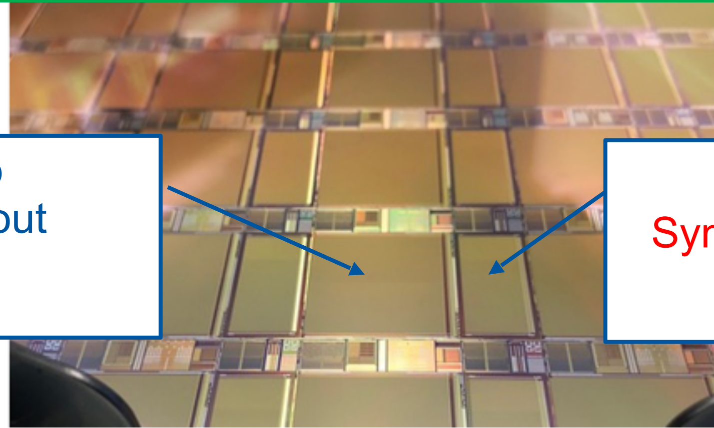


- Electronics and sensor in separate layer
- Can use thick or thin high resistivity material and HV (>200V)
- Special design/ processing to overcome radiation induced charge up of oxides

MALTA & TJ MonoPix – Novel depleted CMOS sensors with small electrodes

Design of two large scale demonstrators to match
ATLAS specifications for outer pixel layers





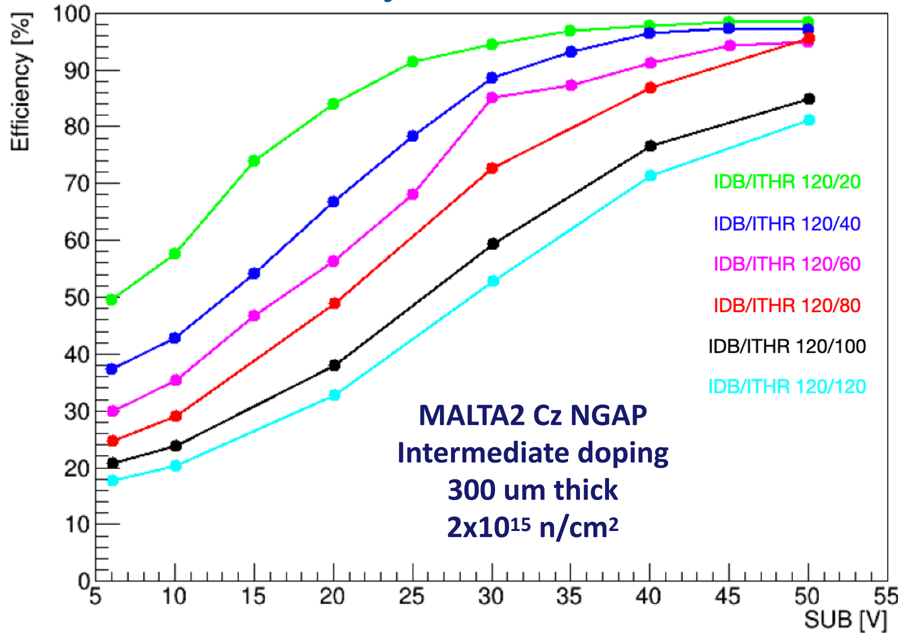
The "MALTA" chip
Asynchronous readout architecture

The "TJ-Monopix" chip
Synchronous readout architecture.

- **Produced in Tower 180nm imaging process ~ 36um pixel pitch**
- **The ATLAS "MALTA" and "MonoPix" chips** for **high hit rate suitable for HL-LHC pp-collisions**
  - **Radiation hard to >10^{15} n/cm^2 & Shaping time 25ns** (BC = 25ns)
  - **MALTA: Asynchronous readout** architecture for high hit rates and fast signal response, 36um pitch 512x512 matrix, ~2x2 cm2
  - **MonoPix: Synchronous Column drain** readout architecture, 33um pitch

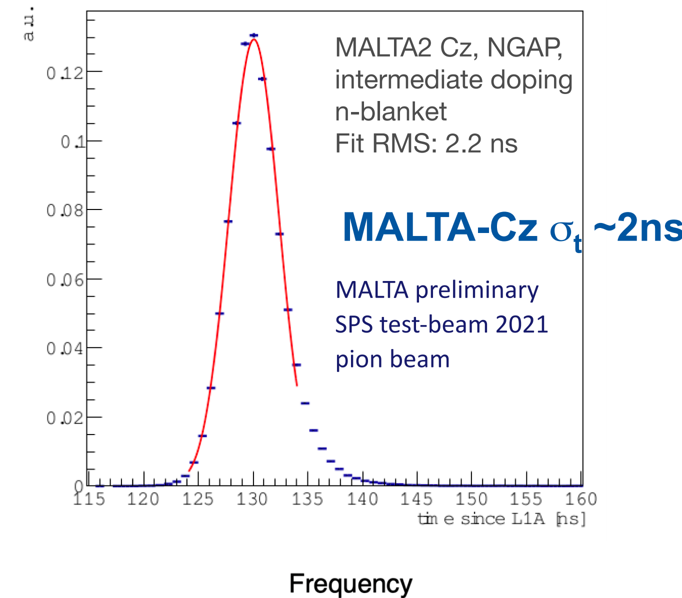
MALTA 2 Sensor

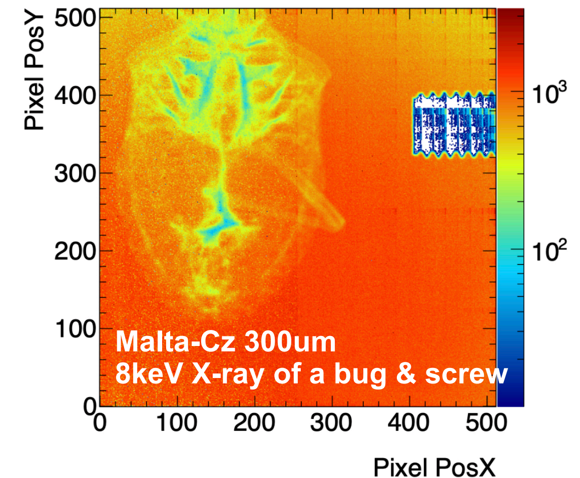
MIP Efficiency



C. Solans / CERN EP

Time resolution

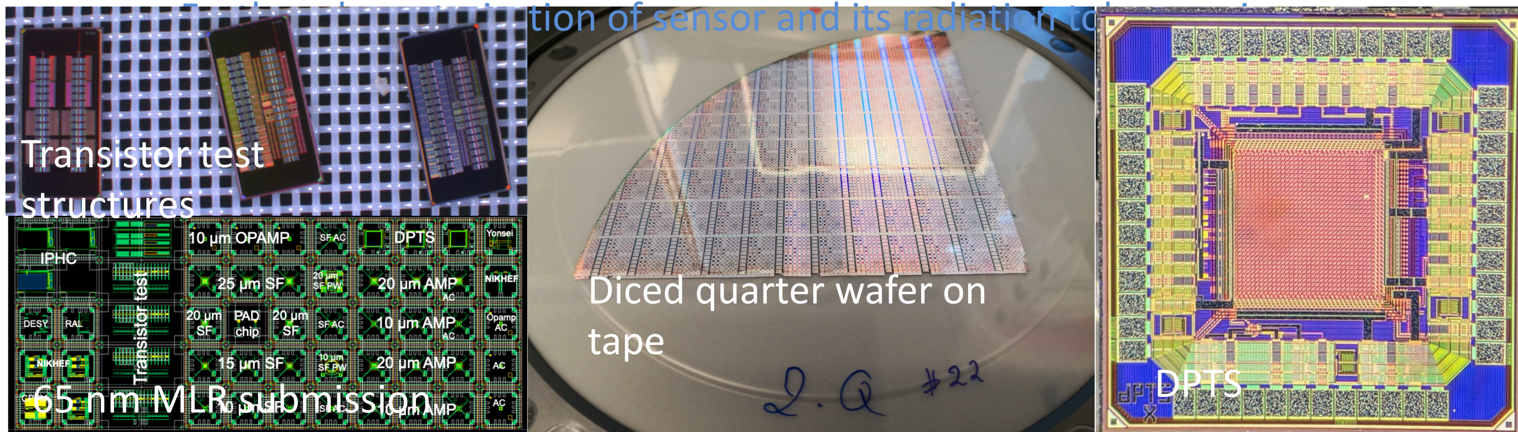




- Produced on 25um epitaxial and 300um HR Cz substrate to allow different applications (charge particles and soft X-ray)
- Cluster size increases with substrate voltage
  - Maximum at ~1.9 at 50 V at 120 e-
- Time resolution ~2ns
- Efficiency after 2×10^{15} n/cm^2 better than 98% at 50 V bias at 120 e-

EP R&D TPSCo 65nm ISC CMOS imaging technology

- Explore 65nm imaging process for future MAPS
  - high density than 180nm allows smaller pixels or more functionality
  - 300mm wafer allows larger sensor if stitching is used
- First MLR1 run: significant contributions from many groups and the ALICE ITS3 collaboration:
  - 55 test chips: IPHC: rolling shutter larger matrices, DESY: pixel test structure, RAL: LVDS/CML receiver/driver, NIKHEF: bandgap, T-sensor, VCO, CPPM: ring-oscillators, Yonsei: amplifier structures, CERN Transistor test structures, analog pixel test matrices (together with IPHC), digital pixel test matrix (DPTS) (32x32), pad structure for assembly testing.
  - Measurements:
    - analog front end, sensor process optimization (fully efficient operation in test beam) and building blocks proven.
    - First characterization of SEU cross-section of registers
    - No showstoppers on transistors and other X-ray irradiation measurements.



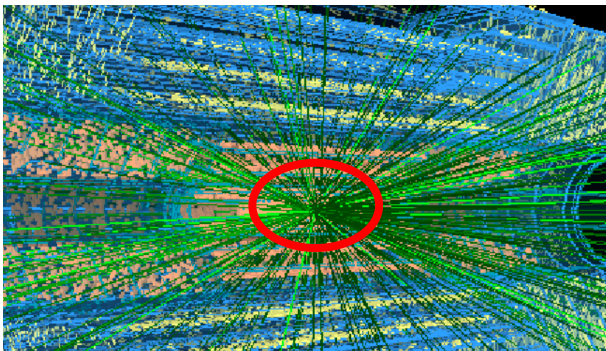
Looking towards the future

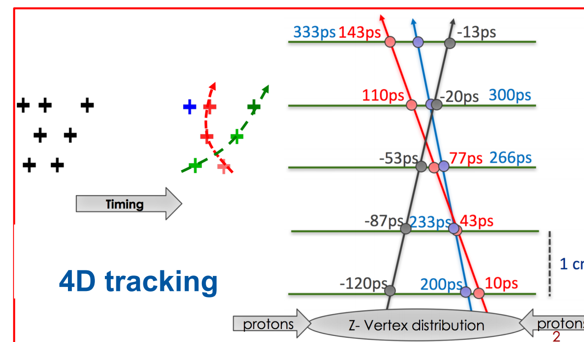
There are very challenging targets ahead at HL-LHC and future collider experiments for new silicon detectors

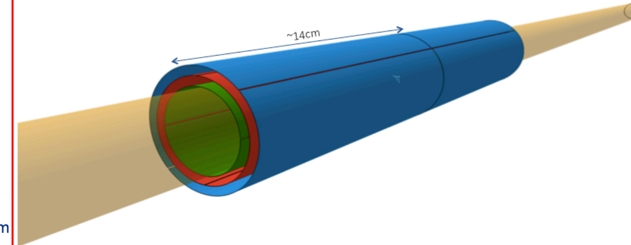
Radiation hard, thin and small pixel Vertex layers for very high hit-rates at innermost layers

Merge tracking and timing: how about a 10x10μm² pixel with 10ps timing? A dream for reconstruction

Ultra-thin detectors: reduced multiple scattering to maybe 1/10th of today?







Summary

- The required functionality from silicon tracking detectors leads to more and more complex detector systems to cope with accelerator's present and future performance

- The need for these new complex systems has triggered a **large RD effort in the area of sensors, electronics and detector integration**

- **Hybrid pixel** detector for HL-LHC cope with **enormous radiation level and hit rates** together with sophisticated on-chip data handling

- **Monolithic CMOS sensors** are being developed for **high-radiation environments with complex readout architectures** for future large pixel systems

- The **combination of timing and tracking** leads to the development of new sensors for new level of performance in future silicon system with **LGAD sensors**

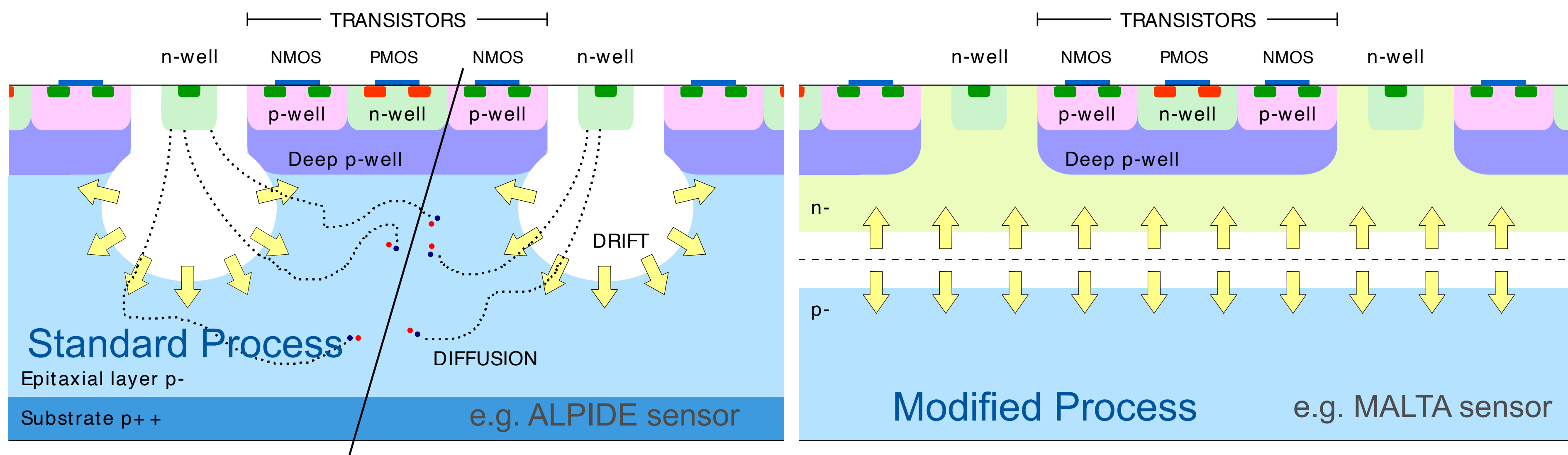
- Developing and **integrating these sensors to modules** and systems leads to many new RD collaborations with semiconductor industry for manufacturing and post-processing

Extra slides

CERN

MAPS with small electrodes

- Small collection electrode (few um^2)
- **Small input capacitance (<3fF) allows for fast & low-power FE**
- High S/N for a depletion depth of ~20um
- To ensure full lateral depletion, uniform n-implant in the epi layer (modified process)

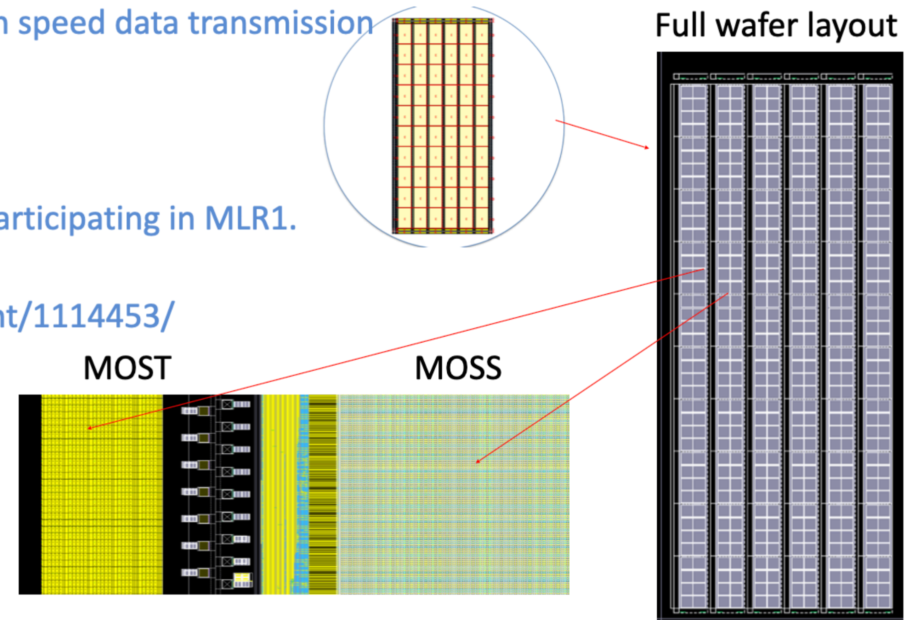


M. Munker, JINST 14 (2019) C05013
M. Dyndal, JINST 15 (2020) P02005
W. Snoeys, NIM A 871 (2017) 90-96
H. Pernegger, NIM A 986 (2021) 164381

TPSCo 65nm ISC CMOS imaging technology

EP R&D

- Next submission ER1: first stitched engineering run:
  - main purpose: prove and learn about wafer=scale stitching in our context, also for ITS3 ALICE upgrade needed for TDR.
  - Includes
    - two sensors MOSS and MOST, stitched in one direction over the full wafer (height ~ 26 cm)
    - a non-stitched pixel test chip originating from hybrid pixel effort (hybrid to monolithic or H2M)
    - several other pixel test chips
    - chips aimed at building blocks for instance for high speed data transmission
    - Transistor test chips
    - SEU test chip
  - New groups joining In addition to the groups already participating in MLR1.
  - Latest WP1.2 status report: https://indico.cern.ch/event/1114453/



17/02/2022

CERN