Radiation Hardness Assurance and Testing

Rudy Ferraro (BE-CEM-EPR)

R2E Annual Meeting – 1-2 March, 2022





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CERN RHA & Testing Challenges

Reliable component qualification is obtained through a wide variety of knowledges and activities:





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Radiation Effects on Electronics

			SEE	TID	DD
Active Elementary Devices	Transistor: Diodes:	MOSFET Bipolar Zener LED Schottky	SET, SEB, SEGR, SEL SET SET SET SET, SEB	$\begin{array}{c} \Delta V_{TH} \\ \Delta H_{CE}, \Delta I_{CE}, \Delta I_{BE}, \Delta V_{BE} \\ \Delta V_{F,} \Delta I_{L} \\ \Delta V_{F}, \Delta P, \Delta I_{L} \\ \Delta V_{F,} \Delta I_{L} \end{array}$	- $\Delta H_{CE}, \Delta I_{CE}, \Delta I_{BE}, \Delta V_{BE}$ $\Delta V_{F}, \Delta I_{L}$ $\Delta V_{F}, \Delta P, \Delta I_{L}$ $\Delta V_{F}, \Delta I_{L}$
Integrated Circuits	Digital: Analog: Mixed: Optronics:	Memory FPGA µController Opamp Regulators ADC DAC Smart Power Optocoupler PhotoMOS	<pre>SEU, SEFI, SEL, MBU SET, SEL SEU, SEFI, SEL, MBU,SET SET</pre>	$\begin{array}{c} \Delta I_{CC} \\ \Delta I_{CC,} \Delta t_{PD}, programma bility \\ \Delta I_{CC,} \Delta V_{REF} \\ \Delta v_{off}, \Delta I_{BIAS}, \Delta G, \Delta I_{quiescient} \\ \Delta I_{CC}, \Delta V_{REF}, \Delta V_{START} \\ \Delta I_{CC}, \Delta V_{REF}, \Delta V_{START} \\ \Delta I_{CC}, \Delta V_{REF}, \Delta_{ENOB} \\ \Delta I_{CC}, \Delta V_{REF}, \Delta_{ENOB} \\ \Delta I_{CC}, \Delta V_{REF}, \Delta_{INOB} \\ \Delta I_{CC}, \Delta I_{TH} \\ \Delta I_{TH,} \\ Switch capability \end{array}$	$\begin{array}{c} - \\ - \\ - \\ \Delta v_{off}, \Delta I_{BIAS}, \Delta G, \Delta i_{quiescient} \\ \Delta I_{CC}, \Delta V_{REF}, \Delta V_{START} \\ - \\ - \\ \Delta T_{P} \\ \Delta CTR, \Delta I_{TH} \\ \Delta I_{TH} \end{array}$
SoC Systems	Can contains all the above		Destructive events Temporary failures Permanent fault states	Performance degradation Parametric degradation	



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Radiation Effects on Electronics

		SEE	TID	DD	
Active Elementary Devices	Transistor:MOSFET BipolarDiodes:Zener LED Schottky	MIL-STD-750, SEB/SEGR ESCC25100	ESCC22900 (ELDR) MIL-STD 883 1019.8 MIL-STD750E 1019.5 ASTM F 1892-06	No standard yet but guidelines	
Integrated Circuits	Digital:Memory FPGA µControllerAnalog:Opamp RegulatorsMixed:ADC DAC Smart PoweOptronics:Optocouple PhotoMOS	Guideline, conference, journal, littérature etc: "Guideline for Optocoupler Ground Radiation Testing and Optocoupler Usage in the Space Radiation Environment", NASA "Field Programmable Gate Array (FPGA) Single Event Effect (SEE) Radiation Testing", NASA "SEE Testing of ADC and DAC", ESCIES RADECS Short courses NSREC Short courses			
SoC Subsystem Systems MegaSystems	Can contains all the above	No standards for system-level H. Quinn, "Challenges ir A. Coronetti et al., "Radiation Hardn Facility Requirements, Tes T. Rajkowski et al., "Comparison of of Load Converter Using Both Con	r system-level testing but guidelines exist (with a big contribution from CERN/R2E): In, "Challenges in Testing Complex Systems,"in IEEE TNS, April 2014 "Radiation Hardness Assurance Through System-Level Testing: Risk Acceptance, equirements, Test Methodology, and Data Exploitation," IEEE TNS 2021 , "Comparison of the Total Ionizing Dose Sensitivity of a System in Package Point r Using Both Component- and System-Level Test Approaches," Electronics 2021		

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Radiation Effects on Electronics

			SEE	TID	DD	
Active Elementary Devices	Transistor: Diodes:	MOSFET Bipolar Zener	MIL-STD-750, SEB/SEGR ESCC25100	ESCC22900 (ELDR) MIL-STD 883 1019.8 MIL-STD750E 1019.5	No standard yet but guidelines:	
		LED Schottky		Optoelectronic qualification for CERN Application		
	Digital:	Memory	Guideline, conference, journal, littérature etc.			
Integrated Circuits		μController	see presentation: "IoT BatMon: Wireless radiation monitoring at CERN", from A. Zimmaro			
	Analog:	Opamp Regulators	"Field Programmable Gate	Combined TID-DE) Effects on ICs	
	Mixed:	ADC DAC	"SEE Testing of ADC and DAC", ESCIES			
	Optronics:	Smart Power Optocoupler PhotoMOS	SET Response in Mixed-Field	Optoelectronic quali Applica	fication for CERN tion	
SoC	Can contains all the above		No standards for system-level testing but guidelines exist (with a big contribution from CERN/R2E):			
Subsystem			H. Quinn, "Challenges in Testing Complex Systems "in IEEE TNS, April 2014 See presentation: "IoT BatMon: Wireless radiation monitoring at CERN", from A. Zimmaro			
Systems MegaSystems			Facility Requirements, Test Methodology, and Data Exploitation," IEEE TNS 2021 T. Rajkowski et al., "Comparison of the Total Ionizing Dose Sensitivity of a System in Package Point of Load Converter Using Both Component- and System-Level Test Approaches," Electronics 2021			



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Optoelectronic Qualification: Context

- > Optoelectronic components are among the weakest part of a system exposed to displacement damage

 - → It is then crucial to have reliable degradation estimations to avoid premature failures in operation
- CERN Component-Level Qualification Process
 - TID: Gamma, DD: neutron DD+TID: proton sources
 - Displacement Damage in operation are estimated by using NIEL scaling theory



- Problem: Systematic NIEL scaling violations for optoelectronic semiconductor materials have been reported in many studies
- Objectives of this study: Investigate the use of application-specific radiation environments for displacement damage qualification for LHC applications



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COTS-based systems are installed in three main LHC areas:

- > **Tunnel**: Dispersion Suppression (DS) areas
 - High Energy (up to tens of GeV)
 - High pions and proton contributions
- Shielded Areas:
 - RR (Lightly Shielded)
 - High energies relatively attenuated
 - Pion and proton contributions attenuated
 - > UJ (Heavily Shielded)
 - High energies strongly attenuated
 - Negligible pion and proton contributions

→ Objective: Quantify the LHC DD spectra characteristics to be reproduced during radiation tests

Proton, pion and neutron Normalized Lethargy Spectra:





LHC Spectra DD characteristics obtained by combining LHC Spectra with particle NIELs Considered Materials: GaAs, AlGaAs, InGaAs

GaAs-like materials specific challenges:

- More sensitive to pion than Silicon
- Pion NIEL mostly theoretical





LHC Spectra DD characteristics obtained by combining LHC Spectra with particle NIELs Considered Materials: GaAs, AlGaAs, InGaAs Typical Spectra DD characteristics:

- Particle contribution to total DD:
 - Si: Negligible proton/pion contributions
 - GaAs/InGaAs/AlGaAs:
 - Proton / pion contributions decrease while shielding increase





LHC Spectra DD characteristics obtained by combining LHC Spectra with particle NIELs **Considered Materials:** GaAs, AlGaAs, InGaAs **Typical Spectra DD characteristics:**

- > Particle contribution to total DD:
 - **Si:** Negligible proton/pion contributions
 - GaAs/InGaAs/AlGaAs:

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- contributions Proton pion decrease while shielding increase
- > Energy Distribution:
 - DD Normalized Reverse Integral (NRI)
 - H_{50%}, H_{10%}: Energy values for which the DD fluences contributes to 50% and 90% of the total displacement damages.

These characteristics has to be reproduced in test environments.





Optoelectronic qualification: Solution



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Test radiation fields characteristics:

- > CHARM (CERN):
 - R6CuOOOO
 - \rightarrow Energies similar to RR
 - \rightarrow Contributions similar to tunnel
 - R1CuOOOO
 - → Energies between RR & UJ
 → Contributions similar to RR
- > JSI (Jozef Stefan Institute) :
 - Nuclear reactor → neutron only
 - Softer energy spectra than UJ
 - Same particle contributions as UJ
- > PSI (Paul Scherrer Institute):

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200 MeV proton beam





- > Clear difference between the different materials
 - AIGaAs factors three times lower than InGaAs
 - \circ ... and 18 times than GaAs

→ InGaAs and AIGaAs are better candidates for radiation environments



CTR = Curent Transfer Ratio



- Very Good agreement JSI/CHARM-R1 \geq
 - Negligible proton/pion contributions in position 1 0
 - Very different energy spectra
 - → No Neutron NIEL violations





CTR = Curent Transfer Ratio

- Clear difference between the materials
- Good agreement JSI/CHARM-R1

≻ Systematic diff CHARMR1 → CHARMR6

- Factors in position 6 about -20% lower for all materials ,
- \circ ~25% of proton and of pion contributions

→ Overestimation of the pion/proton damages?

- NIEL overestimation (→ NIEL model issue)
- Flux overestimation (\rightarrow FLUKA simulation issue)







Lifetime-damage factors comparison

- Clear difference between the materials
- Good agreement JSI/CHARM-R1
- Systematic diff CHARMR1 → CHARMR6
- Proton results not consistent with neutrons/mixed field,
 - No consistent trend observed within the devices
 - ∧ AlGaAs: proton damage two times higher
 → Overestimation of the damage in operation
 - InGaAs: proton damages 4 times lower
 - \rightarrow Underestimation of the damage in operation
 - → Can lead to premature failure in operation



CTR = Curent Transfer Ratio



Optoelectronic Qualification: Resources





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Combined TID-DD effects on ICs: Context

- At CERN, systems can be highly distributed and exposed to a wide variety of ionizing and non-ionizing dose levels.
- Integrated Circuits (ICs) are made of several transistors that can exhibit different sensitivities to TID and DD effects
- In operation different DD/TID rate ratios could lead to complete different component degradation profiles
- Impossible to estimate from individual TID and DD irradiations for most of the components
- No standards or test methodology exist for combined TID-DD qualification



> Objectives of this Study:

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Investigate the impact of the LHC radiation environments on the qualification process of component sensitive to combined TID-DD effects and propose a qualification methodology against this effect



Combined TID-DD effects on ICs: Solution





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Combined TID-DD effects on ICs: Examples

Analysis of Bipolar Integrated Circuit Degradation Mechanisms Against Combined TID-DD Effects

Rudy Ferraro¹⁰, Rubén García Alía¹⁰, Member, IEEE, Salvatore Danzeca, and Alessandro Masi¹⁰

dose (TID) and displacement damage (DD) effects can exhibit degradation profiles resulting from a combination of degradation mechanisms induced by both effects. This work presents circuit simulations based on experimental data to explain degradation mechanisms induced by combined TID and DD effects on a bipolar IC current source. First, the effect of the degradation of each internal transistor on the circuit's response is evaluated by applying electrical parametric changes. Then simulations are performed from different degradation scenarios based on observed circuit behaviors to reproduce the different TID, DD, and combined TID-DD responses. These simulations show that a synervistic interaction between a current leakage induced by DD in [4] and [5]. However, this is not systematically true, and on a transistor located in the bandgap reference part with the as it is the case for TID and DD, it has also been shown that gain degradation of a current mirror induced by both TID and the different internal transistors of an IC can exhibit different DD appears to be responsible for the combined TID-DD response. It is also shown that the circuit degradation rate depends on the DDD/TID rate ratios encountered during the exposition

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Index Terms-Displacement damage (DD), IC radiation response, nonionizing energy loss, particle accelerator, total ionizing dose (TID).

I INTRODUCTION

THE total degradation response of integrated circuits all their internal transistors [1], [2] independently of the technology used (CMOS, BiCMOS, or bipolar). While CMOS technology is only affected by total ionizing dose (TID) and DDD that COTS are exposed to), the bipolar technology, and thus the BiCMOS one as well, can be affected by both TID circuit level. and DD, and even enhanced low dose rate (LDR) sensitivity (ELDRS) effect.

This interaction of the radiation effects at the internal circuit level can make challenging the qualification of devices ponent the different degradation mechanisms can combine exposed to environments inducing both effects such as the ones present in high-energy accelerators, nuclear reactors, or deep space missions. At CERN, the qualification of ICs against such combined effects is a major concern for radiation hardness assurance (RHA). The large hadron collider (LHC) environments present a wide range of DDD/TID rate ratios

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Abstract-Integrated circuits sensitive to both total ionizing that can lead to completely different degradation rates as it has been demonstrated in our previous work [3] with a bipolar IC current source exposed to different ratios.

While no qualification standards exist for ICs exhibiting combined TID-DD internal circuit effects, a similar phenomenon has been intensively studied in the literature, which is the qualification of circuits exhibiting circuit effects induced by ELDRS. For this effect, it has been shown that for most of the devices the total circuit degradation could be related to the degradation of a single transistor in the circuit such as sensitivities to the ELDRS effect and therefore a device can present completely different degradation profiles depending on the TID dose rate [6]. Therefore, the proposed methodology to qualify components against this effect is to identify the worst case responses by irradiation at very LDRs [7], [8], assessing the LDR degradation or dependence of the device.

In our previous work [3], the same approach was followed and a similar methodology to qualify components against exposed to radiation results from the degradation of combined TID-DD based on the assessment of the dependence between degradation and failure rate with the DD over TID rate ratio. An example of the application of this methodology was proposed with a bipolar IC whose observed changes not by displacement damage (DD) dose (DDD) (for standard in degradation profiles with different DDD/TID ratios were assumed to be due to degradation interactions at the internal

This article aims to propose a deeper analysis of the behavior of this component through simulations based on experimental data to understand in detail how in this comand lead to the observed responses. First, the device response against TID and DD will be presented. Then, the simulation model is introduced and the impact of the degradation of each internal component on the circuit response is demonstrated. Then, based on experimental assumptions two circuit degradation profiles are defined to simulate the device response against TID and DD individually. Finally, it is demonstrated how the Manuscript received March 22, 2021; revised May 3, 2021; accepted impact of the DD on the circuit can be enhanced by the TID

II. CIRCUIT MODEL

The device used for this study is the LM334, which is a proportional-to-absolute temperature (PTAT) adjustable current source. No simulation model is provided by the

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R. Ferraro, R. G. Alía, S. Danzeca and A. Masi, "Analysis of Bipolar Integrated Circuit Degradation Mechanisms Against Combined TID–DD Effects," in IEEE Transactions on Nuclear Science, vol. 68, no. 8, pp. 1585-1593, Aug. 2021, doi: 10.1109/TNS.2021.3082646





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Radiation Test Service for Equipment Groups by R. Ferraro (BE-CEM-EPR)

Conclusions

- Reliable component qualification requires knowledge of radiation effects from the lowest level, the material, to the highest level like ICs or System-On-Chip
- Testing standards and guidelines inherited from the space field provide a valuable starting point for our community
- Many of these standards does not apply to particle accelerator spectra and a constant work is being done to develop qualification methods dedicated to CERN
- We have identified weaknesses in the traditional testing methodologies, especially for the qualification of optoelectronics and combined TID-DD effects on ICs
- Then qualification methodologies dedicated to the LHC environments were developed for these two topics
- > It was shown the huge impact on the qualification of having unreliable qualification procedure
- Numerous studies are still been carried out to evaluate methodologies and guidelines for other types of effects



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Thank you for your attention!





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Combined TID-DD effects on ICs: LHC levels Analysis

> Taking the DS area as example:



> DDEF/TID Ratio weighted Distribution:

Combined TID-DD effects on ICs: Solution

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Combined TID-DD effects on ICs: Examples

> Current Source (LM334):

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- Same degradations profile as DD one
- Different degradation mechanism than TID
- Degradation rate increase with TID contribution
- Combined TID+DD response unpredictable from individual TID & DD responses



Combined TID-DD effects on ICs: Solution





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