MIL-STD-1553/1760
5V Monolithic Dual Transceiver
# αRD1567 - prototype

## General Description

The αRD1567 is low power CMOS dual transceiver designed to meet the requirements of MIL-STD-1553/1760 specifications.
The transmitter section of each channel takes complimentary CMOS/TTL digital input data and converts it to bi-phase Manchester encoded 1553 signals suitable for driving the bus isolation transformer. Separate transmitter inhibition control signals are provided for each transmitter.
The receiver section of the each channel converts the 1553 bus bi-phase data to complimentary CMOS/TTL data suitable for inputting to a Manchester decoder. Each receiver has a separate enable input which can be used to force the output of the receiver to a logic 0. To minimize the package size for this function, the transmitter outputs are internally connected to the receiver inputs, so that only two pins are required for connection to each coupling transformer.

The αRD1567 have 5000V HBM built-in ESD protection.

## Ordering information

**Table 1.**

| Part | Temp. range, °C | Package | Package drawing | Burn-In case temp, °C | Burn-In time, hrs |
|---|---|---|---|---|---|
| αRD1567 | –55 to +125 | 24-lead CFP | Figure 4 | +125 | 240 |

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## Pin Function Description

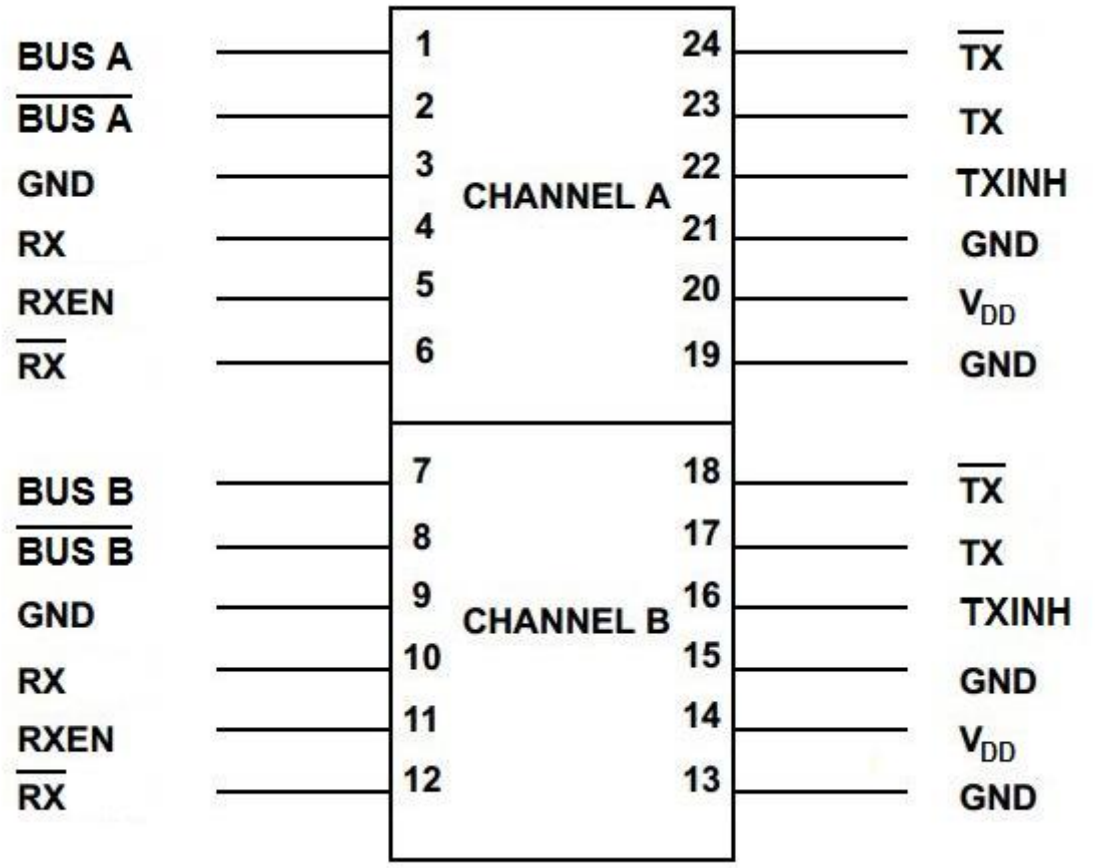



**Table 2.**

| Description | Mnemonic | Pin № | |
|---|---|---|---|
| | | Channel A | Channel B |
| MIL-STD-1533 bus positive signal | BUS | 1 | 7 |
| MIL-STD-1533 bus negative signal | $\overline{\text{BUS}}$ | 2 | 8 |
| Ground | GND | 3, 19, 21 | 9, 13, 15 |
| Receiver output | RX | 4 | 10 |
| Receiver enable | RXEN | 5 | 11 |
| Receiver output inv | $\overline{\text{RX}}$ | 6 | 12 |
| Pover Input | $V_{DD}$ | 20 | 14 |
| Transmitter inhibition | TXINH | 22 | 16 |
| Transmitter input | TX | 23 | 17 |
| Transmitter input inv | $\overline{\text{TX}}$ | 24 | 18 |

## Operating conditions and absolute maximum ratings

**Table 3.**

| Characteristics, units | Symbol | Operating conditions | | Absolute maximum ratings | |
|---|---|---|---|---|---|
| | | min | max | min | max |
| Supply Voltage, V | $V_{DD}$ | 4,5 | 5,5 | – | 7 |
| Logic Input voltage (high), V | $U_{IH}$ | 2 | $V_{DD}$ | –0,3 | $V_{DD}$ |
| Logic Input voltage (low), V | $U_{IL}$ | 0 | 0,8 | –0,3 | $V_{DD}$ |
| Receiver differential voltage, V | $U_{I\,R}$ | – | 9 | – | 10 |
| Peak output current, A | $I_{OUT}$ | – | 0,55 | – | 1 |
| Power dissipation, W | $P_{TOT}$ | – | 0,95 | | 1,1 |
| Simultaneous transmission by both channels is not allowed. Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. | | | | | |

## Electrical characteristics within operating temperature range

**Table 4.**

| Parameter, units | Symbol | Condition | min | typ | max |
|---|---|---|---|---|---|
| Input Current, μA | $I_{IH}$ | $V_{DD}$ = 5,5V $V_{IH}$ = $V_{DD}$ | – | 0,04 | 10 |
| | $I_{IL}$ | $V_{DD}$ = 5,5V, $V_{IL}$ = 0 | –10 | 0,04 | 0 |
| Supply Current, mA | $I_{CC}$ | $V_{DD}$ = 5,5V, no transmission | – | 7 | 24 |
| | $I_{CC1}$ | $V_{DD}$ = 5,5V, 50% duty cycle | – | 250 | 352 |
| | $I_{CC2}$ | $V_{DD}$ = 5,5V, 100% duty cycle | – | 450 | 600 |
| Receiver section | | | | | |
| Output Voltage HI, V | $U_{OH}$ | $V_{DD}$ = 4,5V, $I_{OH}$ = -0,4 mA | 2,7 | 4,3 | – |
| Output Voltage LO, V | $U_{OL}$ | $V_{DD}$ = 4,5V, $I_{OH}$ = 1 mA | – | 0,15 | 0,4 |
| Threshold Voltage, V | $V_{TH}$ | $V_{DD}$ = 5V, 1 MHz sine wave | 0,28 | 0,56 | 1,2 |
| Input Differential Resistance, kOhm | $R_I$ | $V_{DD}$ = 4,5V | 20 | 63 | – |
| Receive Delay, ns | $t_R$ | $V_{DD}$ = 4,5V | – | 250 | 480 |
| Receiver Enable Delay, ns | $t_{R\ EN}$ | $V_{DD}$ = 4,5V | – | 25 | 50 |
| Transmitter section | | | | | |
| Output Voltage, V | $U_{O\ pp}$ | $V_{DD}$ = 4,5…5,5V, $R_L$ = 35 Ohm, fig. 1 | 6 | 7,5 | 9 |
| | | $V_{DD}$ = 4,5…5,5V, $R_L$ = 70 Ohm, fig. 2 | 18 | 22,5 | 27 |
| Transmitter Noise, mV | $U_{N\ pp}$ | $V_{DD}$ = 4,5…5,5V | – | 0,3 | 10 |
| Output Dynamic Voltage Offset, mV | $U_{O\ DIN}$ | $V_{DD}$ = 4,5…5,5V, $R_L$ = 35 Ohm, fig. 1 | –90 | ±5 | 90 |
| | | $V_{DD}$ = 4,5…5,5V, $R_L$ = 70 Ohm, fig. 2 | –270 | ±15 | 270 |
| Output Differential Resistance, kOhm | $R_O$ | $V_{DD}$ = 4,5V, no transmission | 10 | 173 | – |
| Transmission Delay, ns | $t_T$ | $V_{DD}$ = 4,5V | – | 90 | 200 |
| Transmitter Inhibition Delay, ns | $t_{THL\ INH}$ | $V_{DD}$ = 4,5V | – | 30 | 120 |
| | $t_{TLH\ INH}$ | $V_{DD}$ = 4,5V | – | 70 | 190 |
| Rise/Fall Time, ns | $t_F$ | $V_{DD}$ = 4,5…5,5V | 100 | 170 | 300 |

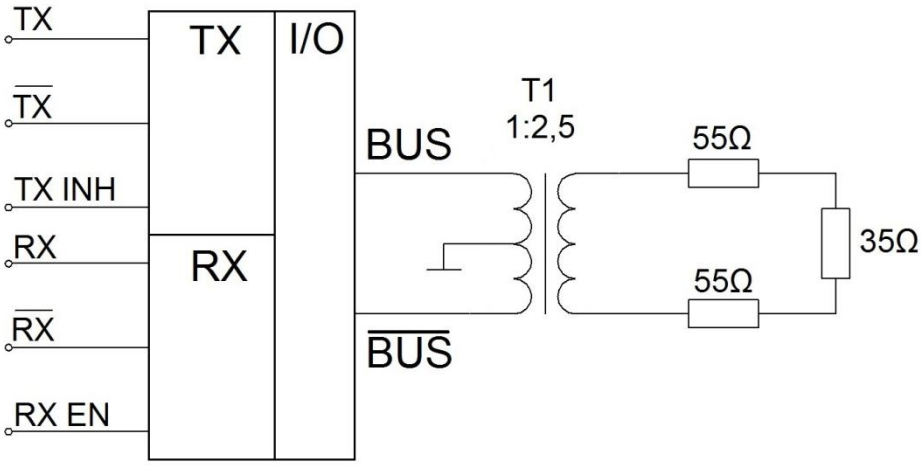



**Figure 1 – Test circuit, direct coupling to MIL-STD-1553 BUS Ω**

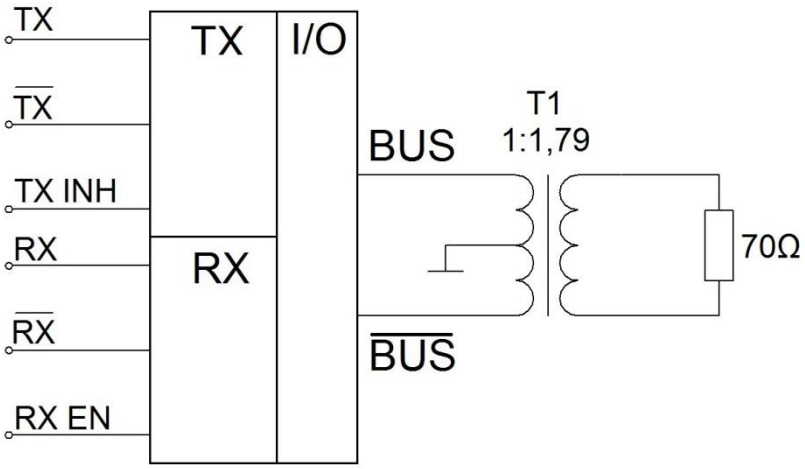



**Figure 2 – Test circuit, transformer coupling to MIL-STD-1553 BUS**

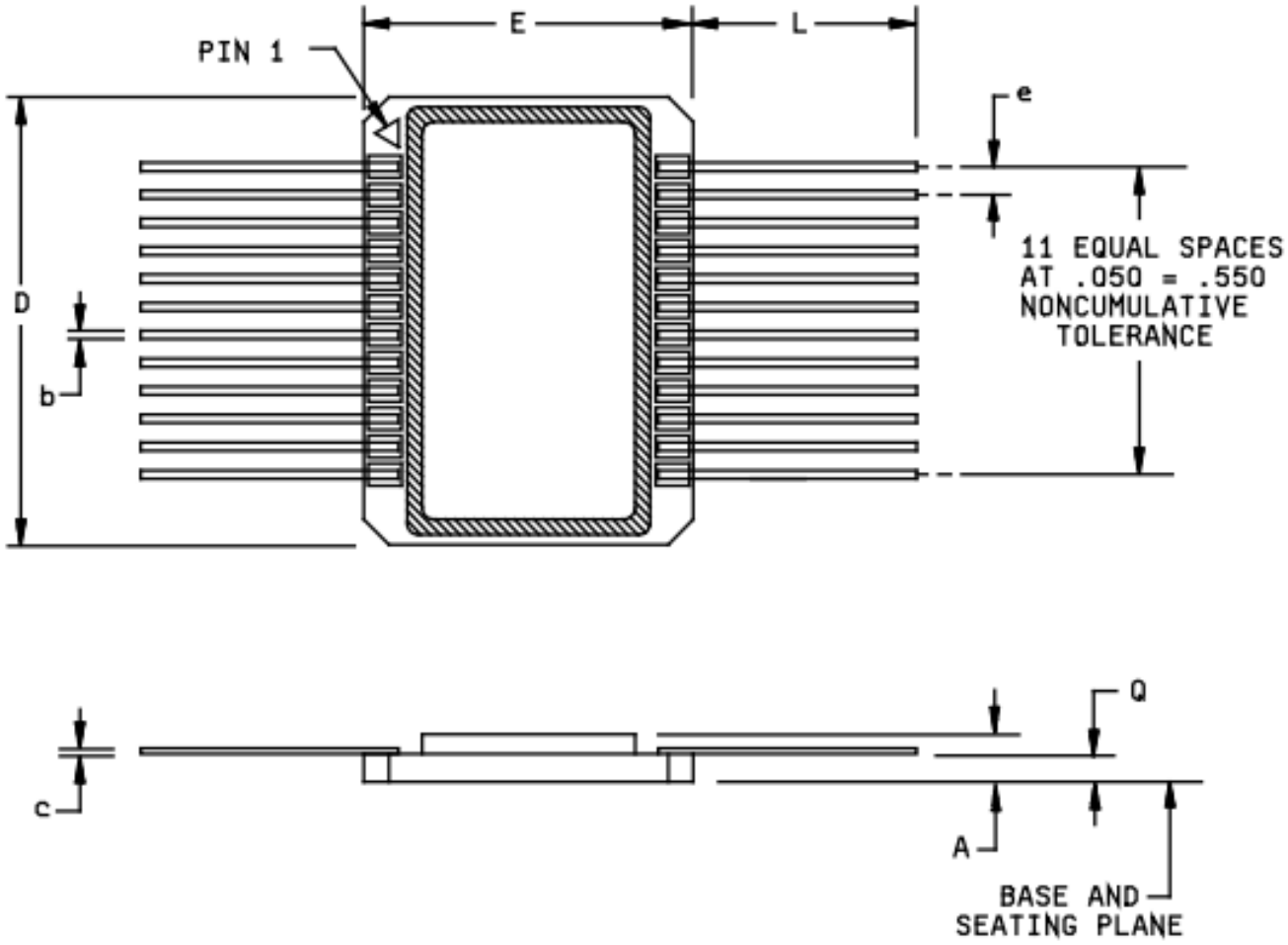
## Recommended thermal protection

Package should be mounted to or contact a heat removal rail located in the printed circuit board. To insure proper heat transfer between the package and the heat removal rail, use a thermally conductive material between the package and the heat removal rail.

## Layout

To minimize Output Dynamic Voltage Offset, layout differences between BUS and $\overline{BUS}$ lines and between TX and $\overline{TX}$ lines should be minimal.

## Physical Dimensions




| Dimension | Inches | |
|---|---|---|
| | Min | Max |
| A | | .095 |
| b | | .018 |
| c | .007 | .013 |
| D | | .810 |
| E | .580 | .600 |
| e | .045 | .055 |
| L | .400 | |
| Q | .060 | .080 |

**Figure 4 – CFP-24 package dimensions**

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