Electronic Engineering @ CERN

BL4S 2022

(28/09/2022)

Manoel Barros Marin

Electronic Engineering @ CERN

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Outline:

- Introduction
- Electronics @ CERN
- Electronics Development
- Summary

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- **Introduction**
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  - Electronics Development
  - Summary

Manoel Barros Marin

Introduction

Who is this guy talking to us…?

Introduction

General information

- Born in Santiago de Compostela, the capital of Galicia (**Spain**)
- Languages (**English, French,** Spanish, Galician)

Relevant information before arrival at CERN

- Electronics design in my **laboratory at home**
- **Worked** in construction companies to cover my studies

University studies:

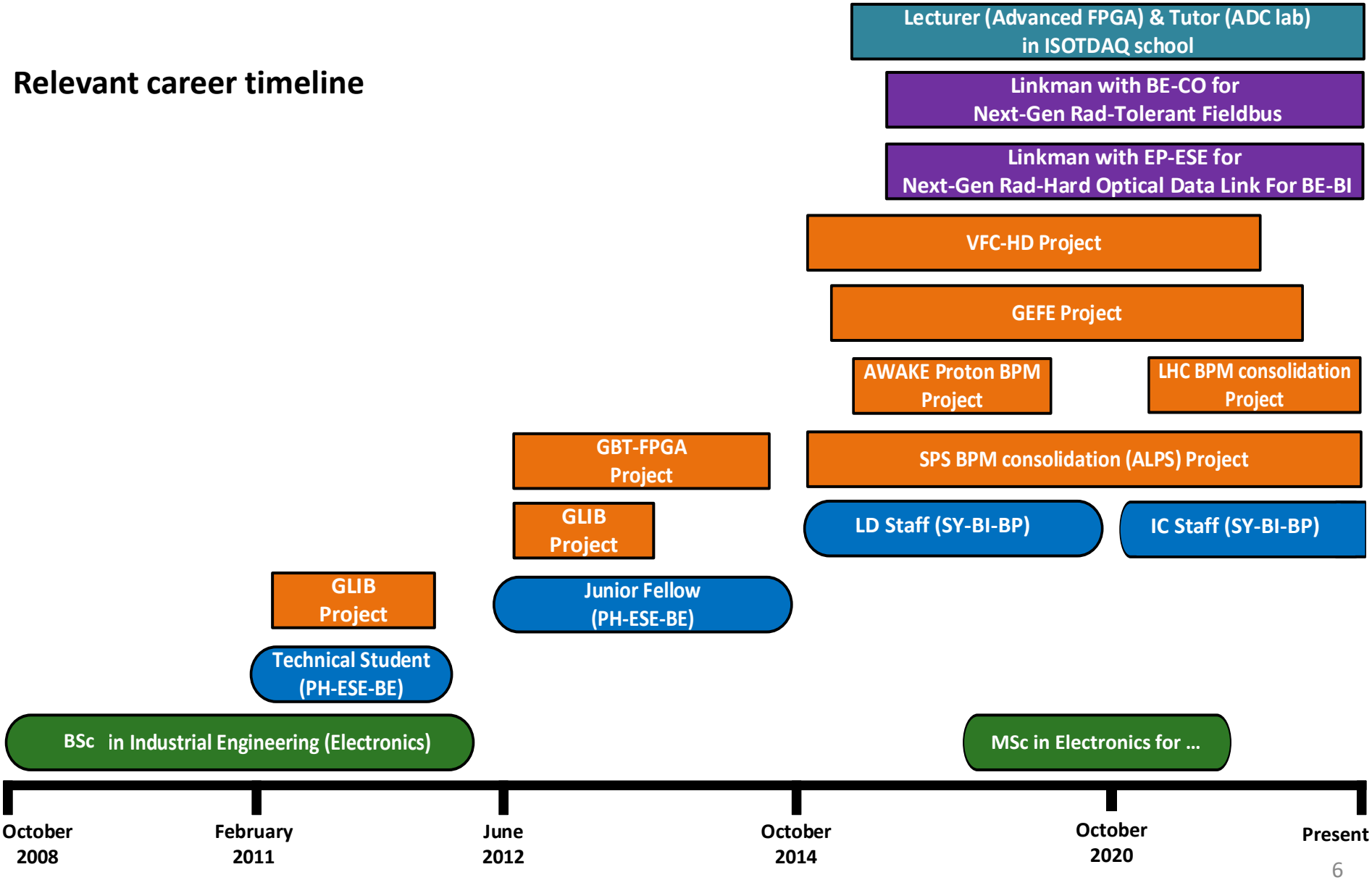
- **BSc in Industrial Electronics**
- **MSc in Electronics for Information and Communication**
- Awards:
  - 2013: "**Excellency in Industrial Technical Engineering (Electronics)** (full Bachelor's Degree)"
  - 2012: "Excellency in Industrial Technical Engineering (Electronics) (academic season 2009-2010)"

Interests

- **Sports:** biking, fitness, snowboarding and kite-surfing
- **Other activities:** photography, DIY, technical books, … and playing with my cats!!

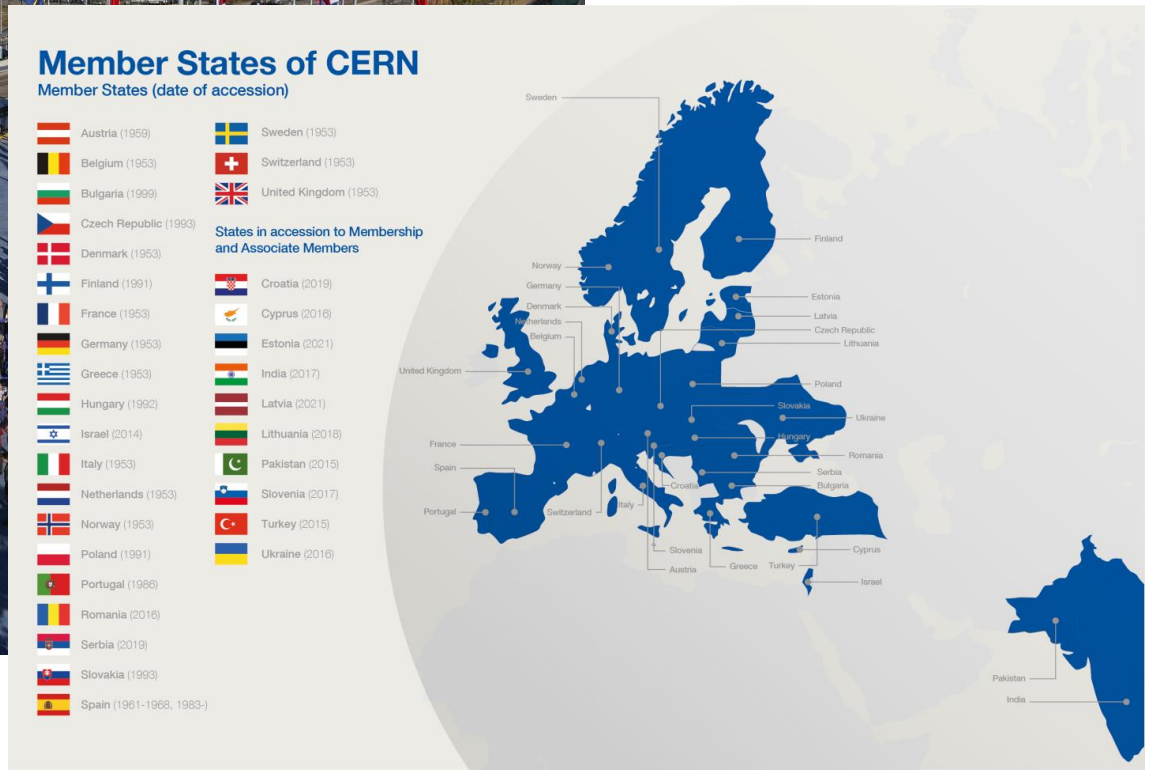
Introduction

Relevant career timeline



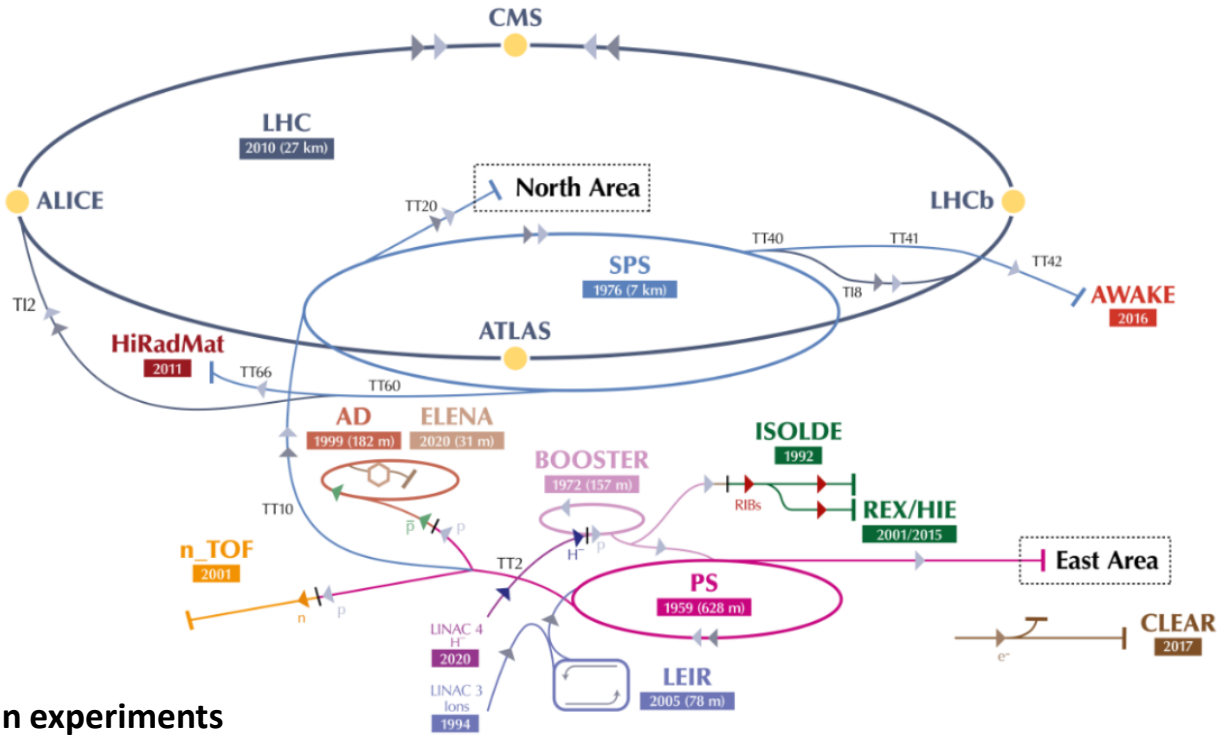
Introduction

CERN: Conseil Européen pour la Recherche Nucléaire



Introduction

Accelerators complex



The four main experiments

ATLAS EXPERIMENT

CMS

ALICE

LHCb

Other experiments

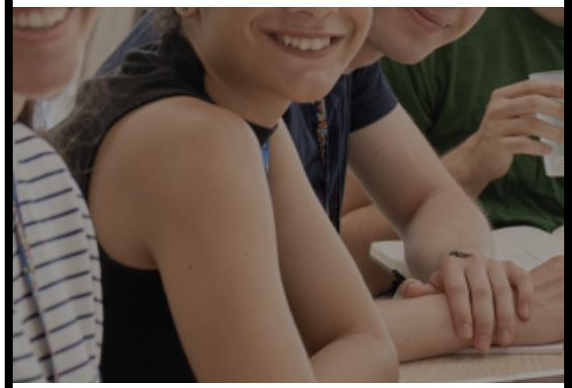
ELENA
Extra Low ENergy Antiprotons

ISOLDE

And Many More!!

Introduction

https://careers.smartrecruiters.com/CERN/students



DOCTORAL STUDENT PROGR

This is a chance to work on you
forefront of science. Whether y
your decision, if your specialisn
this is an invitation to further yo
fact, it's an invitation to get invo
unprecedented scale and scop
else on Earth.
Specific programmes are in pla
Czech Republic, and Norway. C

MARIE-CURIE PHD POSITION

hinking of doing your PhD abro
research beyond the horizon o
Skłodowska-Curie PhD fellowsh
the right opportunity for you.

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There's no better way to learn
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you're an undergraduate in Ap
looking for a practical training p
could spend 4 to 12 months at
or Master). An extension of up

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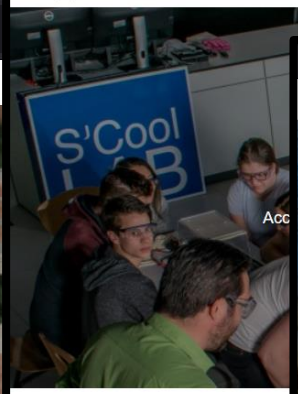

Take part in the Graduate Prog

What could be a better boost for your
largest scientific experiments in the w
develop your technical skills, knowled

If you're a recent graduate from univ
doubt looking for the chance to make
three years working right at the forefr
you could join us for research work in
development work in a broad range o
fields. Whichever route you take, it w

An experience like nowhere else on E

Categories of Graduates

CERN offers different categories of g
levels of education and experience. E
one that best matches your profile. Ta

- **The ORIGIN Programme (Earl**
  Member or Associate Member S
  experience after completing you

- general secondary education, techn
- Bachelor or Master's degree

- **The QUEST Programme (Exp**
  of Member or Associate Membe
  2 and 6 years' experience or Ph
  experience.
- **The RESEARCH Fellowship F**

- Theoretical and Experimental Physi
the fields of theoretical and experimental physics holding a PhD and up to six
years' experience in the field after obtaining their PhD;

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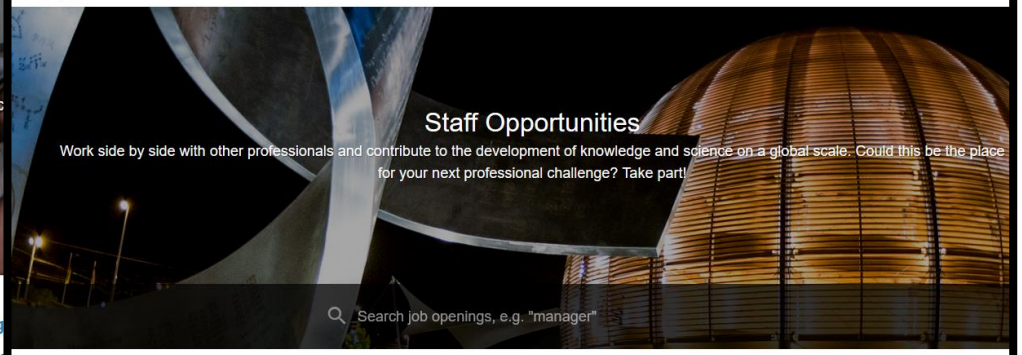

We're not just world-famous for science. To conduct experiments of this scale and importance, we need the very best talent in every part of our organization. Which means, if you're interested in joining us as a professional, CERN needs technicians, engineers, physicists, administration support, lawyers, accountants and many more.

CERN would very much like to benefit from your expertise, commitment and passion. This is more than an opportunity to develop your career: it's an opportunity to develop knowledge and science on a global scale. In fact, it's an opportunity like nowhere else on Earth.

If you join us as a member of staff, we would offer you an initial contract of up to 5 years.

In addition to an exciting career opportunity, CERN offers a comprehensive and competitive benefits package. People here enjoy living a truly cosmopolitan life in the heart of Europe. It's not just the work and atmosphere that makes people enjoy their jobs, it's the tangible elements that they receive too.

Find out more about CERN's benefits package, and about Staff employment conditions.

We have new vacancies opening up regularly.

If you want to join us, see what's on offer below.

HR EXCELLENCE IN RESEARCH

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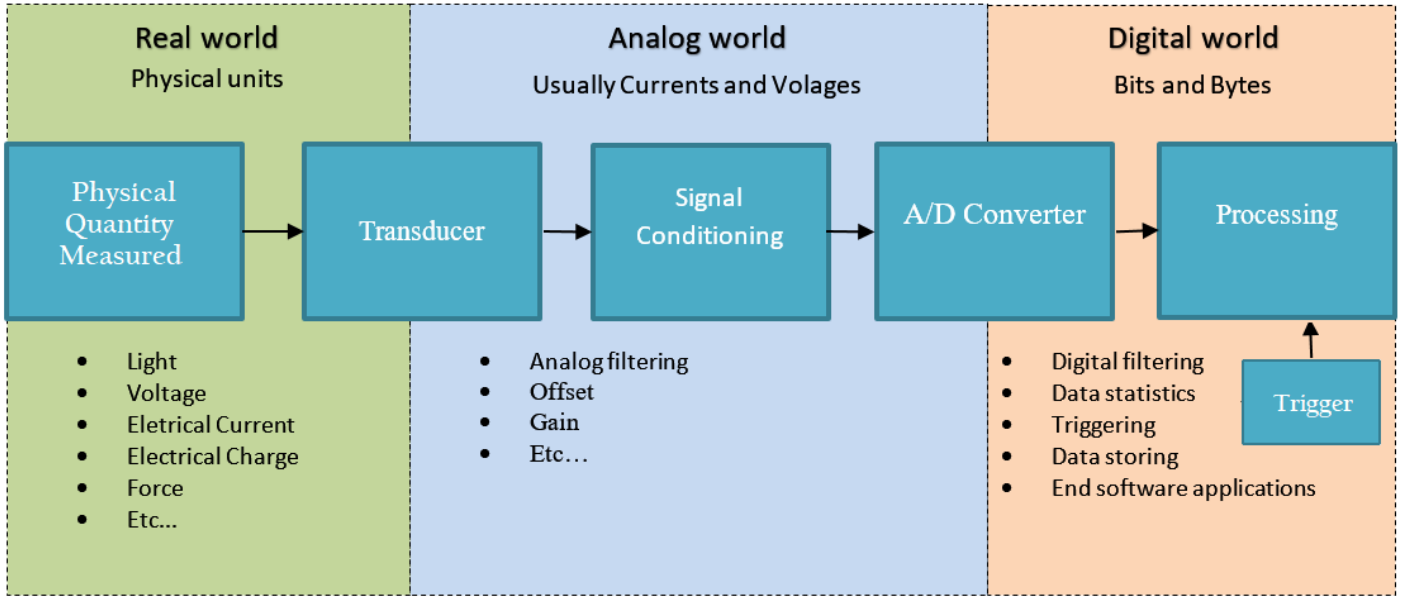
Electronics @ CERN

Block diagram of typical Trigger & Data AcQuisition (TDAQ) system

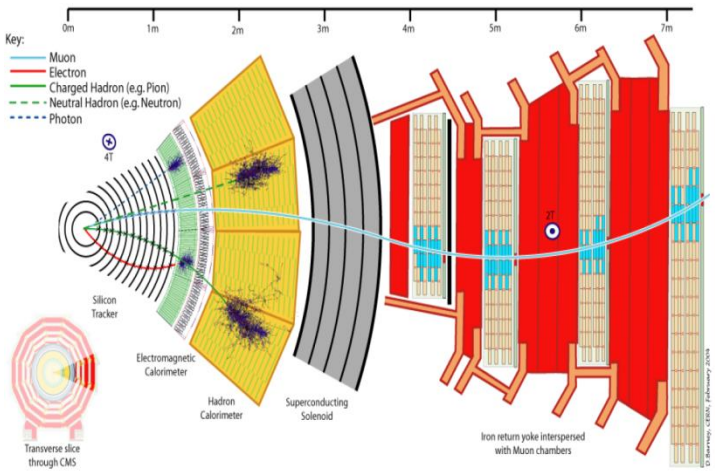


Electronics @ CERN

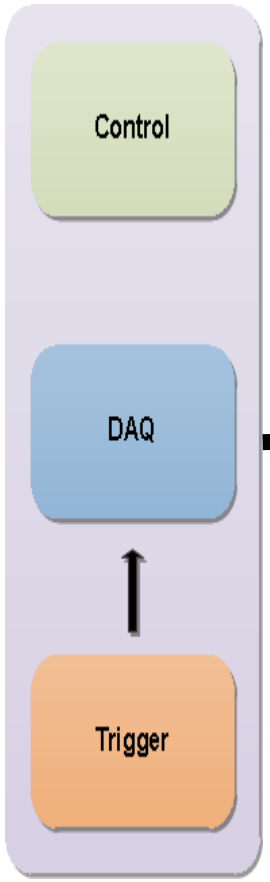
Example of TDAQ for High-Energy Physics (HEP) Experiments

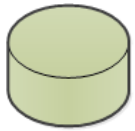
Exposed to Radiation

Front-End



Back-End





Mass Storage

Electronics @ CERN

Example of TDAQ for Particle Accelerators

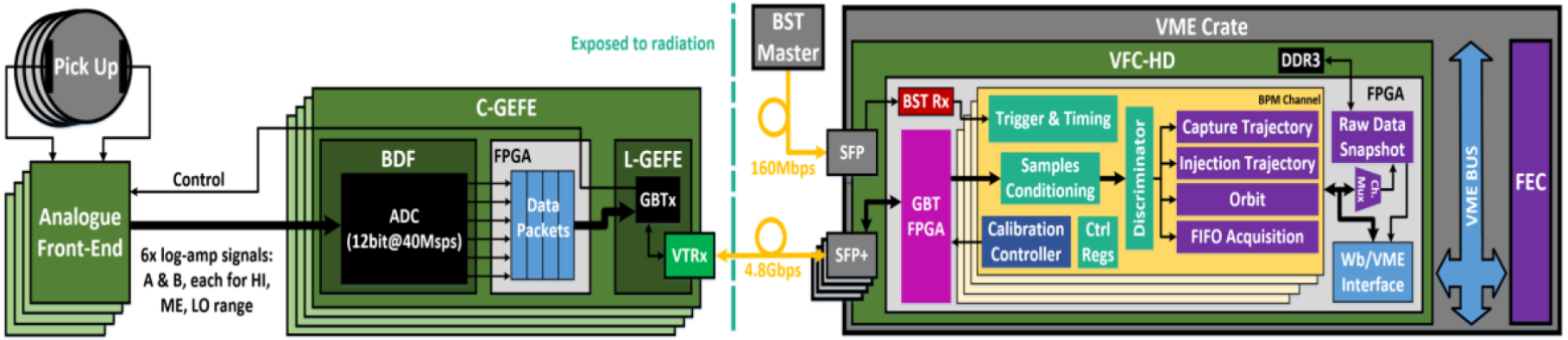
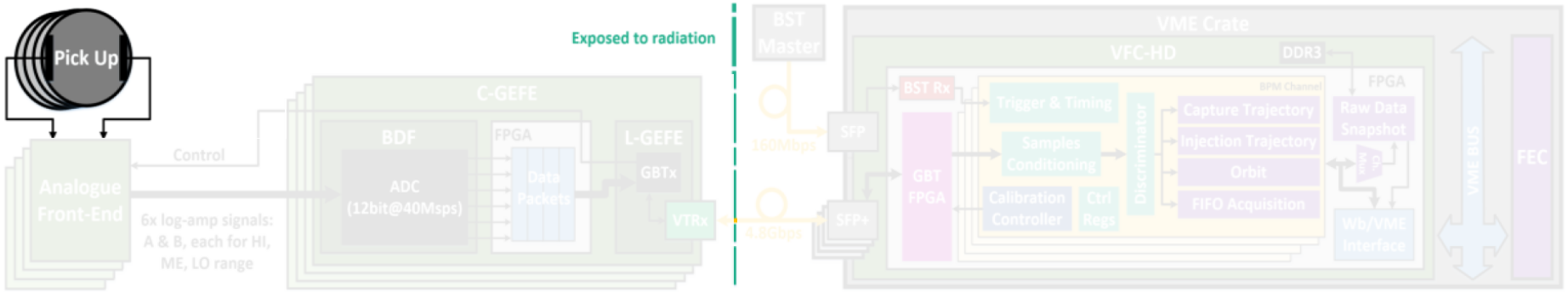


Diagram of a single channel of the ALPS system

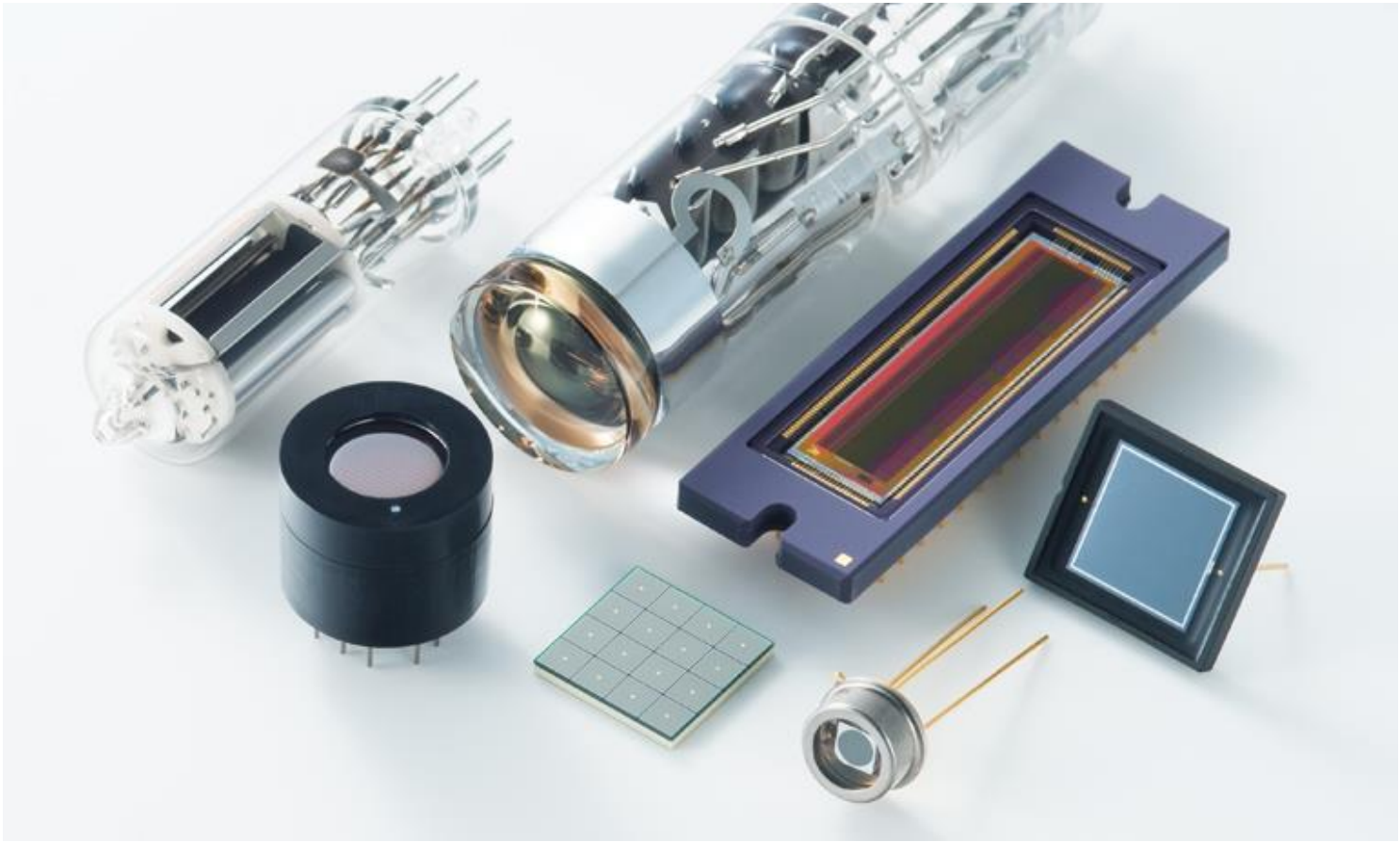
Electronics @ CERN

Sensor



Electronics @ CERN

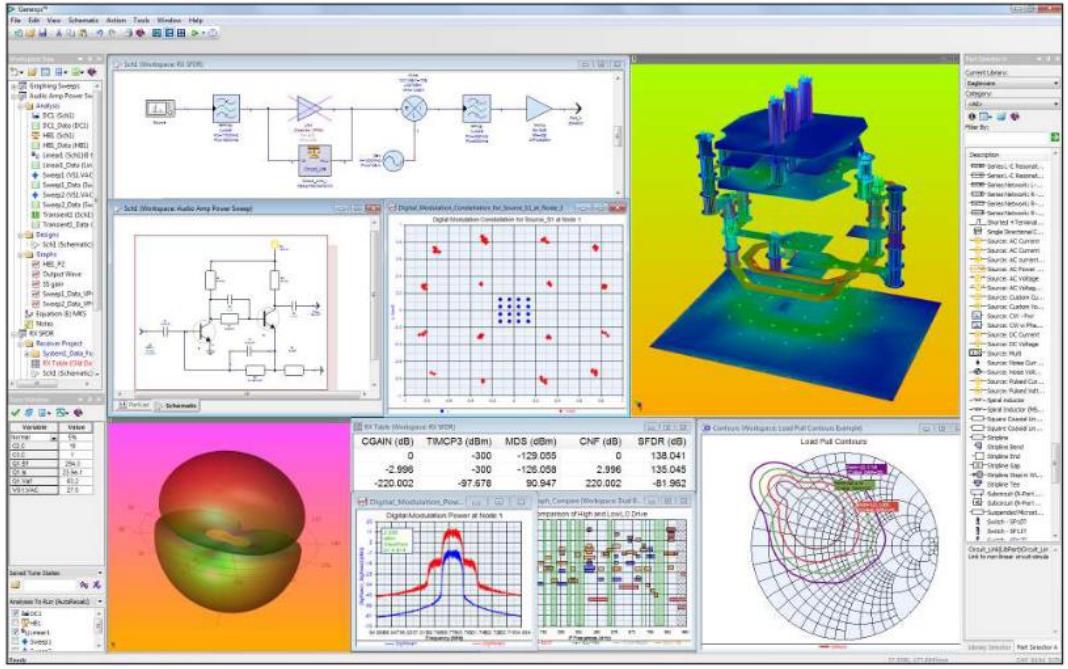
Sensors



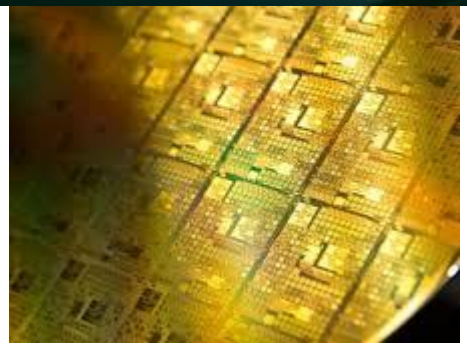
Electronics @ CERN

Sensors

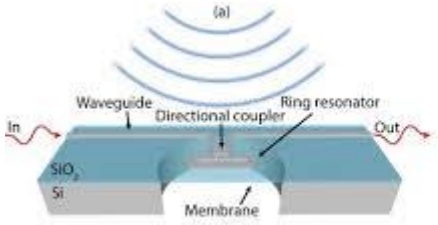
RF electronics

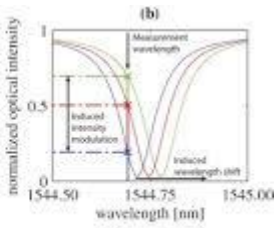


Microelectronics



Physics





Electronics @ CERN

Sensors

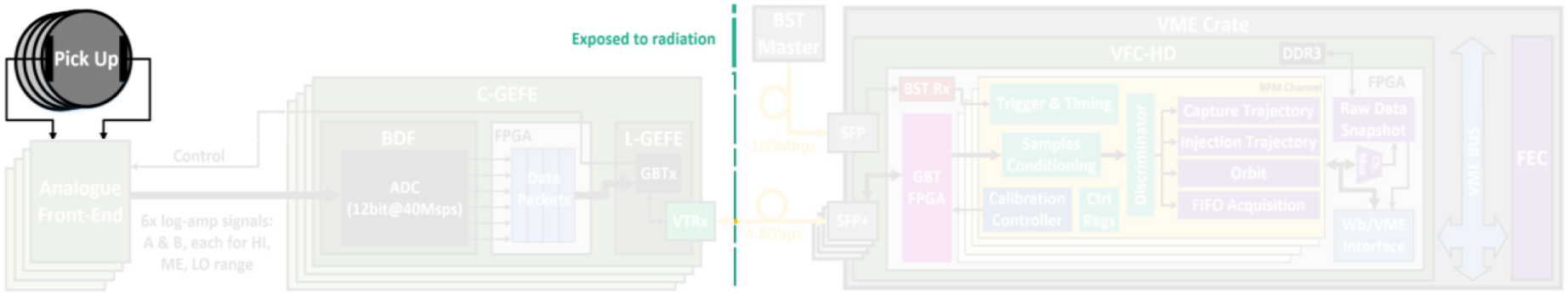
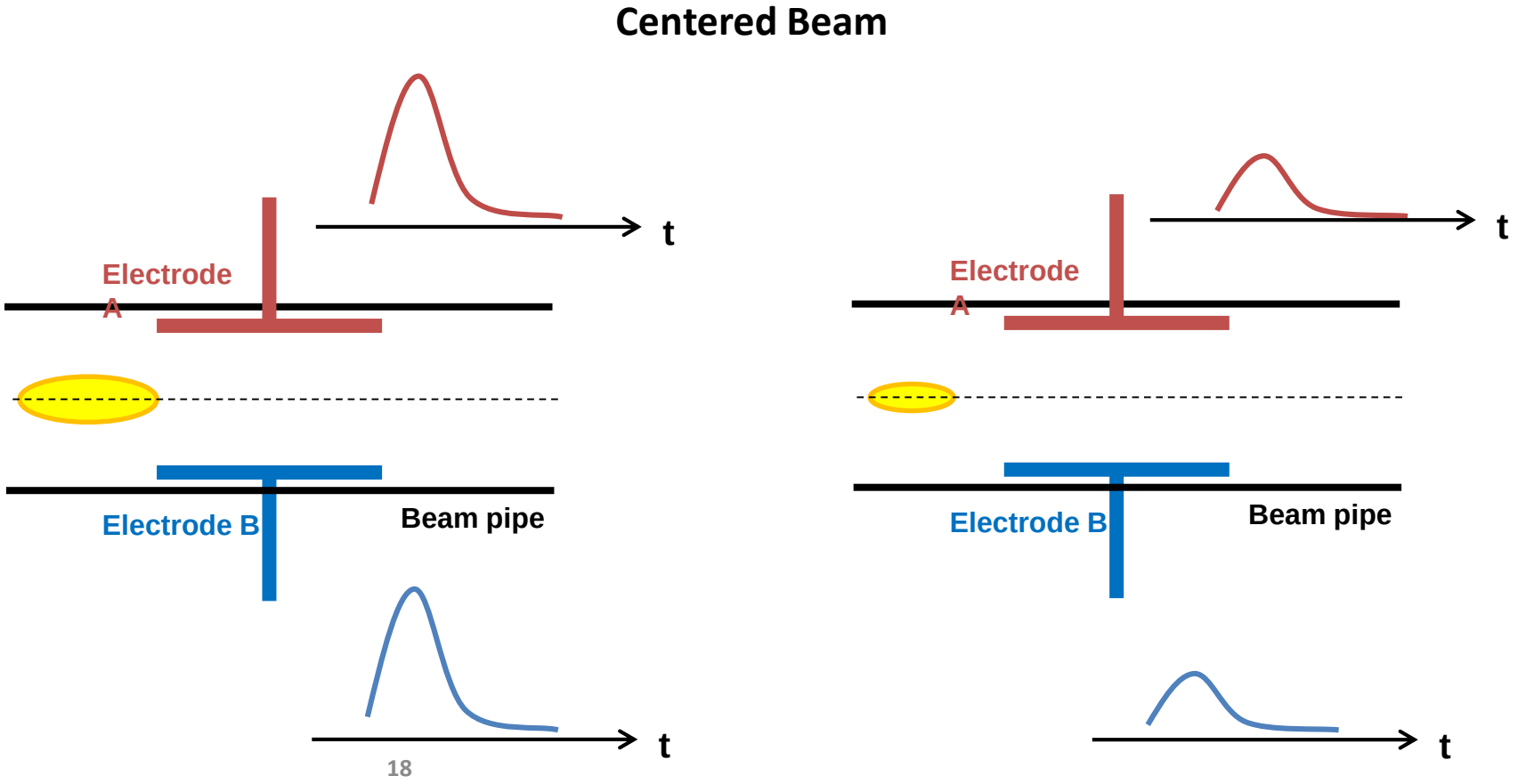


Image of an electrostatic pick-up

Electronics @ CERN

Sensors

Beam Position Monitor

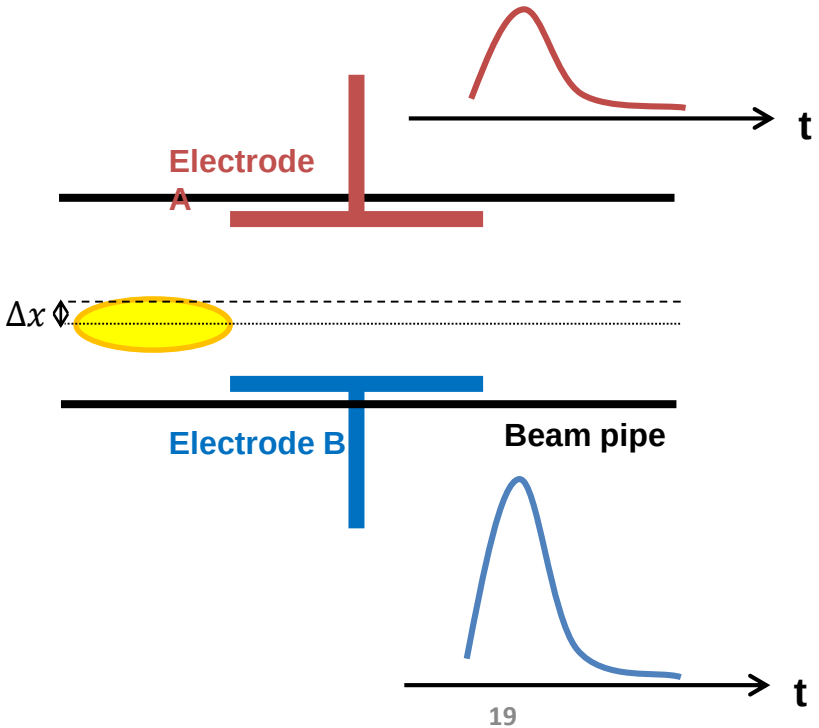


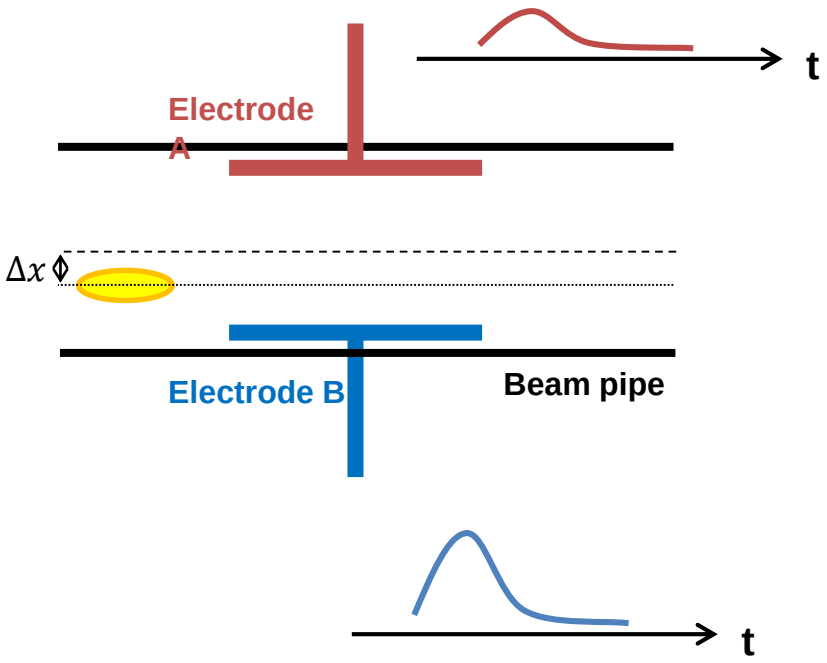
Electronics @ CERN

Sensors

Beam Position Monitor

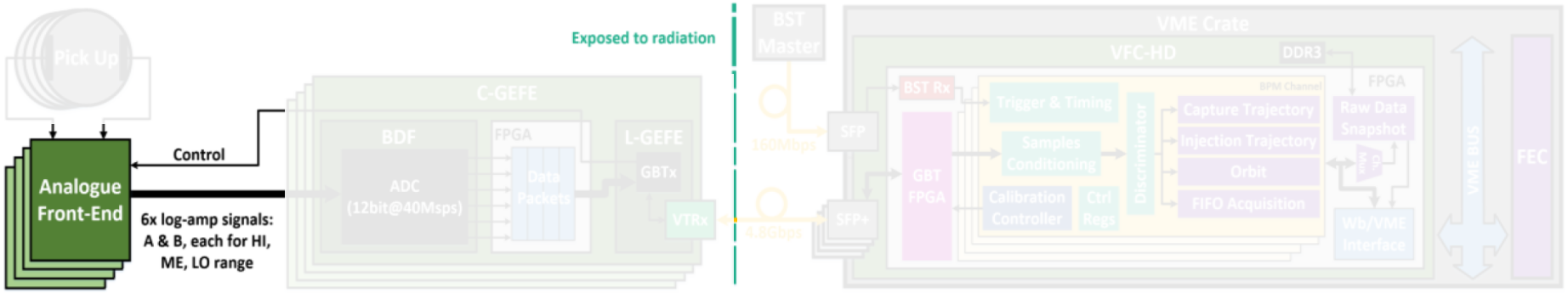
Displaced Beam





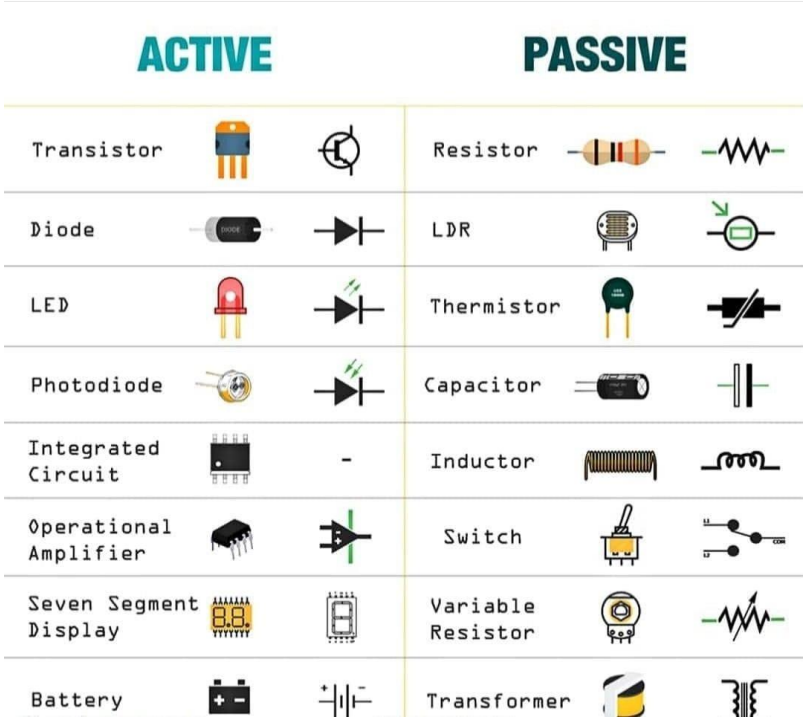
Electronics @ CERN

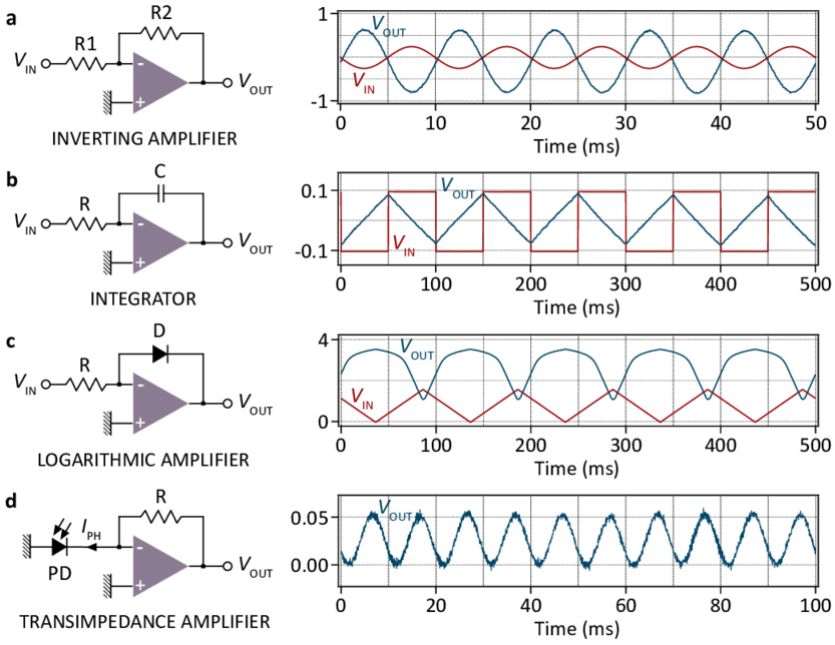
Analogue Front-End



Electronics @ CERN

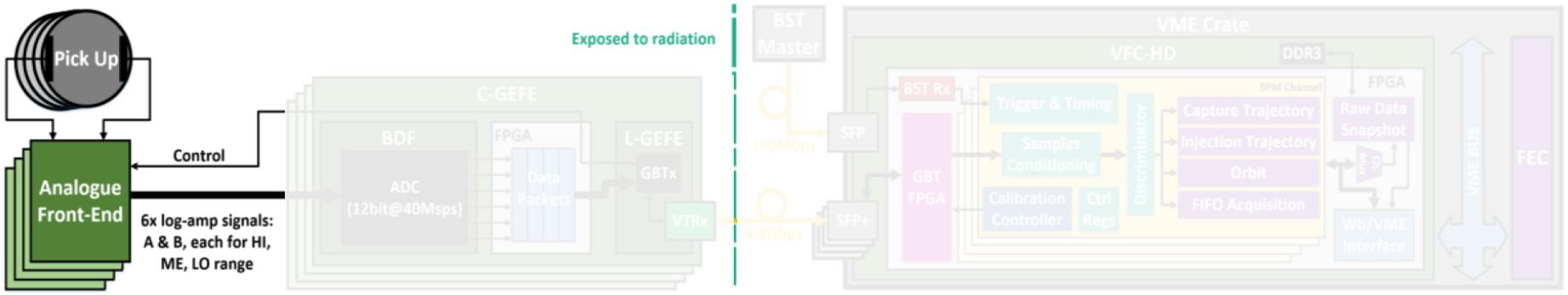
Analogue Front-End

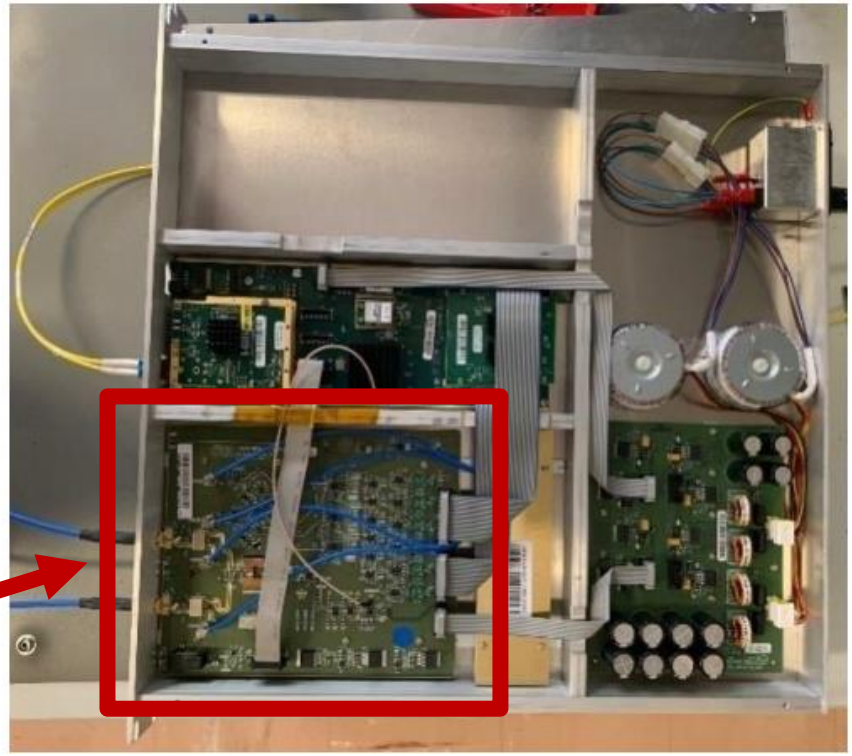




Electronics @ CERNC

Analogue Front-End

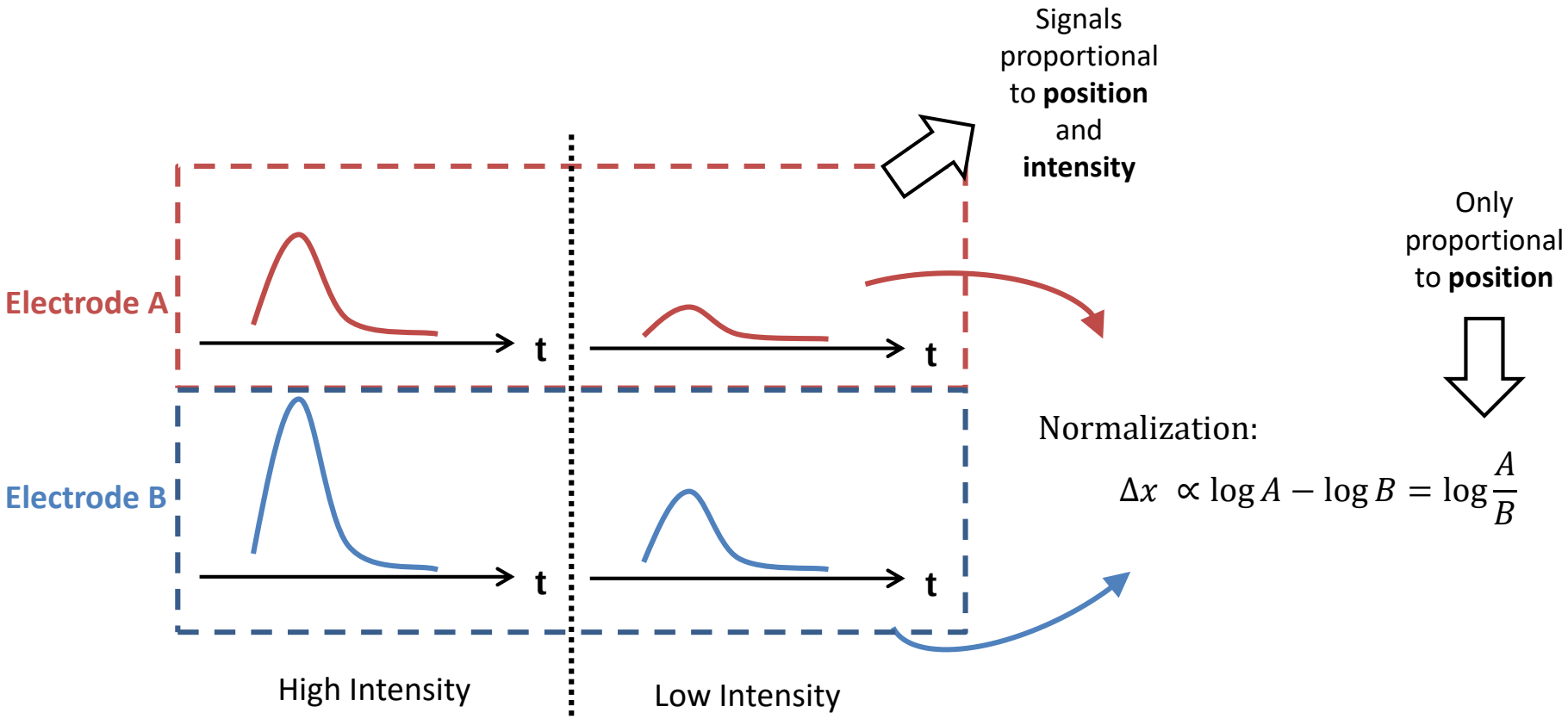




ALPS Analogue Front-End card (EDA-03730-V5-0)

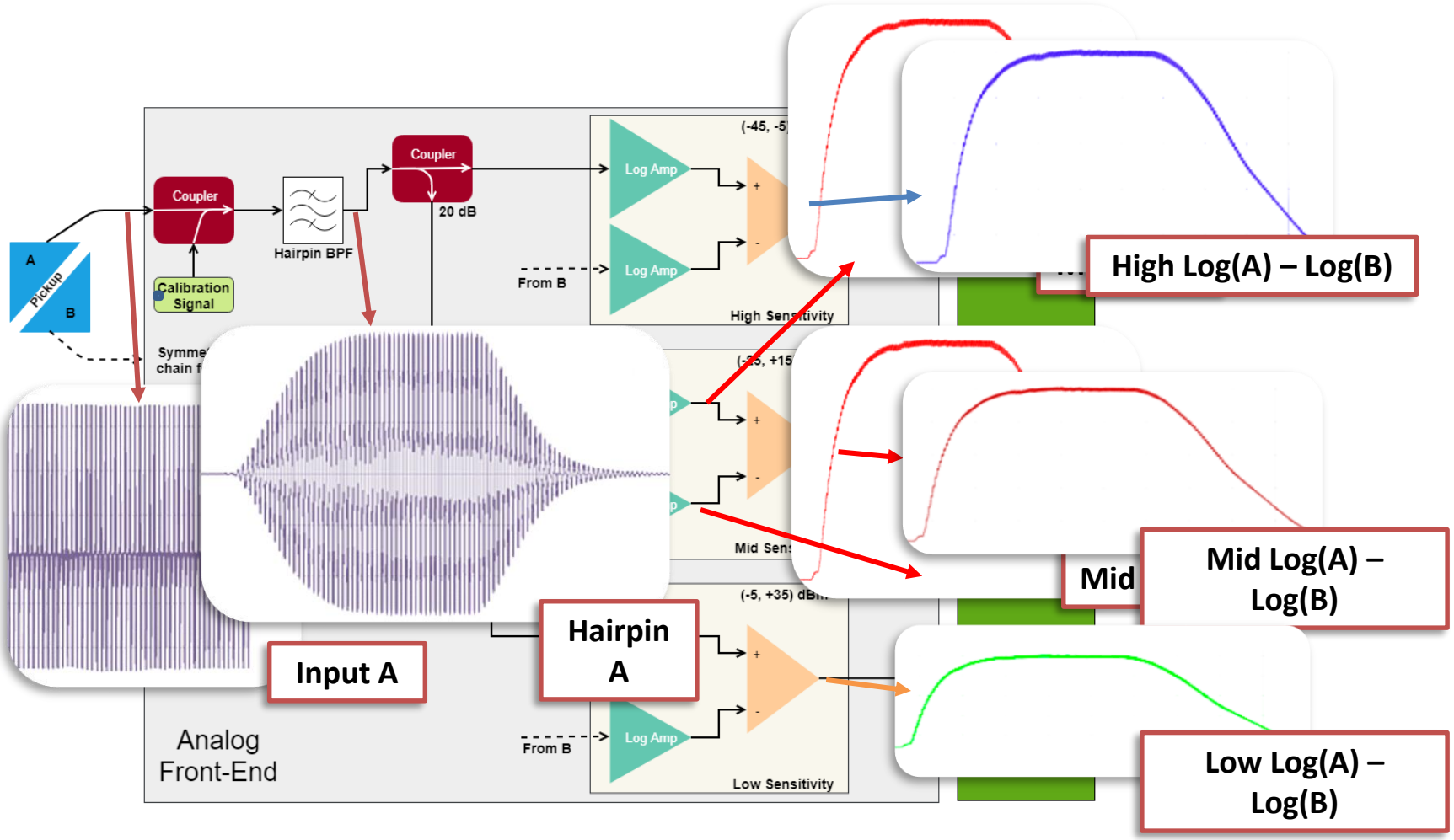
Electronics @ CERNC

Analogue Front-End



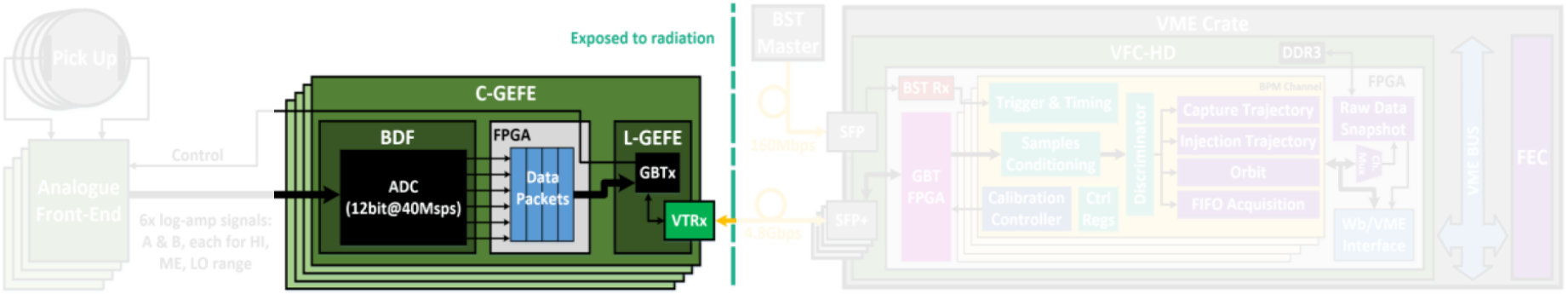
Electronics @ CERN

Analogue Front-End



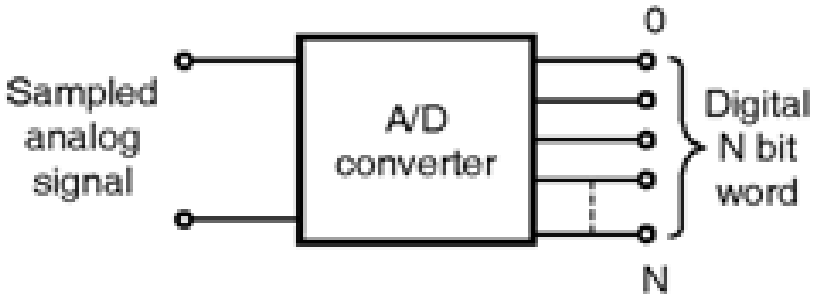
Electronics @ CERN

Digital Front-End

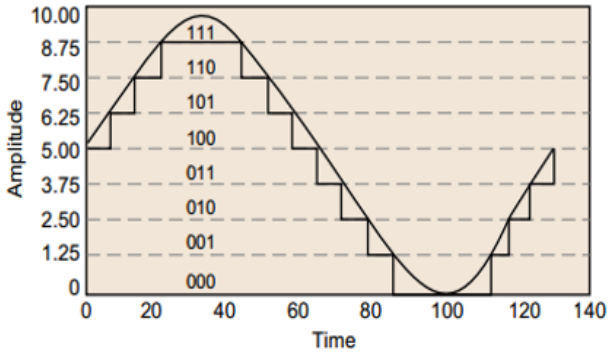


Electronics @ CERN

Digital Front-End



Voltage	Digitizer bits	Integer
0.00 - 1.25	000	0
1.25 – 2.50	001	1
2.50 - 3.75	010	2
3.75 – 5.00	011	3
5.00 - 6.25	100	4
6.25 – 7.50	101	5
7.50 – 8.75	110	6
8.75 – 10.00	111	7



Electronics @ CERN

Digital Front-End

Example of ADC: AD41240

- Rad-Hard design from CERN (EP-ESE)
- Pipelined Analogue-to-Digital Converter (ADC)
- 4 x 12-bit @ 40 Msps (or 1 x 14 @ 40 Msps)
- Differential analogue inputs & Parallel digital outputs
- Radiation Tolerance:
  - TID > 100 kGy (dose rate (X-rays): 333.3 Gy (SiO2)/min)
  - SEE > 3x10^8 p/cm2s (200 MeV proton beam)

AD41240

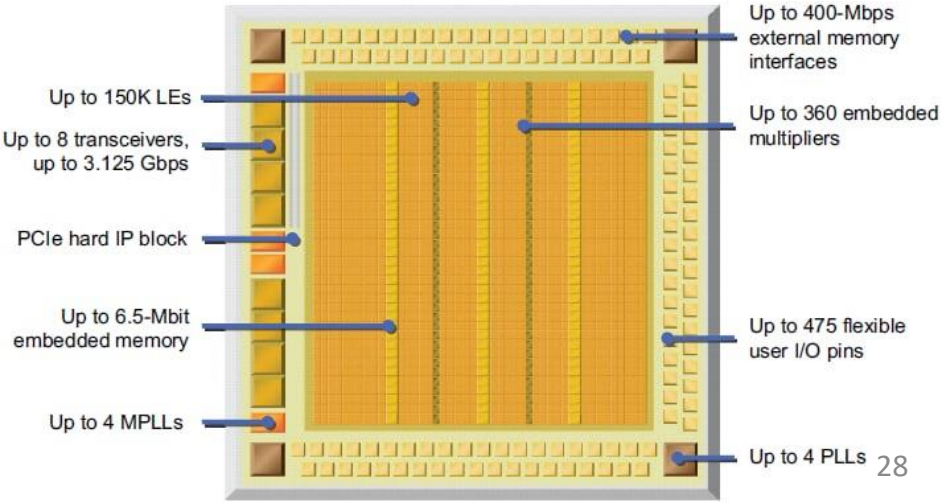
Electronics @ CERN

Digital Front-End

Field-Programmable Gate Array (FPGA)

- Like a ASIC that can be reprogrammed ☺
- Features logic elements (e.g. AND gate), registers, I/O blocks, PLLs, memories
  - But also features other dedicated hard-blocks (e.g. Multi-Gigabit Transceivers (MGT), DSP blocks)
  - Microprocessors may be implemented using logic elements and internal memory
- Volatile (SRAM-based) or Non-volatile (Flash-based) configuration memory
- Very common for interfacing (glue logic) and/or implementing COMPLEX processing cores
- Very good option for Real Time applications (capable of low, fixed and deterministic latency)
- VERY HIGH computing power for general purpose or specific applications
- Parallel processing

Example Diagram of FPGA



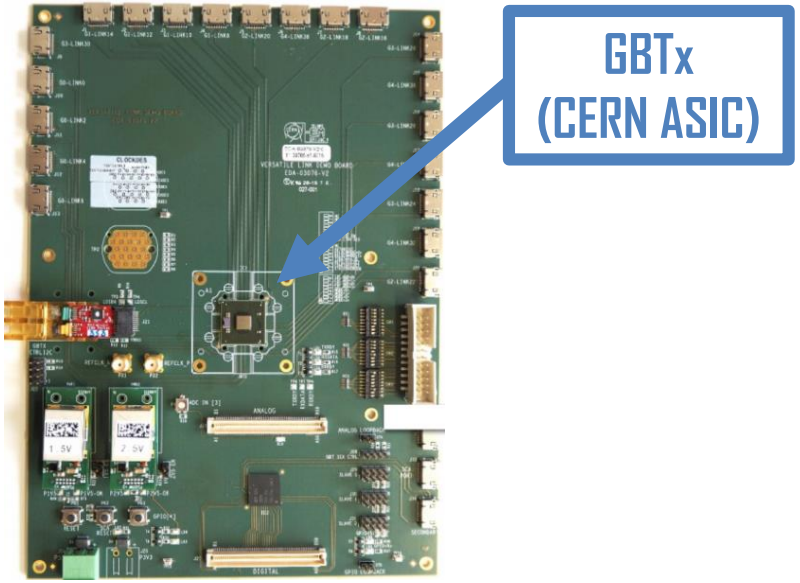
Electronics @ CERN

Digital Front-End

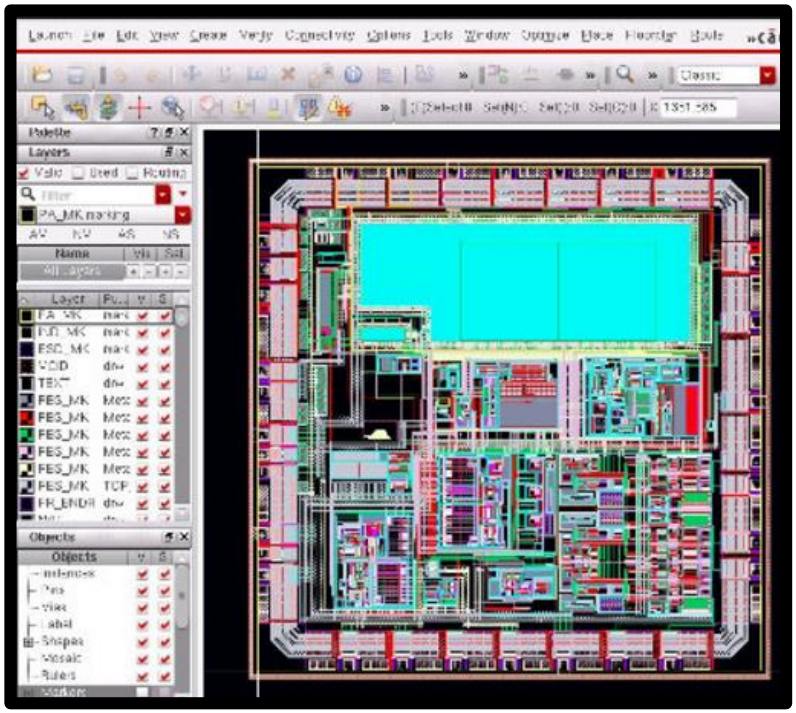
Application Specific Integrated Circuit (ASIC)

- Integrated circuit customised for a particular use, rather than intended for begin general purpose
- Used when COTS components do not suit the application
- May feature any type of peripherals (digital and/or analogue)
- Custom level of computing power
- Single/Multi-threaded and/or Parallel processing

Example of ASIC



Example of ASIC layout



Electronics @ CERN

Digital Front-End

Example of ASIC: GigaBit Transceiver (GBTx)

- Rad-Hard design from CERN (EP-ESE)
- Encoding Protocols:
  - Wide-Bus (No Error Detection)
  - GBT (FEC16 (Reed-Solomon))
- Line Rate:
  - Wide-bus protocol: 4.8. Gbps (4.56 Gbps payload: 114 bits @ 40MHz)
  - GBT protocol: 4.8 Gbps (3.28 Gbps payload: 82 bits @ 40 MHz)
- Latency Deterministic (Downstram/Upstream)
- Use for Data Readout & Timing, Trigger and Control
- Radiation Tolerance:
  - TID >1 MGy (dose rate (X-rays): 1 kGy (SiO2)/min)
  - SEE > 1x10^8 p/cm2s (36 MeV proton beam)

GBTx

Electronics @ CERN

Digital Front-End

Serial Link

Electronics @ CERN

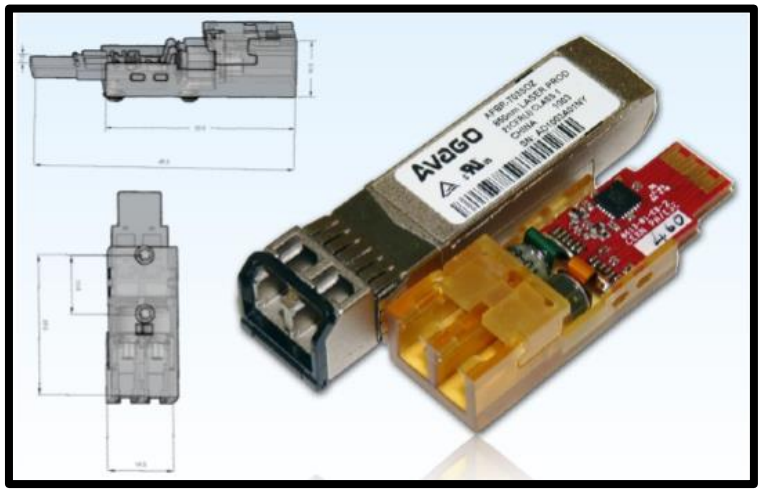
Digital Front-End

Serial Link

Example of Optical Transceiver Versatile Link (VTRx):

- Rad-Hard design from CERN (EP-ESE)
- Line Rate:
  - Up to 5.0 Gbps
- Transmission/Reception modes:
  - Full-Duplex (Rx/Tx): VTRx
  - Dual Transmitter (Tx/Tx): VTTx
- Optical transmission:
  - Multi-mode (MM VTRx / MM VTTx) (850 nm)
  - Single-mode (SM VTRx) (1310 nm)
- Radiation Tolerance:
  - TID > 500 kGy (5x10^14 n/cm2)

VTRx vs SFP+ form factors



(Diagram courtesy of Jan Troska (CERN EP-ESE))

Electronics @ CERN

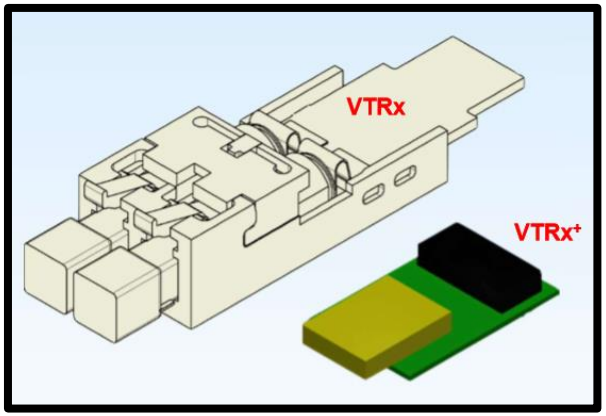
Digital Front-End

Serial Link

Another example of Optical Transceiver:
Versatile Link PLUS (VTRx+)

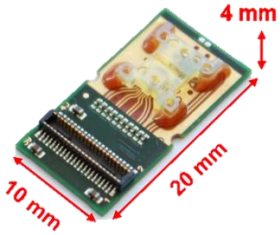
- Rad-Hard design from CERN (EP-ESE)
- Line Rate:
  - Tx: Up to 10.0 Gbps
  - Rx: Up to 2.5 Gbps
- Transmission/Reception modes:
  - Up to 4 Tx + Up to 1 Rx
- Optical transmission:
  - Multi-mode only (850nm VCSEL)
- Radiation Tolerance:
  - TID >1 MGy (5x10^15 hadrons/cm2)

VTRx vs VTRx+ form factor



(Diagram courtesy of Francois Vasey (CERN EP-ESE))

VTRx+ dimensions

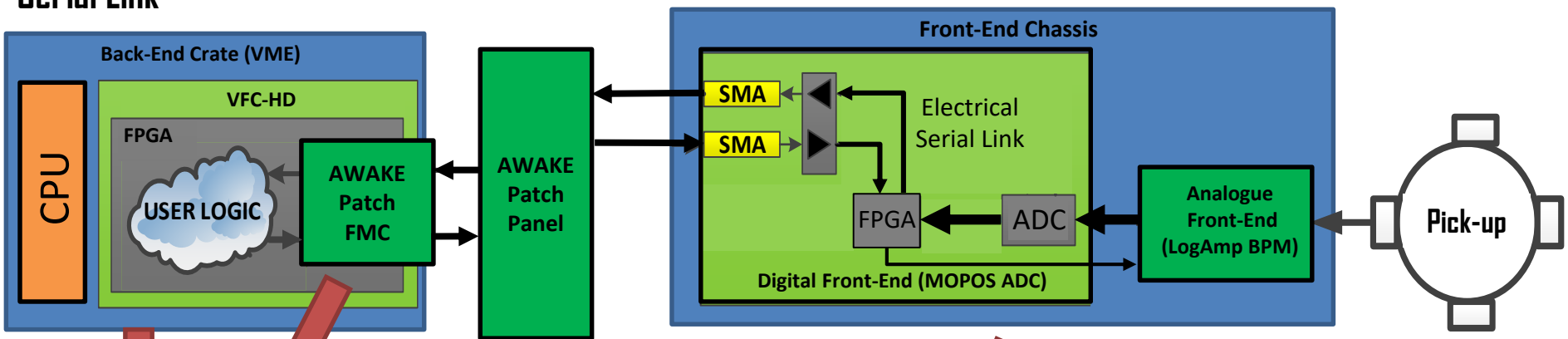


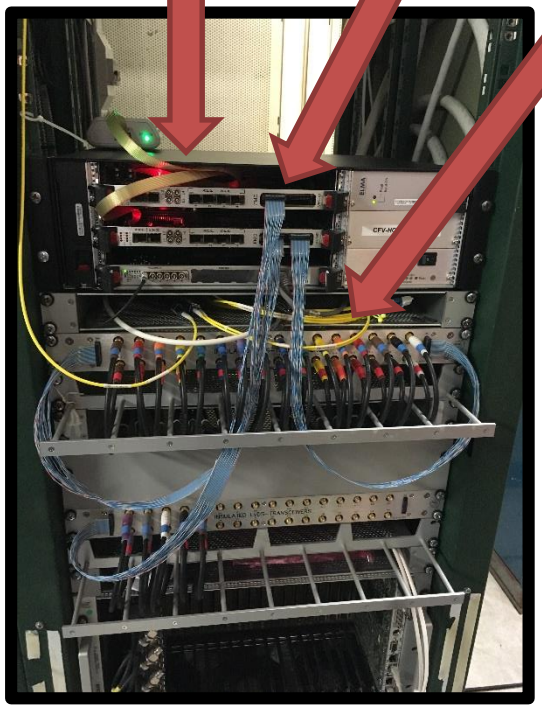
Electronics @ CERN

Digital Front-End

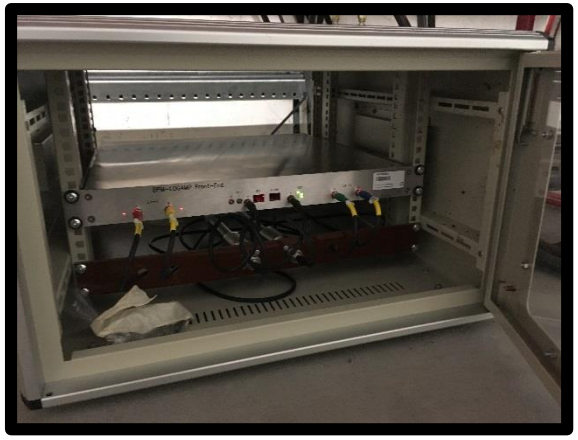
Serial Link

Example of Electrical Link: AWAKE Proton BPM



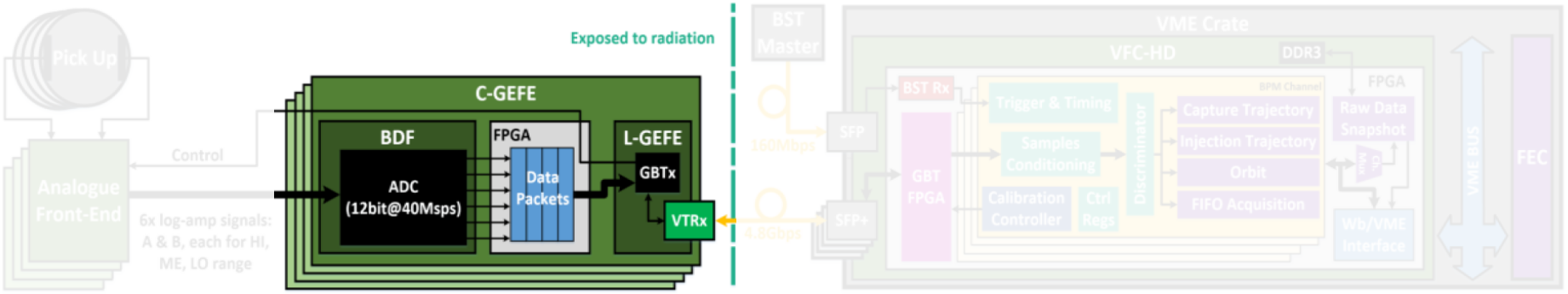


Electrical Serial Link
(10Mbps over 1km of copper cable)



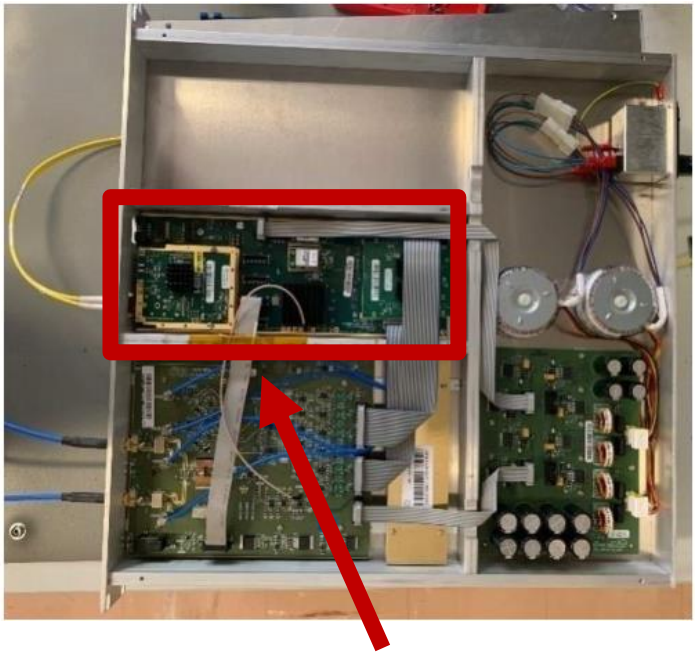
Electronics @ CERN

Digital Front-End



Bpm Digital front-end Fmc (BDF) (EDA-03134-V2-2)

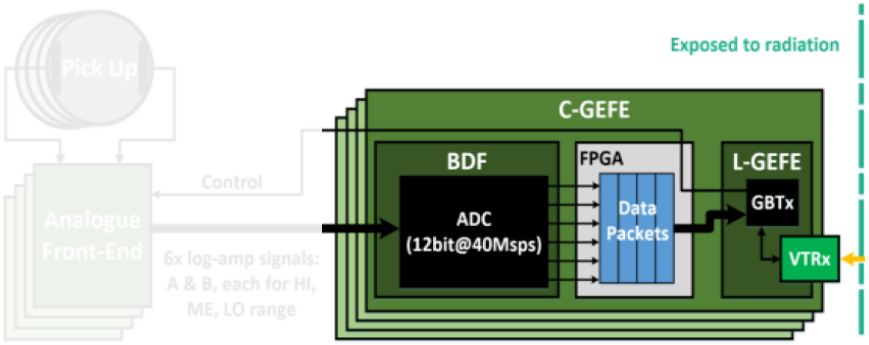
S-GEFE: L-GEFE (EDA-03683-V2-0) and C-GEFE (EDA-03684-V2-0)

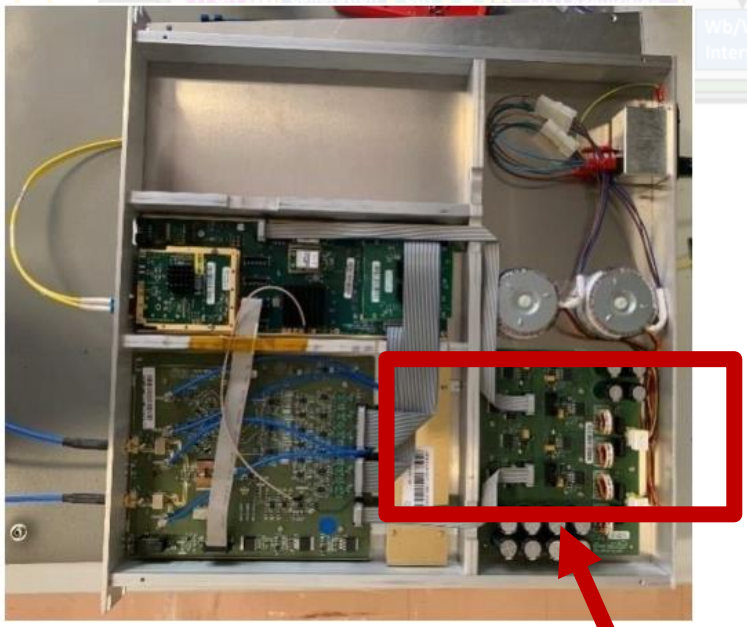


Digital Front-End

Electronics @ CERN

Front-End Power Supply





Power Supply

Electronics @ CERN

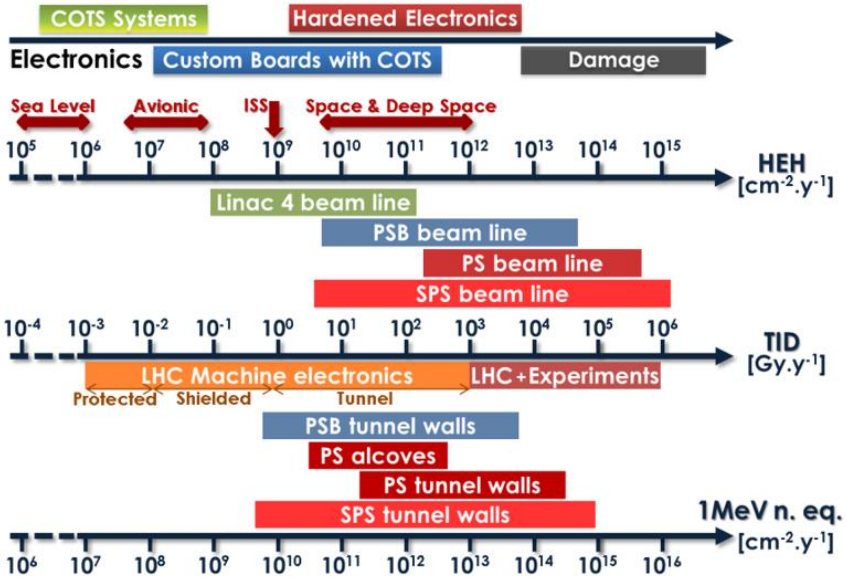
Front-End Power Supply

Linear Voltage Regulator		Switching Voltage Regulator	
Pros	Cons	Pros	Cons
Simple circuit configuration	Relatively poor efficiency	High efficiency	More external parts required
Few external parts	Considerable heat generation	Low heat generation	Complicated design
Low noise	Only step-down (buck) operation	Boost/buck/ negative voltage operation possible	Increased noise

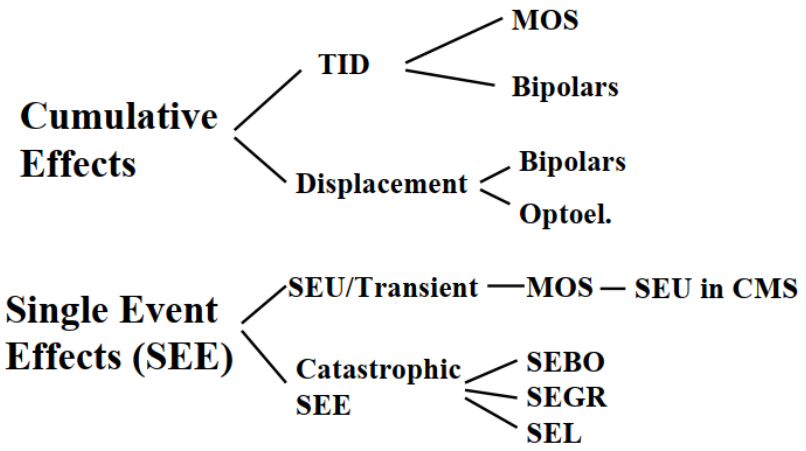
Electronics @ CERN

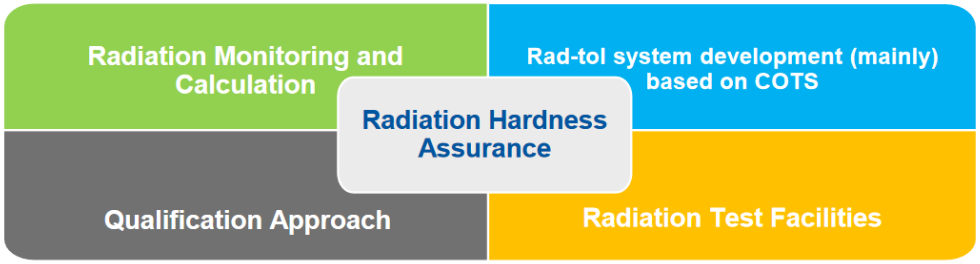
Radiation to Electronics (R2E)

Radiation Levels



Radiation Effects

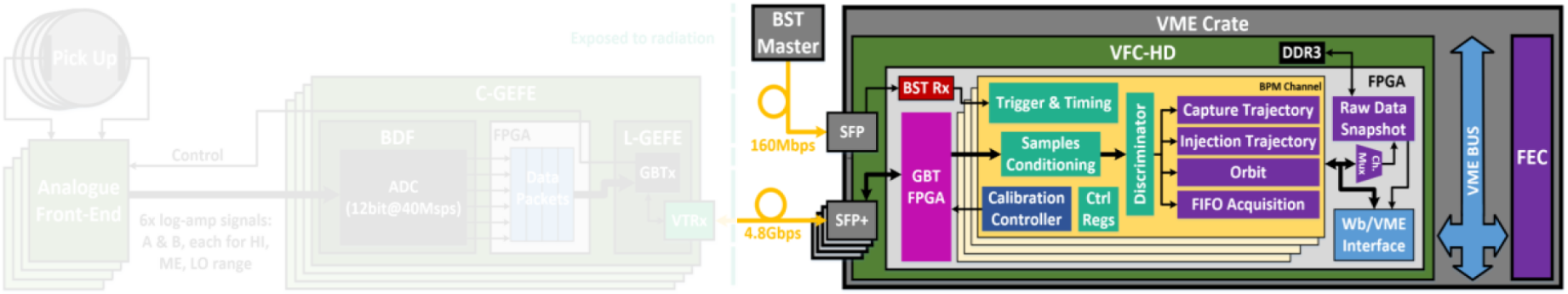




mitigation → prevention

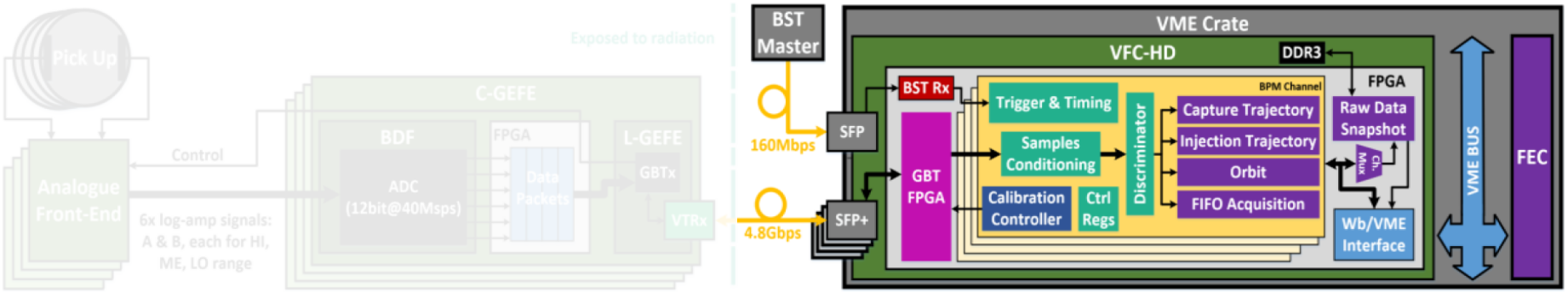
Electronics @ CERN

Back-End

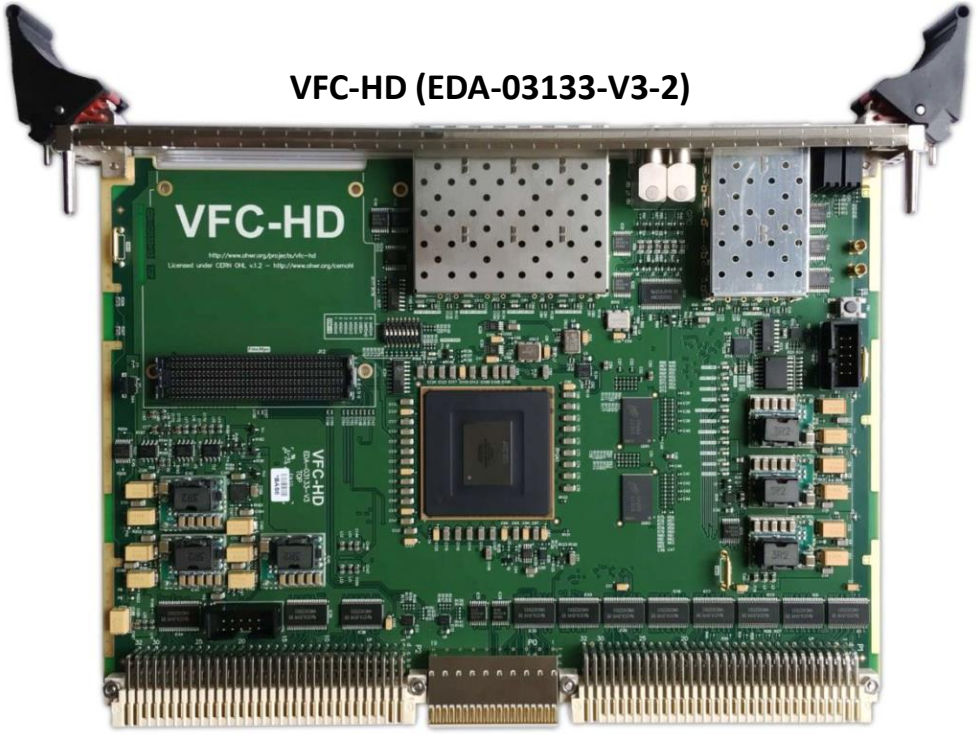


Electronics @ CERN

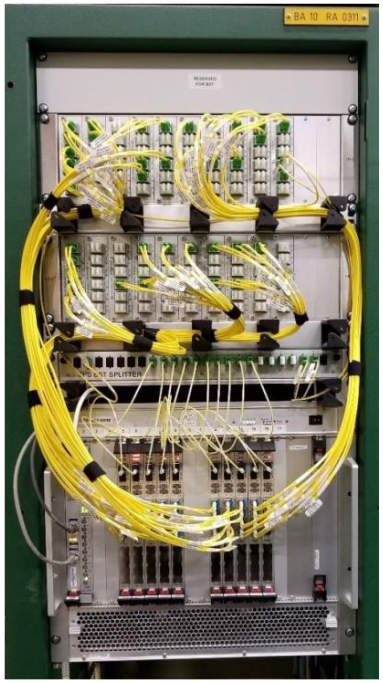
Back-End



VFC-HD (EDA-03133-V3-2)



Back-End Electronics of the ALPS on VME crate

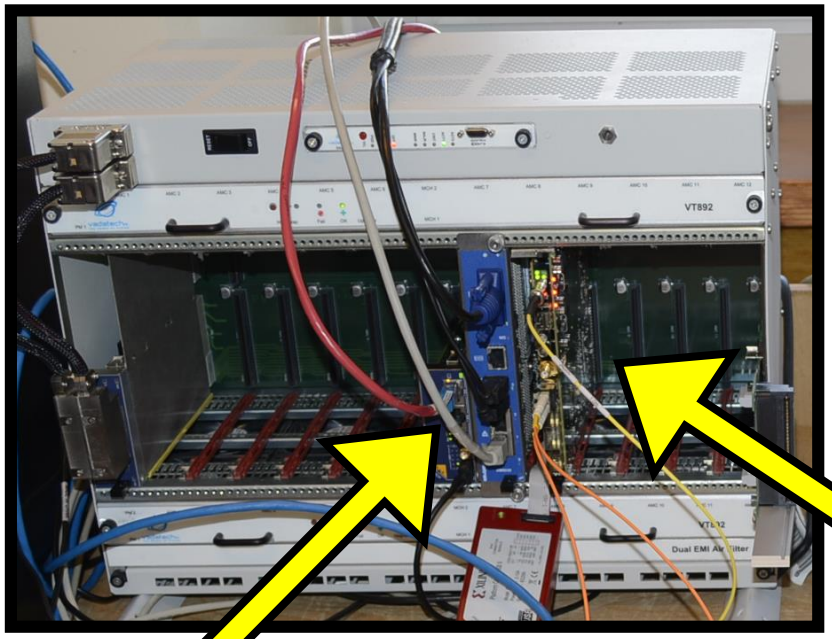


Electronics @ CERN

Back-End

Another example of modular electronics: MTCA-based

MTCA shelf



BE System

TTC FMC

GLIB AMC

SFP+

DAQ

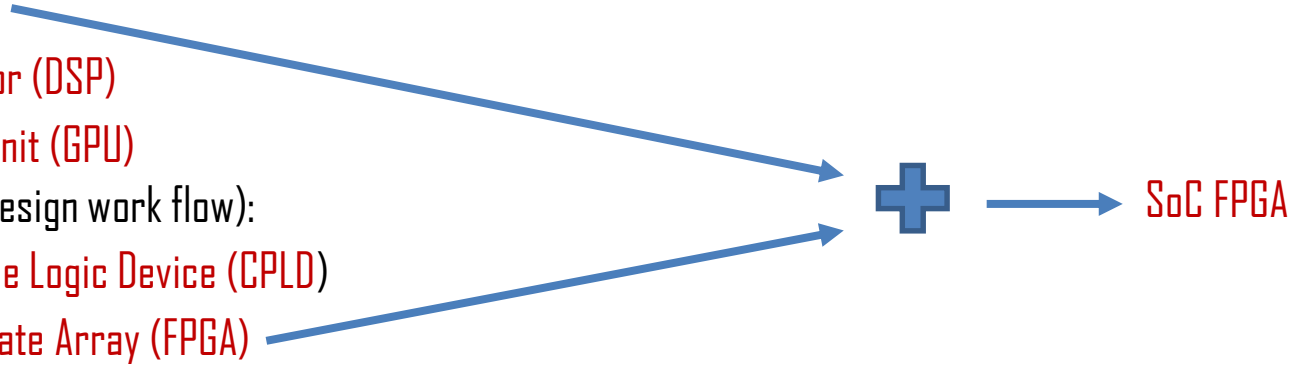
AMC Processor

HardWorking Core in Electronic Systems

- **Device in charge of the control tasks and/or data processing of an electronic system**

Typical HardWorking Cores in Electronic Systems

- **Commercial-Off-The-Shelf (COTS):**
  - Fixed Architecture (Software design work flow):
    - MicroProcessor (µP)
    - MicroController Unit (MCU)
    - System On Chip (SoC)
    - Digital Signal Processor (DSP)
    - Graphics Processing Unit (GPU)
  - Configurable Logic (Logic design work flow):
    - Complex Programmable Logic Device (CPLD)
    - Field-Programmable Gate Array (FPGA)
- **Custom design (Microelectronics design work flow):**
  - Application Specific Integrated Circuit (ASIC)



Electronics @ CERN

HardWorking Core in Electronic Systems

Comparison of typical of HardWorking Cores in Electronic Systems (1 of 2)

Device	Functionality	Main Application	Architecture	Processing	Computing Power	Design Work Flow	Cost Range	Real Time	Form Factor
uP	General Purpose	Computers	Fixed	Single/Multi-thread	High	Software	Mid-High	No	?
MCU	General Purpose	Low-Mid Range ES	Fixed	Single-thread	Low	Software	Low	Yes	?
SoC	General Purpose	Mid-High Range ES	Fixed	Single/Multi-thread	High	Software	Low-Mid	Yes	?
DSP	Application Specific	Digital Signal Processing	Fixed	Single/Multi-thread	High	Software	Low-Mid	Yes	?
GPU	Application Specific	Intensive Processing	Fixed	Multi-thread	High	Software	Mid-High	No	?

Electronics @ CERN

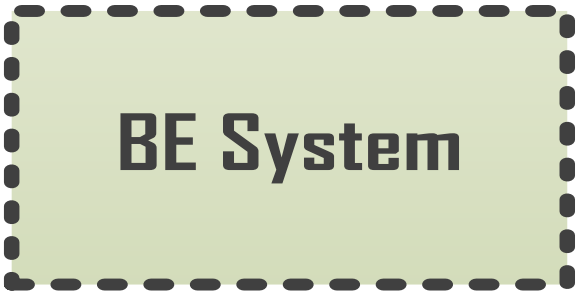
HardWorking Core in Electronic Systems

Comparison of typical of HardWorking Cores in Electronic Systems (2 of 2)

Device	Functionality	Main Application	Architecture	Processing	Computing Power	Design Work Flow	Cost Range	Real Time	Form Factor
CPLD	General Purpose / Application Specific	Glue Logic, Basic Processing	Configurable	Parallel	Low	Logic Design	Low	Yes	?
FPGA	General Purpose / Application Specific	Glue Logic, Control, Intensive Processing	Configurable	Parallel	High	Logic Design	Mid-High	Yes	?
SoC FPGA	General Purpose / Application Specific	Glue Logic, Mid-High Range ES	Fixed & Configurable	Single/Multi-thread & Parallel	High	Software & Logic Design	Mid-High	Yes	?
ASIC	Application Specific	Multiple Applications	Custom	Custom	Custom	ASIC	Based On Order Size	Yes	?

Electronics @ CERN

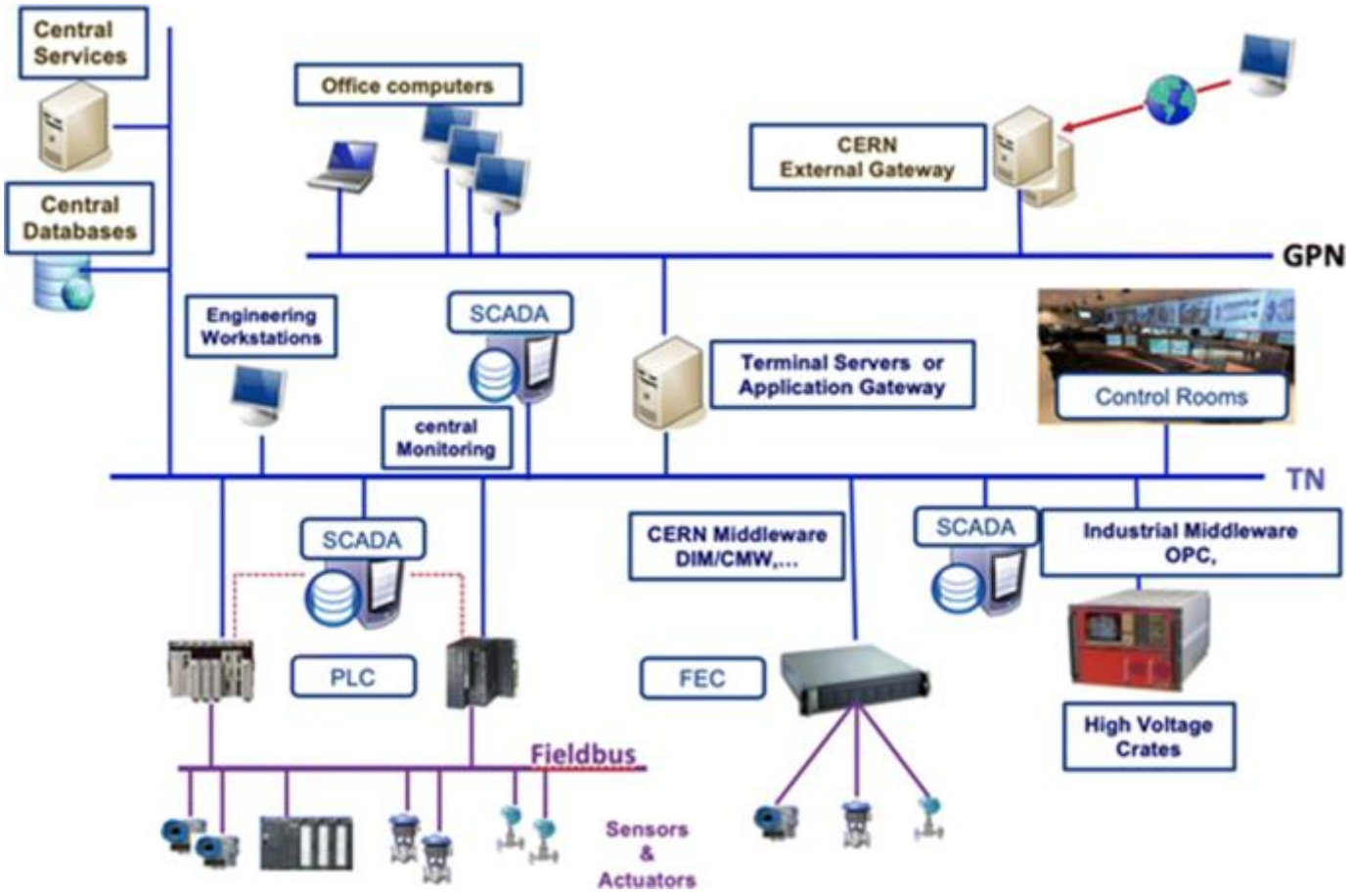
Timing, Trigger & Control



Standard TTC system

Electronics @ CERN

CERN Network & Data Storage



Electronic Engineering @ CERN

BL4S 2022

(28/09/2022)

Outline:

- Introduction
- Electronics @ CERN
- **Electronics Development**
- Summary

Manoel Barros Marin

Electronics Development

HardWare

Development Procedure

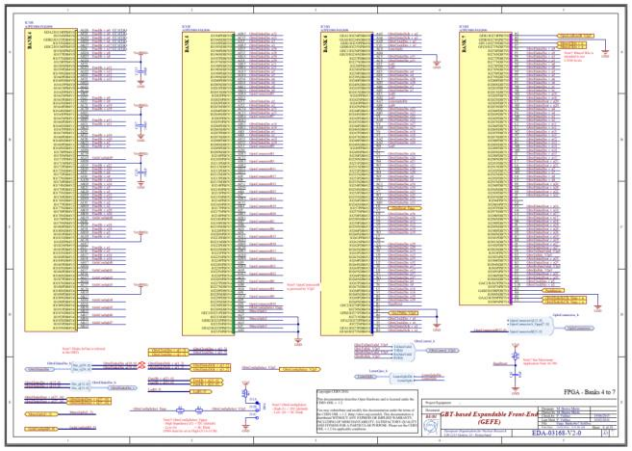
1. Specification
2. Schematics design
3. “Printed Circuit Board” (PCB) design
4. Simulation
5. Components procurement
6. Prototype production
7. Functional and Qualification (performance and radiation tolerance) tests
8. Production
9. Production tests

Electronics Development

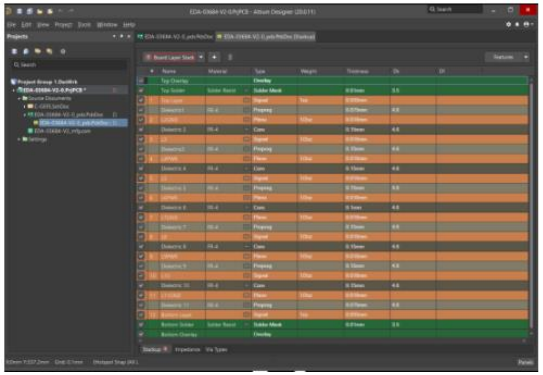
HardWare

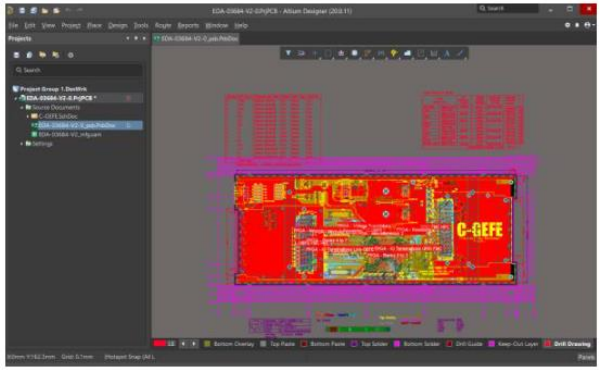
EDA Tools

Schematics



PCB



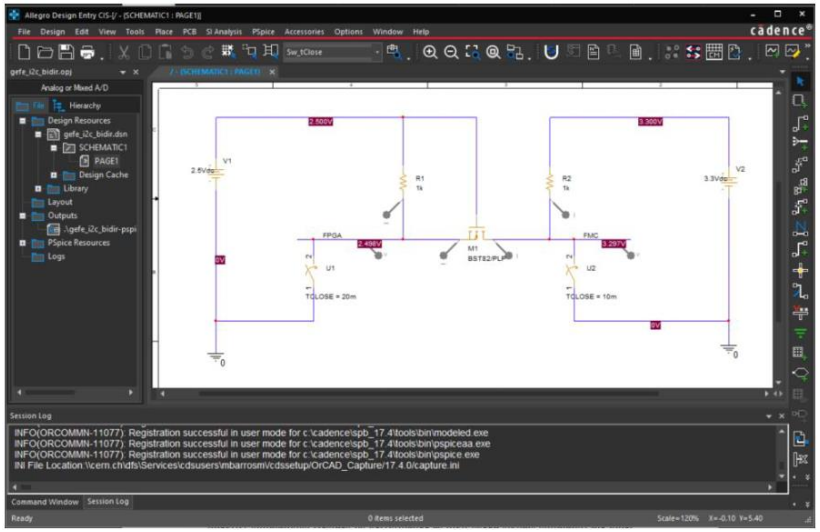


Electronics Development

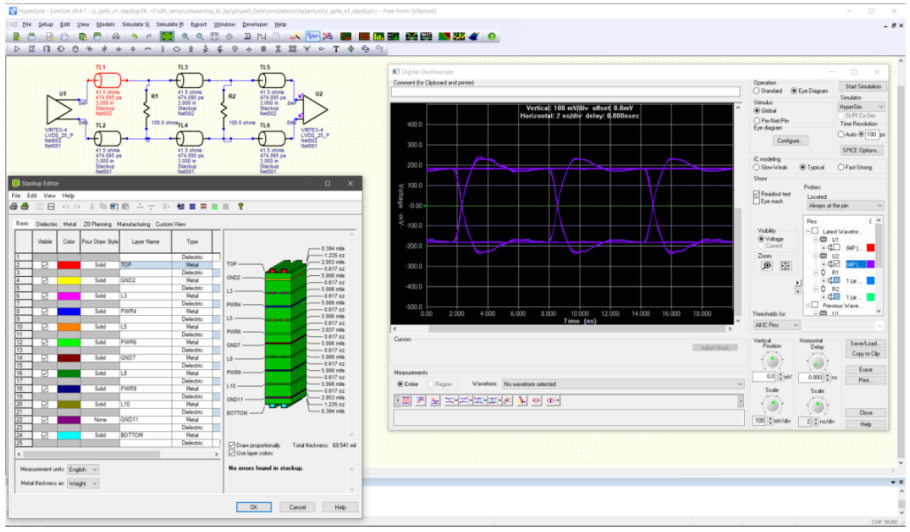
HardWare

Simulation

Critical parts with low/medium-speed signals in Spice-based simulator



Critical parts with high-speed signals in 3D Field Solver

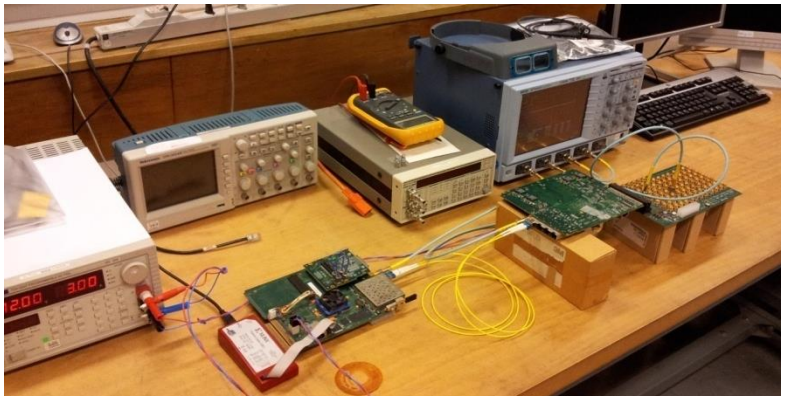


Electronics Development

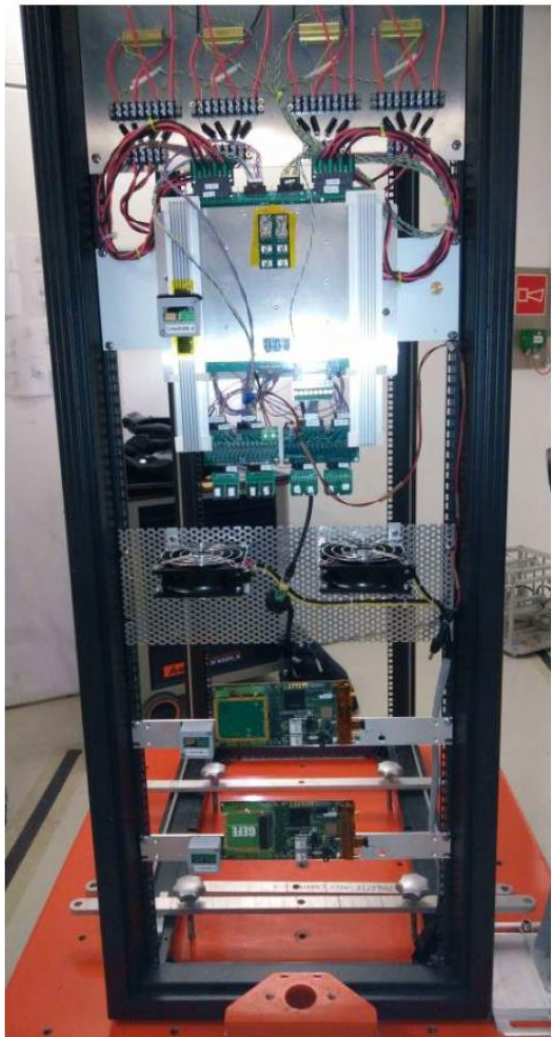
HardWare

Tests

Functional & Qualification Tests

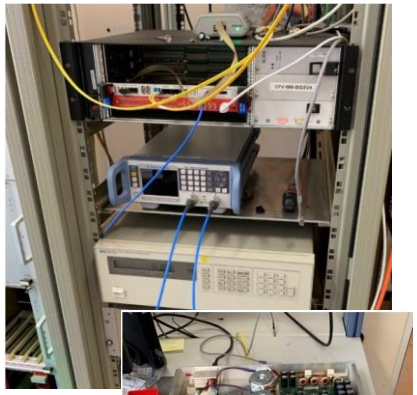


Radiation Tests



Production Tests

System Calibration



Electronics Development

FPGA GateWare

We are describing HARDWARE

Hardware Description Language (HDL)

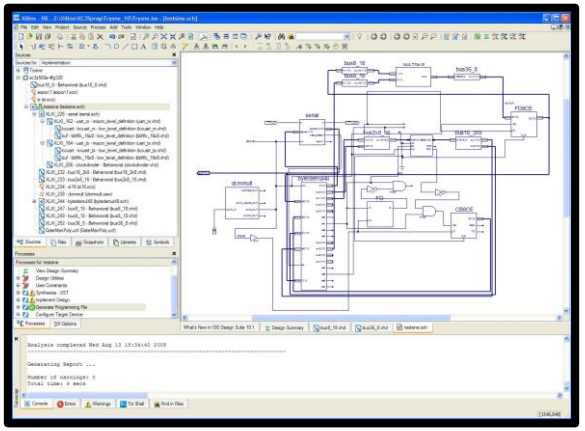
```
simple_delay_counter : process (delay_rst, delay_clk, delay_ena)
begin  -- process
  if delay_rst = '1' then
    s_count     <= delay_ld_value;
    s_delay_done <= '0';
  elsif rising_edge(delay_clk) then
    if delay_ena = '1' then
      if delay_ld = '1' then
        s_count <= delay_ld_value;
      else
        s_count <= s_count - 1;
      end if;
    end if;
    if s_count = 0 then
      s_delay_done <= '1';
    else
      s_delay_done <= '0';
    end if;
  end if;
end process;
```

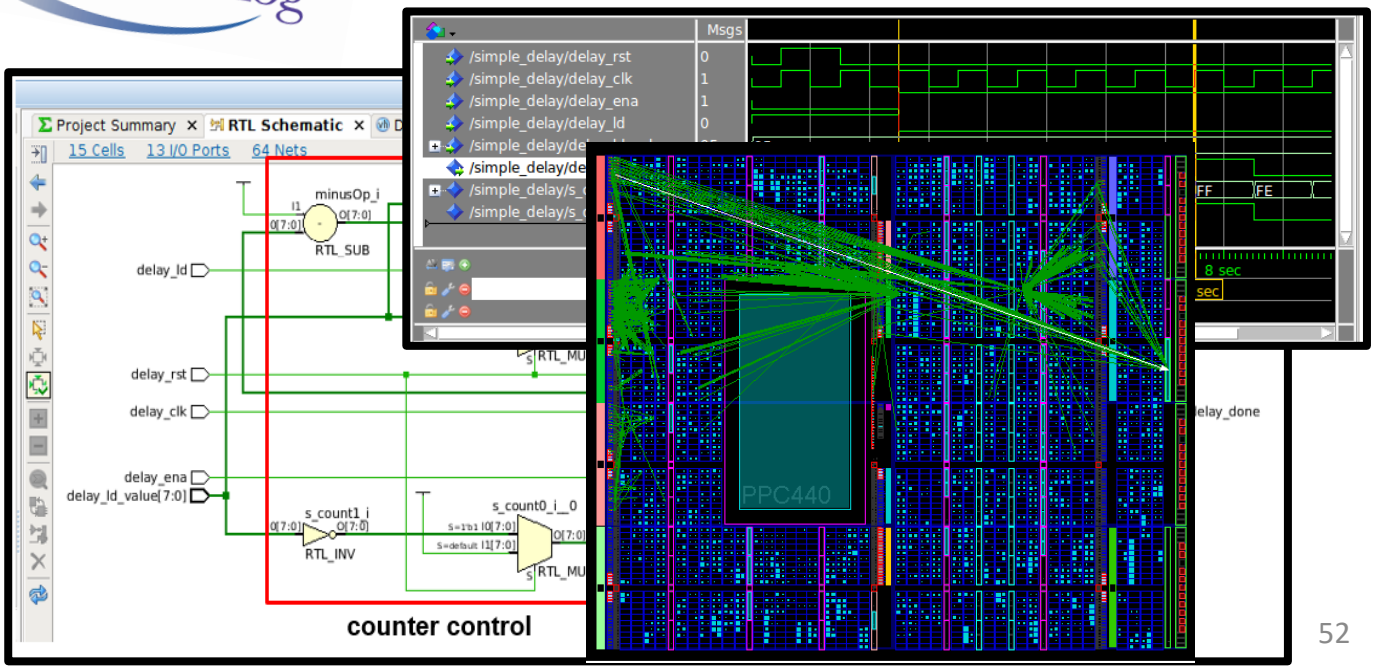
VHDL

SystemVerilog

HDL to RTL

Schematics





Electronic Engineering @ CERN

BL4S 2022

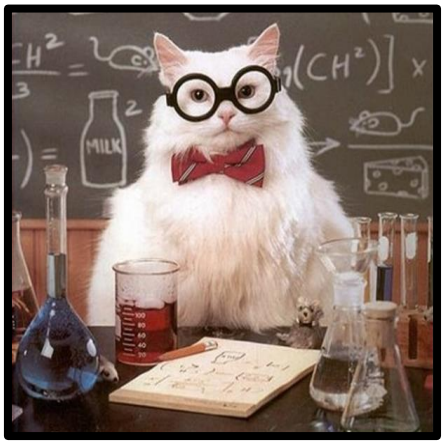
(28/09/2022)

Outline:

- Introduction
- Electronics @ CERN
- Electronics Development
- **Summary**

Manoel Barros Marin

Summary



- CERN offers nice challenges to students, graduates and professionals
- TDAQ are used in both Particle Accelerators and HEP experiments
- TDAQ covers a large variety of electronics
- At CERN we usually design our own electronics
- You can always contact me to discuss about this ☺: manoel.barros.marin@cern.ch

Any Question?

… from the previous lesson

What is an Field Programmable Gate Array (FPGA)?

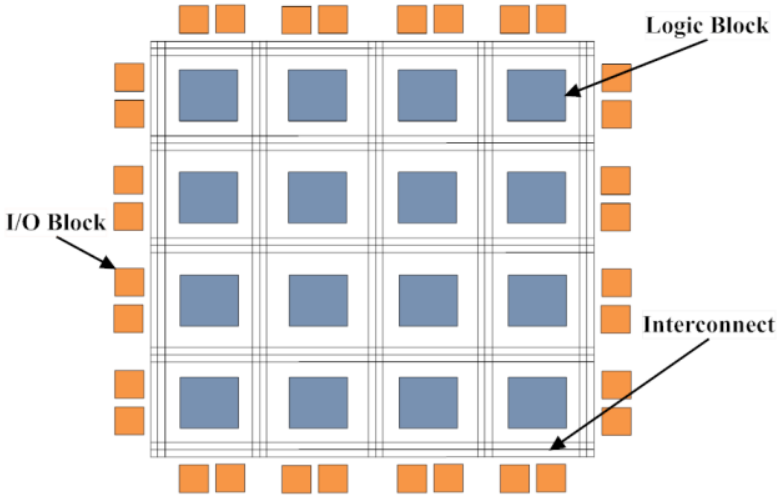
FPGA - Wikipedia

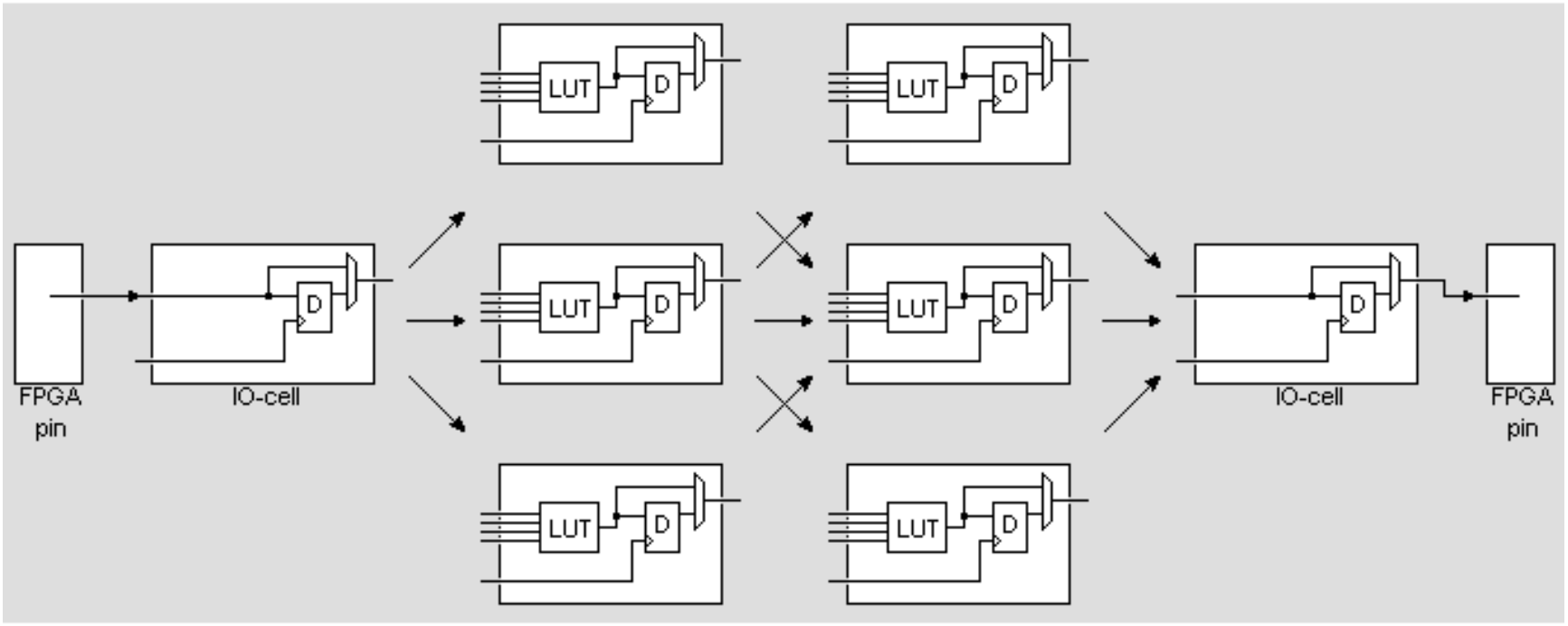
https://en.wikipedia.org/wiki/Field-programmable_gate_array

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence "field-programmable".

… from the previous lesson

- **FPGA fabric (matrix like structure) made of:**
  - I/O-cells to communicate with outside world
  - Logic cells
    - Look-Up-Table (LUT) to implement combinatorial logic
    - Flip-Flops (D) to implement sequential logic
  - Interconnect network between logic resources
  - Clock tree to distribute the clock signals

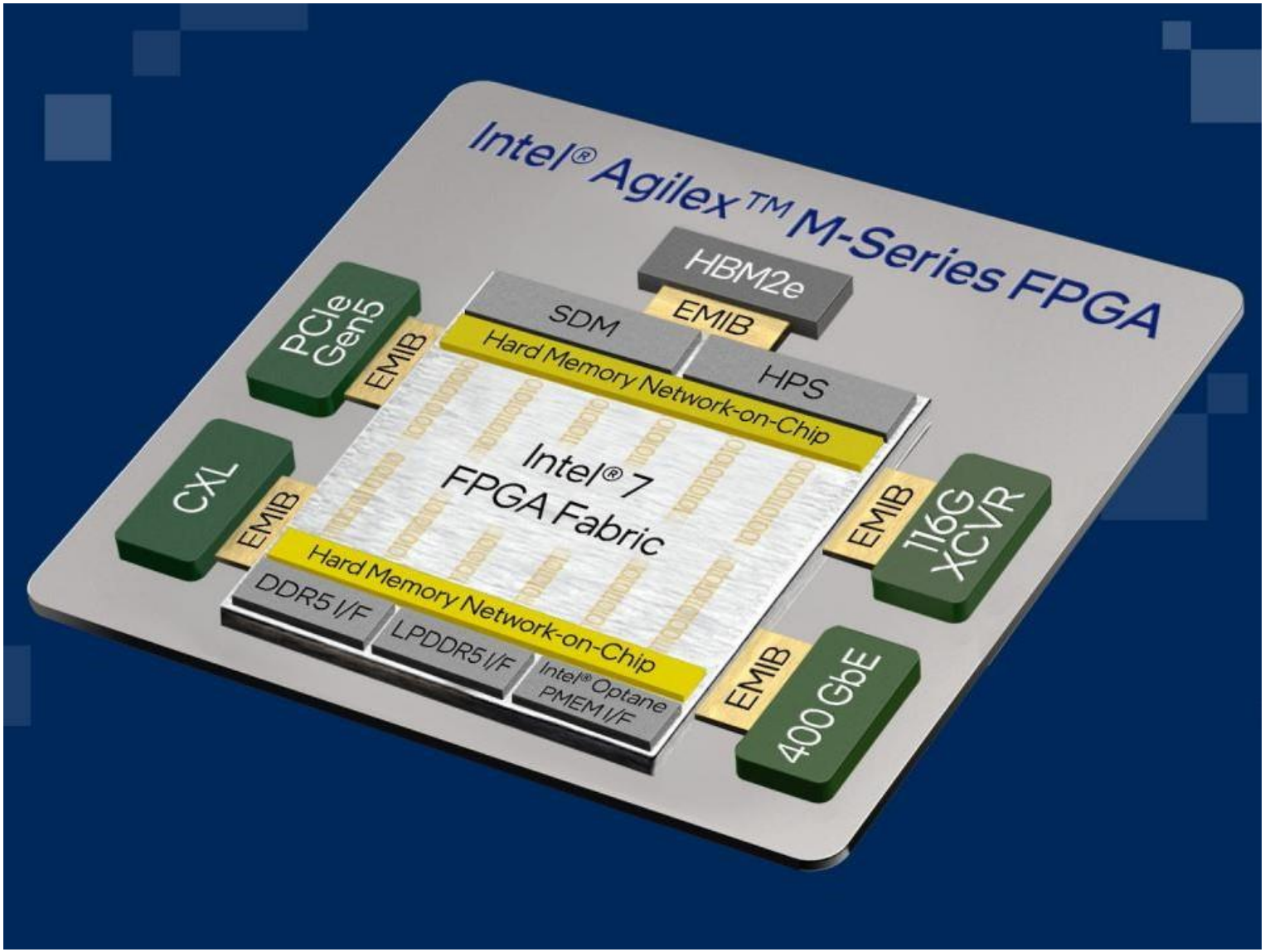




… from the previous lesson

- **But it also features Hard Blocks:**

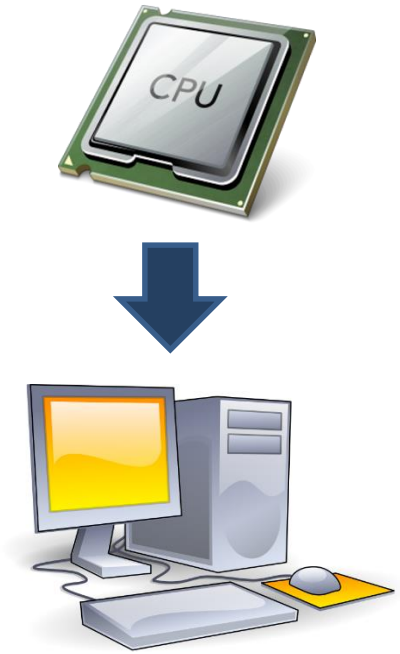
Example of FPGA architecture



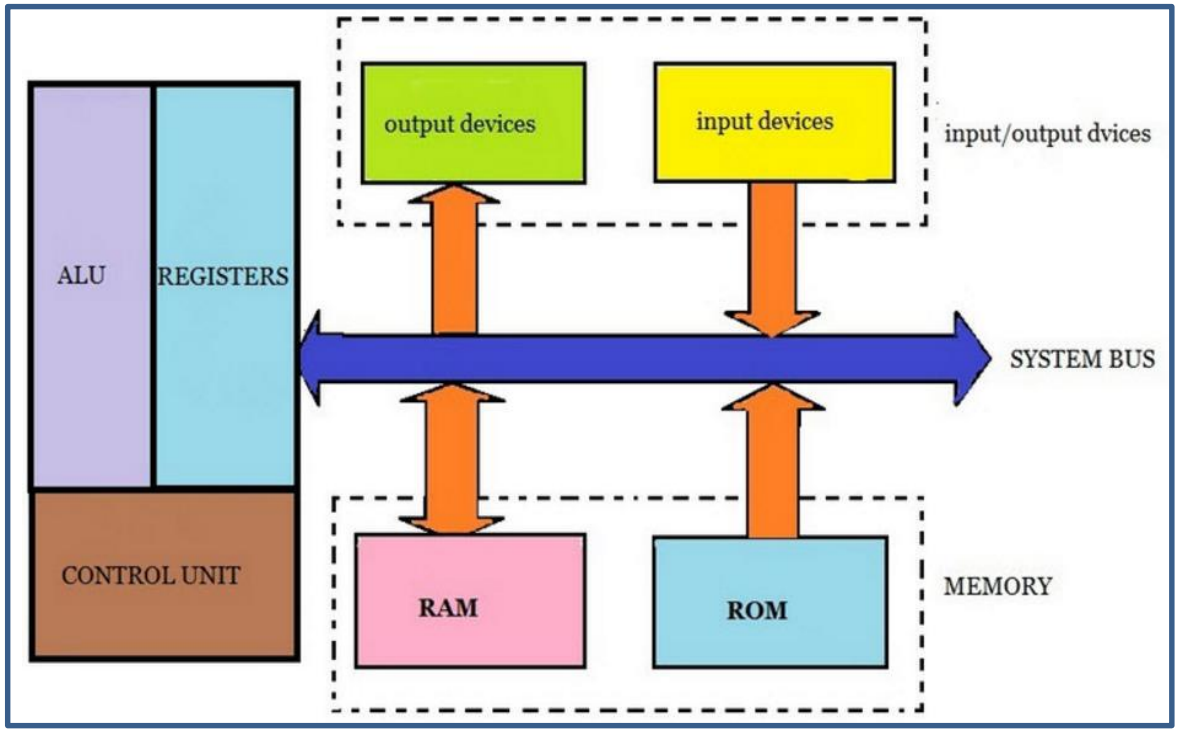
Introduction (4 of 13)

COTS: fixed architecture

- **Microprocessor (μP):**
  - Computer Central Processing Unit (CPU) on a single Integrated Circuit (IC) (e.g. Intel i7, AMD RYZEN)
  - Represents the core of a computer
  - HIGH computing power for general purpose applications
  - Single/Multi-thread processing



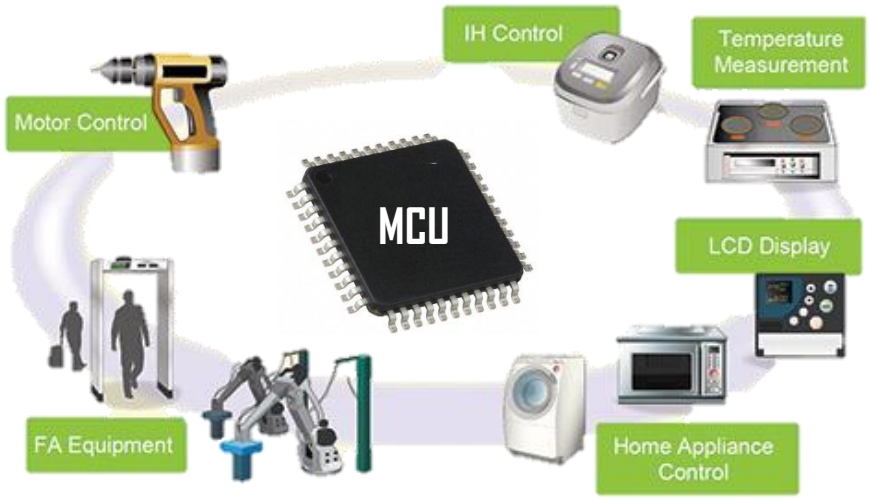
Example Diagram of Microprocessor



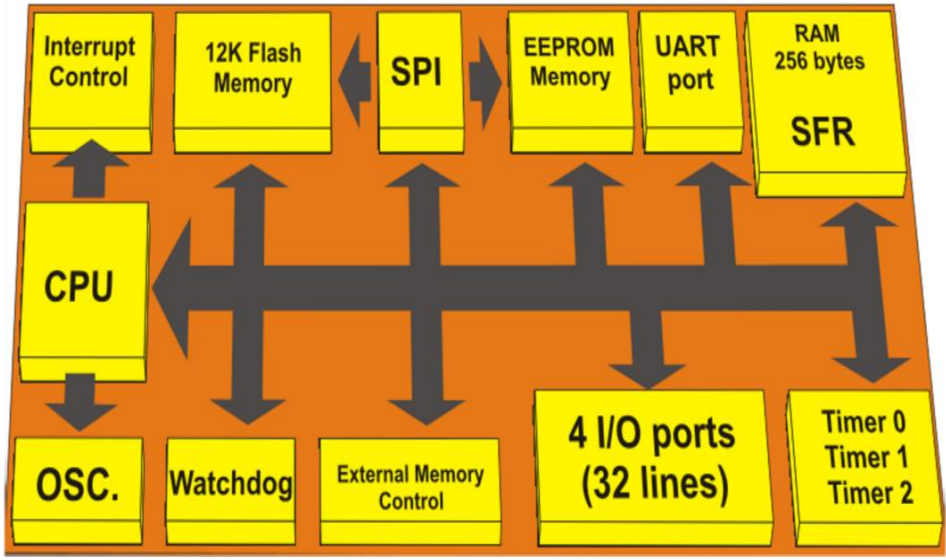
Introduction (5 of 13)

COTS: fixed architecture

- **Microcontroller (MCU):**
  - Small computer on a single integrated circuit (e.g. Atmel AT Mega, Microchip PIC)
  - Multiple peripherals (e.g. ADC, timer)
  - LOW computing power for general purpose applications (compared to µP)
  - May be used in Real Time applications (capable of low latency & Real Time Operating Systems (RTOS))
  - Very common in Embedded Systems (ES) (e.g. Arduino, modem, TV)
  - Single-thread processing



Example Diagram of Microcontroller

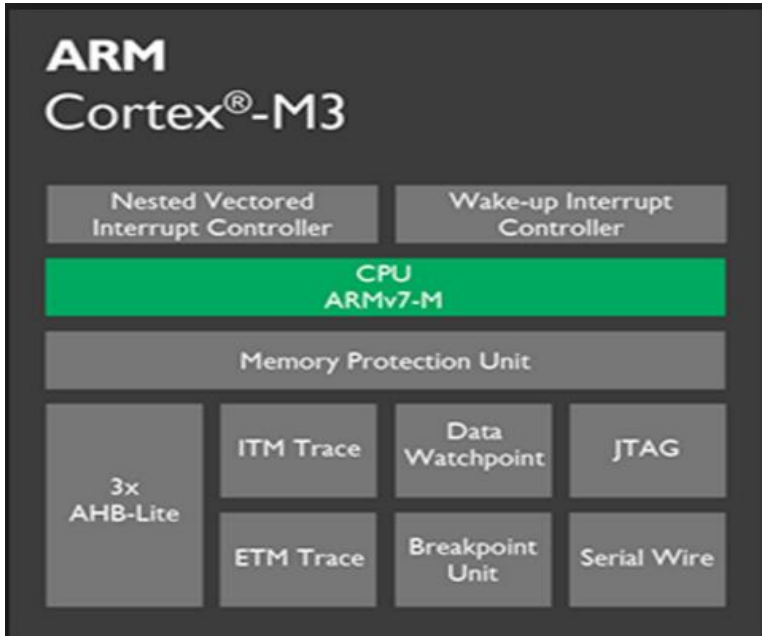


Introduction (6 of 13)

COTS: fixed architecture

- **System On Chip (SoC):**
  - Like a microcontroller with steroids ☺
  - ARM architecture has become standard
  - Multiple peripherals (e.g. GPU, DSP)
  - HIGH computing power for general purpose applications (capable to run Operating Systems (e.g. Linux))
  - May be used in Real Time applications (capable of low latency & Real Time Operating Systems (RTOS))
  - Very common in Embedded Systems (ES) (e.g. smartphones, tablet)
  - Single/Multi-thread processing

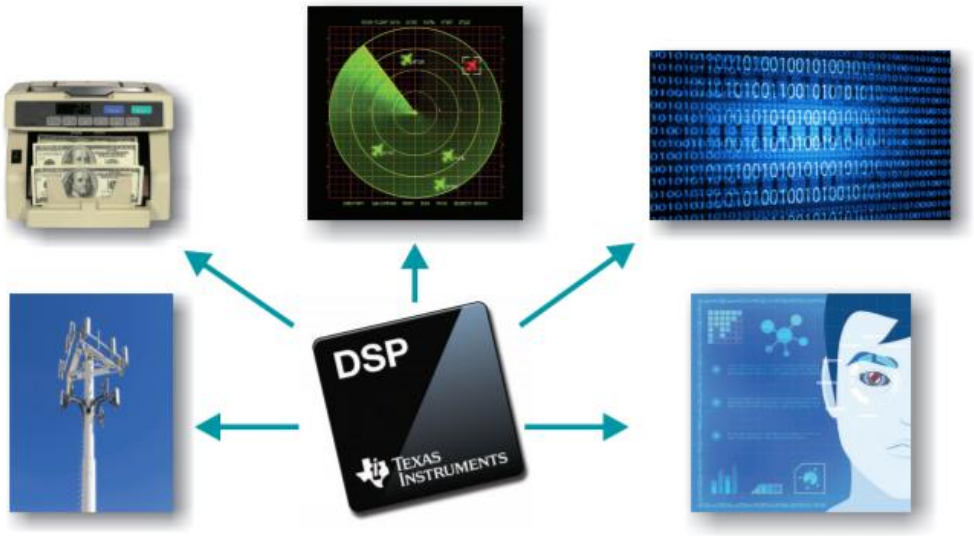
Example Diagram of SoC



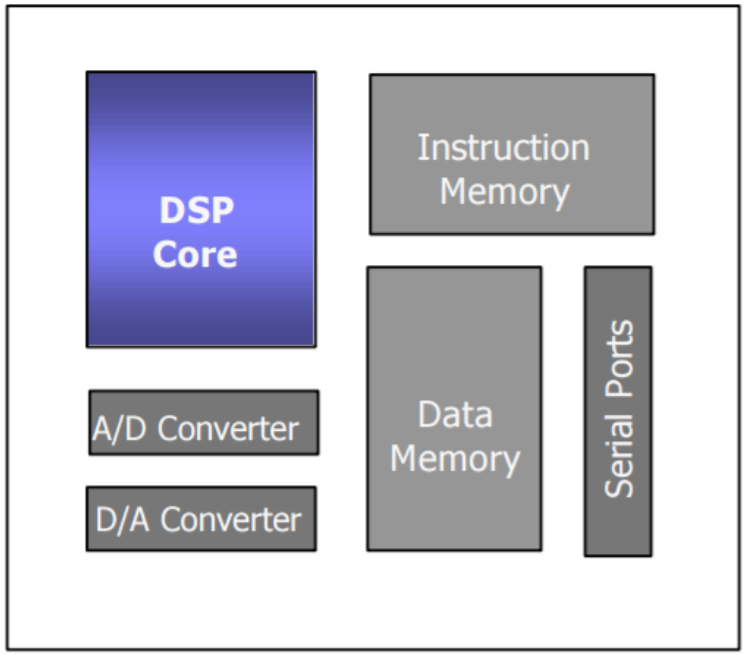
Introduction (7 of 13)

COTS: fixed architecture

- **Digital Signal Processor (DSP):**
  - Specialized microprocessor with its architecture optimized for digital signal processing (e.g. FFT, filters)
  - Dedicated blocks for mathematic operations (e.g. multiplier-accumulators (MAC), shift registers)
  - May have multiple peripherals (e.g. ADC, timer)
  - Separated Data/Instruction buses (Harvard architecture)
  - HIGH computing power for specific applications
  - May be used in Real Time applications (capable of low latency)
  - Single/Multi-thread processing



Example Diagram of DSP



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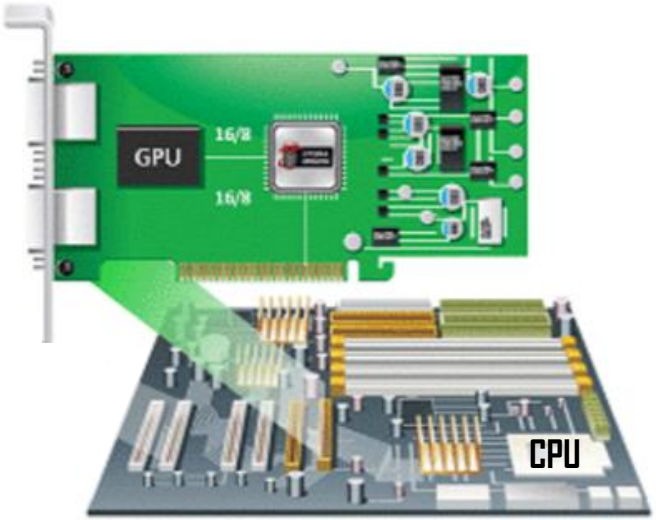
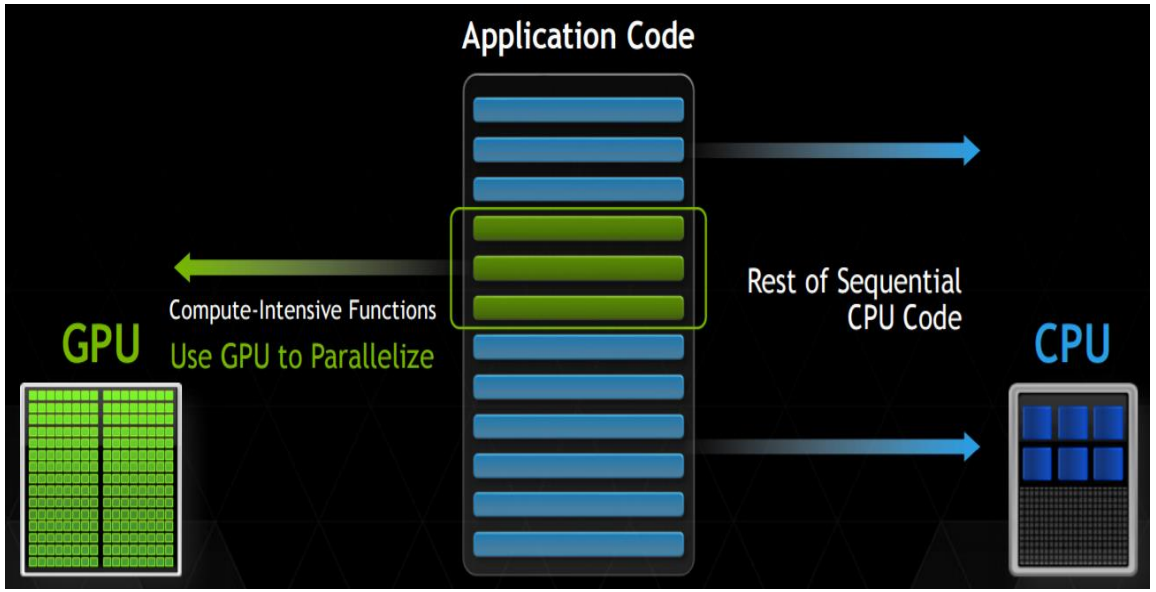
COTS: fixed architecture

- **Graphic Processor Unit (GPU):**
  - A GPU is a multi-core integrated circuit highly tuned for graphics generation
  - Used as co-processor in computers
  - Very common for graphics generation but becoming very popular for other applications (e.g. Medical, Physics)
  - VERY HIGH computing power for specific applications
  - Multi-thread processing
  - Complex parallel programming



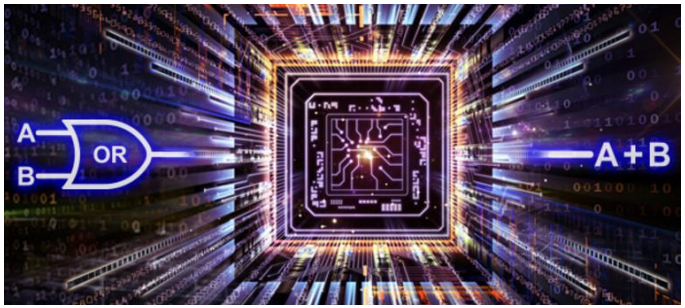
Example Diagram of Combined CPU + GPU Processing



Introduction (9 of 13)

COTS: configurable logic

- **Complex Programmable Logic Device (CPLD):**
  - Programmable Logic Device (PLD)
  - Features logic elements (e.g. AND gate), registers, I/O blocks (it may feature PLLs & memories)
  - Non-volatile (Flash-based) configuration memory
  - Very common for interfacing (glue logic) and/or implementing SIMPLE processing cores
  - Very good option for Real Time applications (capable of low, fixed and deterministic latency)
  - LOW computing power for specific applications
  - Parallel processing



Example Diagram of CPLD