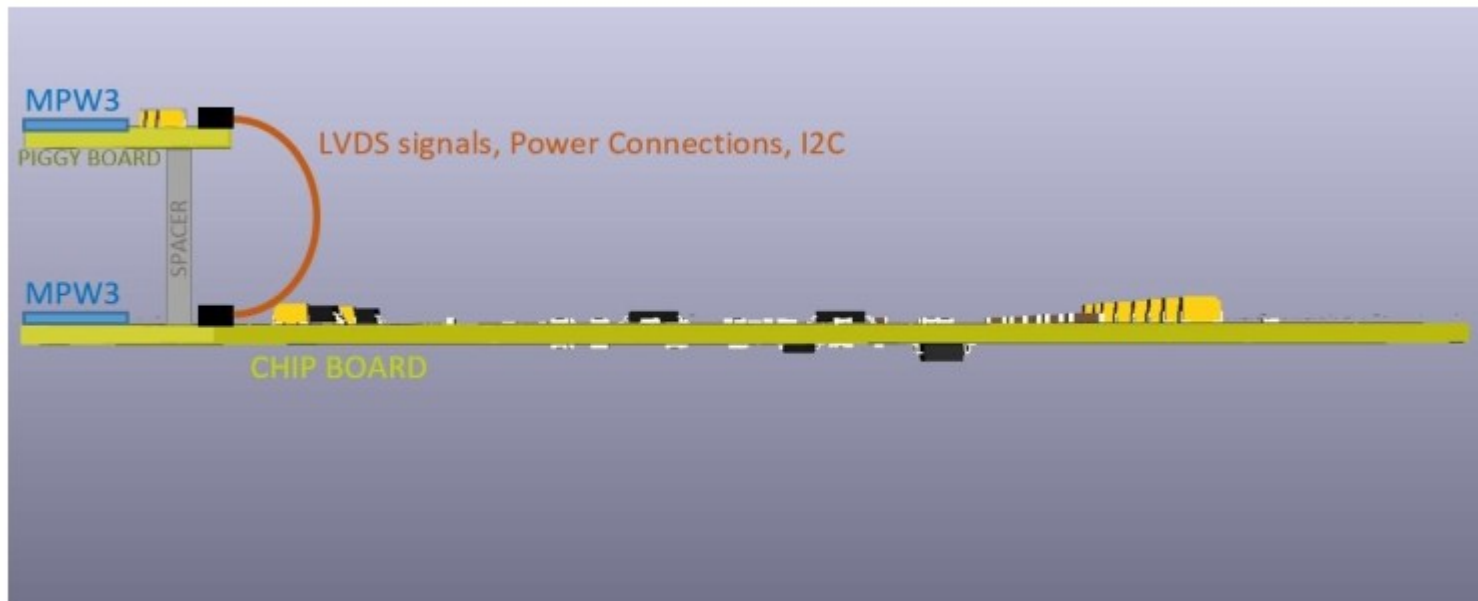


RD50-MPW3 chip and piggy boards

*Ricardo Marco Hernández
IFIC (CSIC-UV)*

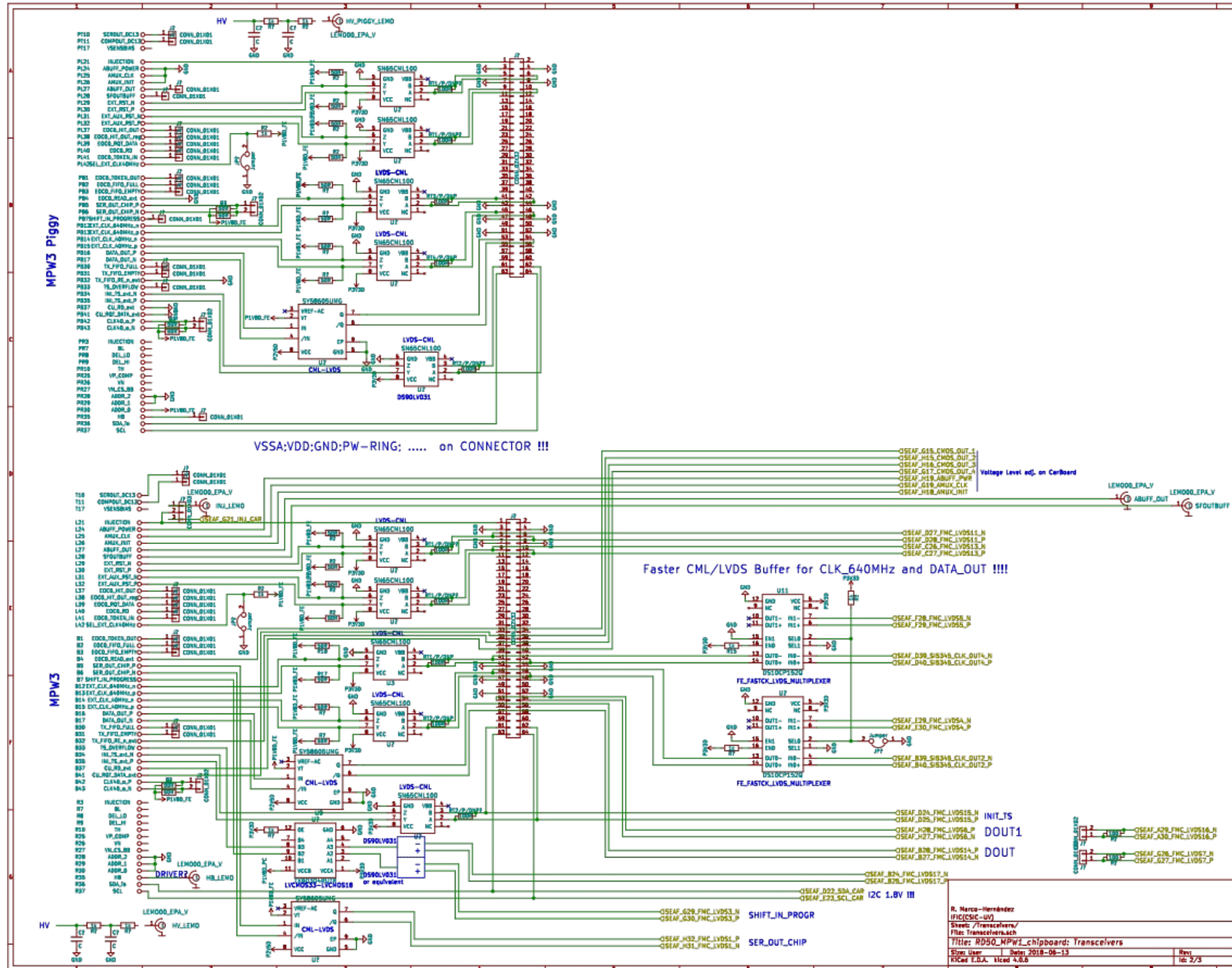
Proposal from HEPHY for RD50-MPW3 chip board and piggy board

- **RD50-MPW3 chip board for one MPW3:** similar to prior chip board versions (MPW1 and MPW2).
 - Features all functions of the chip and monitoring.
 - With SEAF connector to communicate with CaR board.
- **RD50-MPW3 piggy board: accommodates one MPW3 chip.**
 - It can be stacked on the chip board.
 - Connection to chip board required (connectors on both boards and cables between them).
 - Read out of chip board and piggy board by means of only one CaR board.
 - Space between boards adjustable (from few cm to tens of cm).



Proposal from HEPHY for RD50-MPW3 chip board and piggy board

- RD50-MPW3 chip board and piggy board preliminary schematic.



RD50-MPW3 chip board and piggy board connections

- **Signals between RD50-MPW3 chip board and piggy board.**
 - 6 LVDS differential pairs: 100 Ω impedance and bandwidth of 640 MHz required.
 - EXT_RST_P/N.
 - EXT_AUX_RST_P/N.
 - EXT_CLK_640MHZ_P/N.
 - EXT_CLK_40MHZ_P/N.
 - DATA_OUT_P/N.
 - INI_TS_ext_P/N.
 - 2 I2C signals (SDA/SCL): “slow” digital signals.
 - 1 pulsed signal (injection): “not very fast” pulsed signal (considered as analog).
 - 8-11 power supply levels: maximum consumption per power level lower than 500 mA assumed.
 - GND: common ground.
 - VDDA (1.8 V): analog circuits.
 - VSSA (1.3 V): pixel CSA (analog).
 - VDDC (1.8 V): pixel comparator (analog).
 - vdd! (1.8 V): digital circuits.
 - vdd_io (1.8 V): digital IO.
 - NW_RING (1.8 V): Nwell guard ring
 - VNSENBIAIS (1.8 V): DNWell bias (analog).
 - vdd_DIG0 (1.8V): **analog or digital?. Can be connected to VDDA or vdd!?.**
 - vdd_DIG1 (1.8V): **analog or digital?. Can be connected to VDDA or vdd!?.**
 - vdd_io_DIG (1.8 V): **Can be connected to vdd_io?.**

- **Signals between RD50-MPW3 chip board and piggy board (continuation).**
 - ...
 - 4 voltage references: low current.
 - TH (BL + V_{th}).
 - DEL_HI (0 V, 1.8 V).
 - DEL_LO (0 V, 1.8 V).
 - BL (~ 900 mV).

RD50-MPW3 chip board and piggy board connections

- LVDS signals require 100 Ω differential impedance cables with high bandwidth (640 MHz).

Table 7-6. Application-Driven Decisions Used When Selecting Cable Media

Cable Type	Cable Construction	Data Rates (Gbps)	Typical Markets	Gauge	Typical Media Lengths (meters)
Dual DVI	6 Data, 1 clock, 3 control	1.65	Consumer Digital Video	22, 24, 26, 28	5 to 30
HDMI	3 Data, 1 clock, 3 control	1.65	Consumer Digital Video	24, 26, 28	5 to 30
Category 5e	4 Data	Up to 3.125	Broad Market	26, 28	10
PCI-Express Gen2	X1, X2, X4, X8	5	PC	24, 26, 28	several feet, 10 meters
SATA-2	1 set bi-directional data pairs	3	Storage Applications	24, 26	several feet, 10 meters

From "LVDS Owner's Manual". Texas Instruments. 2008.

- Different possibilities for LVDS signals.
 - Use 2 8P8C-RJ45 (Ethernet) connectors with cat5e (100 MHz), cat6 (250 MHz), cat6A (500 MHz) or cat8 (1 GHz) cables.
 - 4 differential signals per connector.
 - Standard cables from 0.3 m to 10 m.
 - Use 2 HDMI connectors with standard (74.25 MHz) or high speed (340 MHz) cables.
 - 4 differential signals plus 7 additional signals available per connector.
 - Standard cables from 0.3 m to 10 m.
 - Use specific high speed connector and cable assembly.
 - More expensive solution.
 - See for example: <https://www.samtec.com/cables/high-speed>

RD50-MPW3 chip board and piggy board connections

HDMI pinout

Pin out



HDMI type A receptacle

- Pin 1** TMDS Data2+
- Pin 2** TMDS Data2 Shield
- Pin 3** TMDS Data2-
- Pin 4** TMDS Data1+
- Pin 5** TMDS Data1 Shield
- Pin 6** TMDS Data1-
- Pin 7** TMDS Data0+
- Pin 8** TMDS Data0 Shield
- Pin 9** TMDS Data0-
- Pin 10** TMDS Clock+
- Pin 11** TMDS Clock Shield
- Pin 12** TMDS Clock-
- Pin 13** Consumer Electronics Control (CEC)
- Pin 14** Reserved (HDMI 1.0-1.3a) Utility/HEAC+ (HDMI 1.4+, optional, HDMI Ethernet Channel (HEC) and Audio Return Channel (ARC))
- Pin 15** SCL (I²C serial clock for DDC)
- Pin 16** SDA (I²C serial data for DDC)
- Pin 17** Ground (for DDC, CEC, ARC, and HEC)
- Pin 18** +5 V (up to 50 mA)
- Pin 19** Hot Plug Detect (all versions) HEAC- (HDMI 1.4+, optional, HDMI Ethernet Channel and Audio Return Channel)

HDMI cable



8P8C/RJ45 pinout



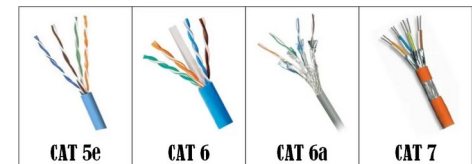
ANSI/TIA-568 T568A termination

Pin	Pair	Wire ^[d]	Color
1	3	tip	white/green
2	3	ring	green
3	2	tip	white/orange
4	1	ring	blue
5	1	tip	white/blue
6	2	ring	orange
7	4	tip	white/brown
8	4	ring	brown

ANSI/TIA-568 T568B termination

Pin	Pair	Wire ^[d]	Color
1	2	tip	white/orange
2	2	ring	orange
3	3	tip	white/green
4	1	ring	blue
5	1	tip	white/blue
6	3	ring	green
7	4	tip	white/brown
8	4	ring	brown

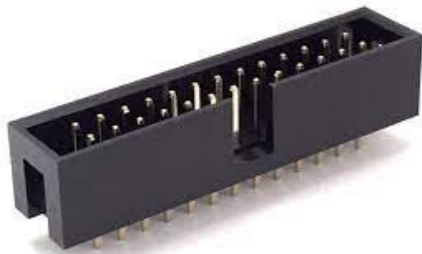
RJ45 cable



RD50-MPW3 chip board and piggy board connections

- Power levels, voltage reference levels and I2C/injection signals:
 - Through standard IDC connector and flat ribbon cable.
 - Maximum 2x17 positions required with GND interleaved between signals.
 - With HDMI connectors: I2C and injection signals can be transmitted using HDMI cables.
- Other possibilities:
 - Why not LVDS signals through IDC connector and flat ribbon twisted cable?
 - Differential impedance of flat ribbon twisted cable compatible with LVDS ($\sim 100 \Omega$).
 - With short lengths of cable (up to 3 m) is possible to transmit signal bandwidth up to ~ 200 MHz.
 - Why not using FFC (flat flexible cable) instead of flat ribbon twisted cable for LVDS signals?
 - Differential impedance compatible with LVDS ($\sim 100 \Omega$) and high bandwidth (~ 500 - 1000 MHz).
 - Limited length: max ~ 0.3 m.
 - Much less robust: not conceived for frequent plug/unplug cycles.
 - See: <https://www.digikey.es/en/product-highlight/m/molex/lvds-premo-flex-cable>

IDC connector



Flat ribbon twisted cable



Flat flexible cable



RD50-MPW3 chip board and piggy board connections

- Example of boards with 2 RJ45 connectors and IDC connector (2x20 positions):

