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The design and implementation of an ANN architecture for in-pixel signal processing

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Modern hybrid pixel X-Ray detectors produce more and more data, exceeding tens of GB/s, and so the communication with the detector becomes an important issue. One way to manage the issue of increased amount of data being produce by the detector, is the information extraction on the sensor level, before sending them to the control system. The information can be extracted with certain, fixed functionality as long as we do know precisely how the signal behaves, which is very difficult to predict due to imperfection of the technology etc., However, it is often possible to utilize an artificial neural network (ANN), which can be trained towards desired functionality.
With this work we present a design of a hardware processor suitable for implementation of the ANN having different architectures, like e.g. Multi-Level Perceptron (MLP). Designed using CMOS 28 nm, the area of the automatically synthetized block is lower than 150 um x150 um. With such as small size it is possible to fit the ANN inside a single pixel of an X-ray detector.
We present the design of the scalable processor, capable of providing an ANN functionality as well as we demonstrate an in-house developed tools, allowing automatic conversion of an ANN model designed with the TensorFlow library from Google, into a HDL code. The hardware code is written in SystemVerilog, and the synthesized module can perform calculations of a neural network with very high speed exceeding 400MHz. Our software-tool supports the conversion of an arbitrary multilayer perceptron neural network into a state machine module that can perform calculations. It is also dynamically reconfigurable so that the ANN operating in the hardware can be changed after deployment to an ASIC.
The project aims the in-pixel implementation towards x-ray photon energy estimation with the accuracy exceeding the accuracy of an ADC converter used to digitize the pulse generated by the photon.

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