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Digital signal processing for position-sensitive gamma ray detectors

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Room temperature semiconductor sensors (CdZnTe, TlBr) have been proven to be exceptionally performing in gamma-ray spectrometer for many applications [1,2,3]. In particular, the 3D position-sensitive Virtual Frisch-Grid (VFG) detector configuration is advantageous for integrating CZT crystals into large area arrays, where the signals captured by the anode, cathode and four pads electrodes, enable the 3D reconstruction of interaction points and measurements of the energies deposited in the event. The conventional ASIC architecture implementation of a suitable readout electronic for such applications consists of a low noise charge sensitive amplifier (CSA) and a pulse-shaping stage followed by a peak and time of peak detector [4]. Another approach is to couple a multi-channel front-end ASIC, where each channel is composed of a low noise CSA and shaper stage, to ADCs, forming a waveform “digitizer” and convert the captured signals into a time series of digital values. Then, an optimized Finite Impulsive Response (FIR) digital filter is applied to extract the information about energy and time of the particle interaction event. This solution adds the flexibility to adapt the signal processing parameters and tailor the optimal filter on a specific digitized set of waveforms without being constrained by the implemented ASIC electronic. Moreover, further corrections can be applied to the processed data to mitigate detector defects and non-uniformities improving the energy resolution response [5].

In this work, we present the development of a waveform digitizer composed of the front-end ASIC [6] and the readout electronic (ADCs and FPGA). Also, we describe the optimization of the FIR filter applied to characterize the energy resolution of gamma-ray detectors, demonstrating the energy resolution of ~1% (FWHM) at 662 keV.

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Primary author: PINAROLI, Giovanni

Co-authors: BOLOTNIKOV, Aleksey (Brookhaven National Laboratory); CARINI, Gabriella; FRIED, Jack (Brookhaven National Laboratory (US)); DEPTUCH, Grzegorz; HERRMANN, Sven (Brookhaven National Laboratory)

Presenter: PINAROLI, Giovanni

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