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Characterization of 3.2 Gbps readout in 65 nm CMOS technology

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The current trends in particle detector design are increasing pixel resolution and readout rates. Therefore, new requirements for the readout systems and their bandwidths have arisen. Fast differential serial communication is mainly used for its robustness against external interference and better electromagnetic compatibility than the legacy serial-parallel communication. However, its implementation provides extra challenges [1-2].

Transmitters described in this work use channel encoding that adds bit redundancy to assure the neutral DC balance of the transmission line. The encoding 8b/10b also provides enough state transitions for the receiver clock recovery circuit to lock onto and provides word error correction. Encoded data then passes into a chain of registers that serialize the data with the phase-locked loop synthesized clock of 1.6 GHz, as shown in Figure 1. The transmitter drivers use current-mode logic with 1-tap preemphasis to ensure proper adaptation to the transmission channel. Current approaches and design of gigabit transmitter implemented in 65 nm CMOS technology will be presented in this work. It will describe the functionality of its internal blocks and data flow. Its functionality, jitter and channel performance will be characterized.

[1] C. Chen et al., "Characterization of a gigabit transceiver for the ATLAS inner tracker pixel detector readout upgrade,"Journal of Instrumentation, vol. 15, no. 3, pp. T03005–T03005, Mar. 2020, doi: 10.1088/1748-0221/15/03/t03005.

[2] E. A. Lee and D. G. Messerschmitt, Digital communication. Springer Science & Business Media, 2012.

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