iWoRiD 2022
23rd International Workshop on Radiation Imaging Detectors
26 – 30 June 2022
Riva del Garda, Italy

Contribution ID: **91** Type: **Poster**

A 2.56 Gbps or 10 Gbps Clock Data Recovery ASIC for Detector Front-end Readout

Wednesday, 29 June 2022 17:49 (1 minute)

The bi-directional serial optical data transceiver system is employed between the front-end and the back-end in the detector readout electronics. The low jitter clock data recovery (CDR) ASIC is one of the key components in the high-speed serial down link direction. It receives a pair of high-speed serial input data, recovers the clock signal from the data and resamples the input data at the same time. Some similar ASICs used in particle physics experiments have been reported, such as the GBTx [1] (2.56 Gbps CDR in down link) and LpGBT [2] [3] (2.56 Gbps CDR in down link). The proposed CDR ASIC has been fabricated in a 55 nm CMOS technology for detector front-end readout, which is selectable to operate at 2.56 Gbps or 10 Gbps data rate.
The CDR ASIC consists of an input equalizer stage, a bang-bang phase detector (BBPD), a charge pump circuit (CP), a low-pass filter (LPF), two selectable LC voltage-controlled oscillator (LC-VCO) circuits and a SPI module. The input equalizer stage adopts a 5-step continuous-time linear equalizer (CTLE) structure [4] to compensate the high frequency loss from the system level including PCB traces, bonding wires and pads. The CTLE boosts maximum up to 9.8 dB at 7 GHz while providing a DC gain of 4.7 dB. The BBPD is used to detect the phase difference between the input data jump edge and sampling clock. To obtain low leakage current and reduce dynamic mismatch, two feedback operational amplifiers are employed in the charge pump circuit. To accommodate the two different data rates (2.56 Gbps or 10 Gbps), the two LC-VCOs which is configured by the SPI module are employed in the CDR. The LC-VCO1 and LC-VCO2 circuits can operate at 2.56 GHz and 10 GHz, respectively. They adopt the two-step capacitor tuning structure and the capacitor array unit to obtain a reasonable frequency range and an optimized Q factor performance.

The low jitter CDR ASIC was presented with a 2.56 Gbps or 10 Gbps data rate in a 55 nm CMOS technology for detector front-end readout and the ASIC features a size of 1.5 mm ⊠ 1.5 mm. Widely-open resampling data eye has been observed at 2.56 Gbps or 10 Gbps data rate. The simulation results show that the jitters of 2.56 Gbps or 10 Gbps resampling data eye are 1.4 ps and 2.8 ps, respectively. At 2.56 GHz, the recovered clock achieves a phase noise of -112 dBc/Hz at 1 MHz offset and a jitter of 1.2 ps. At 10GHz, the recovered clock achieves a phase noise of -106 dBc/Hz at 1 MHz offset and a jitter of 1.5 ps. The chip has been taped out and the tests are planned to be conducted in this April. The test and total ionizing dose (TID) test will be performed. The test results will be reported in the meeting.

[1] Paulo Moreira et al., The Radiation Hard GBTX Link Interface Chip. https://indico.cern.ch/event/267408/attachments/477815/661090/es
[2] Paulo Moreira et al., lpGBT –a User's Perspective. https://indico.cern.ch/event/697988/contributions/3075493/attachments/1720215/277
[3] Stefan Biereigel et al., A Low Noise Fault Tolerant Radiation Hardened 2.56 Gbps Clock-Data Recovery Circuit With High Speed Feed Forward Correction in 65 nm CMOS. IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS–I 2019.
[4] S. Gondi et al., A 10 Gb/s CMOS Adaptive Equalizer for Backplane Applications, IEEE ISSCC 2005 (2005) 328-329.

This work is supported by General Program of National Natural Science Foundation of China (Grant No. 11875145).

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Session Classification: Poster